HIGH-VOLTAGE MIXED-SIGNAL IC

UC8171

All-in-one driver IC w/ Timing Controller for
White/Black/Red Dot-Matrix Micro-Cup ESL

PP Specifications
Datasheet Revision: 0.8 (for TFT Module Use only)

IC Version: c_C
December 5, 2019

ULTRACHIP

The Coolest EPD Driver, ˇEver!

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UC8171

All-in-one driver IC with Timing Controller for White/Black/Red Dot-Matrix Micro-Cup ESL

INTRODUCTION

The UC8171 is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VDH/VDL (±2.4V~±15.0V) and VDHR (+2.4V~+15.0V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

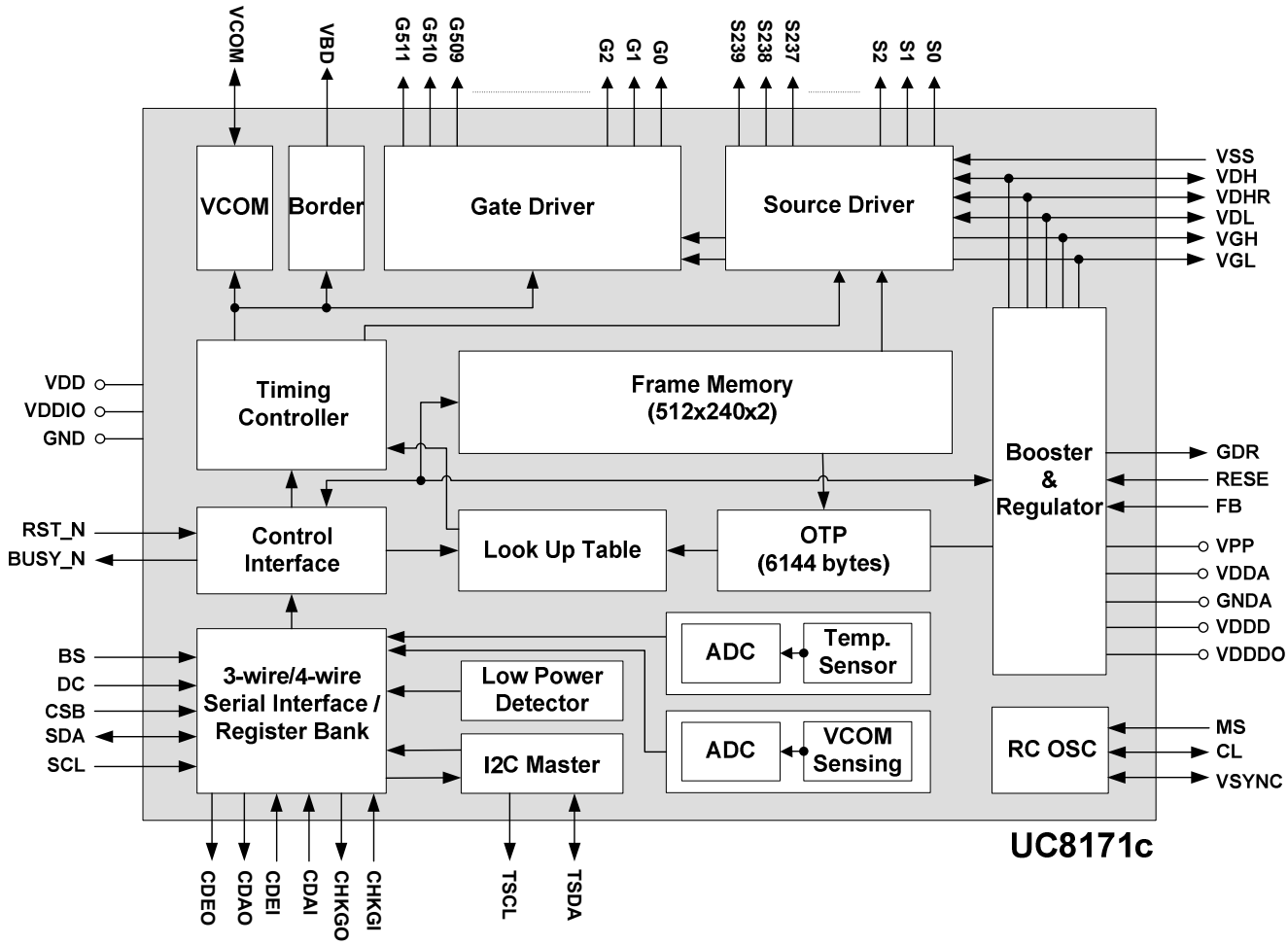
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several resolutions
  - Up to 240 source x 512 gate resolution + 1 border + 1 VCOM
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: 2 or more chips cascade mode
- Memory (Max.): 240 x 512 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 °C ± 2.0°C / 8-bit status
  - Off-Chip: -55~125°C ± 2.0°C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection
  - V_{DD} < 2.5V or 2.4V or 2.3V or 2.2V (by setting)
- OSC / PLL: On-chip RC oscillator
- VCOM:
  - AC-VCOM / DC-VCOM (by LUT)
  - Support VCOM sensing (6-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +9V~+12V, +17V~+20V (programmable)
  - VGL: -9V~-12V, -17V~-20V (programmable)
  - VDH: +2.4 ~ +15.0V (programmable, black/white)
  - VDL: -2.4 ~ -15.0V (programmable, black/white)
  - VDHR: +2.4 ~ +15.0V (programmable, red)
- Supply voltage: 2.3~ 3.6V
- OTP: 6K-byte OTP for LUTs and Settings
- Package: COG
- Source/Gate bump information
  - Bump pitch: 14 μM (output bump)
  - Bump space: 0 μM (2uM stagger-overlapped)
  - Bump surface: 1200 μM^2

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UC8171cHAC-U0X3-3	IC thickness: 300uM, with 3” double-faced tray
UC8171cHAC-U0X3-4	IC thickness: 300uM, with 4” double-faced tray

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	7	PWR	Digital power
VDDA	10	PWR	Analog power
VDDIO	7	PWR	IO power
VDDDO	5	PWR	Digital power output (1.8V)
VDDD (VDDDI)	5	PWR	Digital power input (1.8V)
VPP	7	PWR	OTP program power (7.75V)
VDM	6	PWR	Analog Ground.
GND	25	PWR	Digital Ground.
GNDA	17	PWR	Analog Ground
LDO PINS			
VDH (VSH)	9	I/O	Positive source driver Voltage (+2.4V ~ +15V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +15V)
VDL (VSL)	9	I/O	Negative source driver voltage (-2.4V ~ -15V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. H: 3-wire interface.
RST_N	1	I (Pull-up)	Global reset pin. Low: active. When RST_N becomes low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 50us.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	2	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDEI	1	I	Cascade signal input pin. Connect to GND if not used.
CDEO	1	O	Cascade signal output pin. Leave it open if not used.
CDAI	1	I	Cascade data input pin. Connect to GND if not used.
CDAO	1	O	Cascade data output pin. Leave it open if not used.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.

Pin (Pad) Name	Pin Count	Type	Description
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data Connect to GND if BS=High.
I^2C INTERFACE			
TSCL	2	O (open-drain)	I^2C clock (External pull-up resistor is necessary.) Leave them open if not used.
TSDA	2	I/O (open-drain)	I^2C data (External pull-up resistor is necessary.) Leave them open if not used.
OUTPUT PINS			
S0~S239 (S<0>~S<239>)	240	O	Source driver output signals.
G0~G511 (G<0>~G<511>)	512	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD (VBD<0>, VBD<1>)	1, 1	O	Border output pins.
BOOSTER PINS			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	11	I/O	Positive Gate voltage.
VGL	11	I/O	Negative Gate voltage.
CHECK PANEL PINS			
CHKGI	1	I (Pull-down)	Check panel break input. Leave open if it is not used.
CHKGO	1	O	Check panel break output. Leave open if it is not used.
RESERVED PINS			
VSYNC	2	O	Reserved pins. Leave it floating.
TEST1~TEST3	1x3	I	Reserved pins. Leave it floating or connected to VSS.
TEST4~TEST7	1x4	O	Reserved pins. Leave it floating.
TEST8~TEST13	1x6	I	Reserved pins. Leave it floating.
DUMMY	37	-	Reserved pins. Leave it floating.
GD<0>~GD<3>	1x4		Reserved pins. Leave it floating.
NC	12	-	Not Connected.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	--	--	#	#	#	#	#	#	REG, KW/R, UD, SHL, SHD_N, RST_N	0FH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	--	--	#	#	#	VSR_EN, VS_EN, VG_EN	03H
		0	1	--	--	--	--	#	#	#	#	VCOM_HV, VG_LVL[2:0]	00H
		0	1	--	--	#	#	#	#	#	#	VDH_LVL[5:0]	26H
		0	1	--	--	#	#	#	#	#	#	VDL_LVL[5:0]	26H
		0	1	--	--	#	#	#	#	#	#	VDHR_LVL[5:0]	03H
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data (240x512):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-7:n]	-
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (240X512):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-7:n]	-
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
14	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
16	K2W LUT (LUTKW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
17	W2K LUT (LUTWK / LUTW) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
18	K2K LUT (LUTKK / LUTK) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
19	Border LUT (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1		25H
		0	1	#	#	#	#	#	#	#	#	Level select-0~3[1:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-0[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-1[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-2[7:0]	-
		0	1	:	:	:	:	:	:	:	:	Number of frames-3[7:0]	-
		0	1	#	#	#	#	#	#	#	#	Times to repeat[7:0]	-
20	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	#	--	--	--	--	--	--	STATE_XON[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
21	KW LUT option (KWOPT)	0	0	0	0	1	0	1	0	1	1		2BH
		0	1	--	--	--	--	--	--	#	#	ATRED, NORED	00H
		0	1	#	#	--	--	--	--	--	--	KWE[9:8]	00H
		0	1	#	#	#	#	#	#	#	#	KWE[7:0]	00H
22	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	--	--	#	#	#	#	FRS[3:0]	04H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
23	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
24	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
25	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H
26	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43H
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
27	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44H
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
28	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50H
		0	1	#	--	#	#	--	--	#	#	BDZ, BDV[1:0], DDX[1:0]	31H
		0	1	--	--	--	#	#	#	#	#	SDEND, CDI[3:0]	07H
29	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	--	--	--	--	--	--	--	#	LPD	01H
30	End Voltage Setting (EVS)	0	0	0	1	0	1	0	0	1	0		52H
		0	1	--	--	--	--	#	--	#	#	VCEND, BDEND[1:0]	02H
31	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
32	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	F0H
		0	1	--	--	--	--	--	--	#	#	VRES[9:0]	02H
		0	1	#	#	#	#	#	#	#	#		00H
33	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00H
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
34	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFH
		1	1	--	--	--	--	#	#	#	#	CHIP_REV[3:0]	0CH
35	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
36	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
37	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	--	#	#	#	#	#	#	VV[5:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
38	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	--	#	#	#	#	#	#	VDCS[5:0]	00H
39	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00H
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	EFH
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	01H
		0	1	#	#	#	#	#	#	#	#		FFH
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
40	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
41	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
42	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
43	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
44	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
45	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0H
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
46	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3H
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H
47	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
48	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	0	1	**-**	**-**	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH

REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	-	-	VSR_EN	VS_EN	VG_EN	07H
	0	1	-	-	-	-	VCOM_HV	VG_LVL[2:0]			00H
	0	1	-	-	VDH_LVL[5:0]						26H
	0	1	-	-	VDL_LVL[5:0]						26H
	0	1	-	-	VDHR_LVL[5:0]						03H

VSR_EN: Source LV power selection
0 : External source power from VDHR pins
1 : Internal DC/DC function for generating VDHR. (Default)

VS_EN: Source power selection
0 : External source power from VDH/VDL pins
1 : Internal DC/DC function for generating VDH/VDL. (Default)

VG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_HV: VCOM Voltage Level
0 : VCOMH=VDH+VCOM_DC, VCOML=VDL+VCOM_DC. (Default)
1 : VCOMH=VGH, VCOML=VGL

VG_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 **(Default)**	VGH=20V, VGL= -20V

VDH_LVL[5:0]: Internal VDH power selection for K/W pixel.(**Default value: 100110b**)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	**100110**	**10.0 V**	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

VDL_LVL[5:0]: Internal VDL power selection for K/W pixel. (**Default value: 100110b**)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	**100110**	**-10.0 V**	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	111010	-14.0 V
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

VDHR_LVL[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 000011b**)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	**3.0 V**	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	03H
	0	1	**-**	**-**	T_VDS_OFF[1:0]		**-**	**-**	**-**	**-**	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA[7:6]		BT_PHA[5:3]			BT_PHA[2:0]			17H
	0	1	BT_PHB[7:6]		BT_PHB[5:3]			BT_PHB[2:0]			17H
	0	1	-	-	BT_PHC[5:3]			BT_PHC[2:0]			17H

BT_PHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BT_PHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BT_PHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BT_PHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “K/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	1	1	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	--
	0	1	:	:	:	:	:	:	:	:	--
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	--

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “NEW” data to SRAM.

In KWR mode, this command writes “RED” data to SRAM.

(13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	0	0	0	1	0	1	1	1	17H
	0	1	1	0	1	0	0	1	0	1	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host’s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores VCOM Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:

D[7:6], D[5:4], D[3:2], D[1:0]: Level Selection

00b: VCOM_DC
01b: VDH+VCOM_DC (VCOMH)
10b: VDL+VCOM_DC (VCOML)
11b: Floating

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

(15) W2W LUT (LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38:

Level Selection.

00b: GND
01b: VDH
10b: VDL
11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43:

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

(16) K2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for K2W or Red (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0	22H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:

Level Selection.

00b: GND
01b: VDH
10b: VDL
11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42, 45~48, 51~54, 57~60:

Number of Frames

0000 0000b: 0 frame
: :
: :
1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:

Times to Repeat

0000 0000b: 0 time
: :
: :
1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

(17) W2K LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

(18) K2K LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

(19) BORDER LUT (LUTBD) (R25H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for Border (43-byte command, Bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1	25H
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		--
	0	1	NUMBER OF FRAMES-0								--
	0	1	NUMBER OF FRAMES-1								--
	0	1	NUMBER OF FRAMES-2								--
	0	1	NUMBER OF FRAMES-3								--
	0	1	TIMES TO REPEAT								--

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2~7, 8~13, 14~19, 20~25, …), while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38:

Level selection.

00b: VCOM
01b: VDH
10b: VDL
11b: VDHR

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43:

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Only 7 LUTBD groups are used in KW mode or KWR mode.

(20) LUT OPTION (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	0	0	1	0	1	0	1	0	2AH
	0	1	STATE_XON[9:8]		-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H

This command sets XON control enable.

STATE_XON[9:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

00 0000 0000b: no All-Gate-ON

00 0000 0001b: State-1 All-Gate-ON

00 0000 0011b: State-1 and State2 All-Gate-ON

: :

(21) KW LUT OPTION (KWOPT) (R2BH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
KW LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	2BH
	0	1	-	-	-	-	-	-	ATRED	NORED	00H
	0	1	KWE[9:8]		-	-	-	-	-	-	00H
	0	1	KWE[7:0]								00H

This command sets KW LUT mechanism option in KWR mode's LUT and only valid in K/W/R mode.

{ATRED, NORED}: KW LUT or KWR LUT selection control

ATRED	NORED	Description
0	0	KWR LUT always
0	1	KW LUT only
1	0	Auto detect by red data
1	1	KW LUT only

KWE[9:0]:

KW LUT enable control bits. Each bit controls one state, KWE[0] for state-1, KWE[1] for state-2, … .

At least 1 Enable Control bit should be set when KW LUT only is selected in KWR mode.

00 0000 0001b: KW LUT enable in State-1

00 0000 0011b: KW LUT enable in State-1 and State2

00 0000 1011b: KW LUT enable in State-1, State2 and State-4

(22) PLL CONTROL (PLL) (R30H)

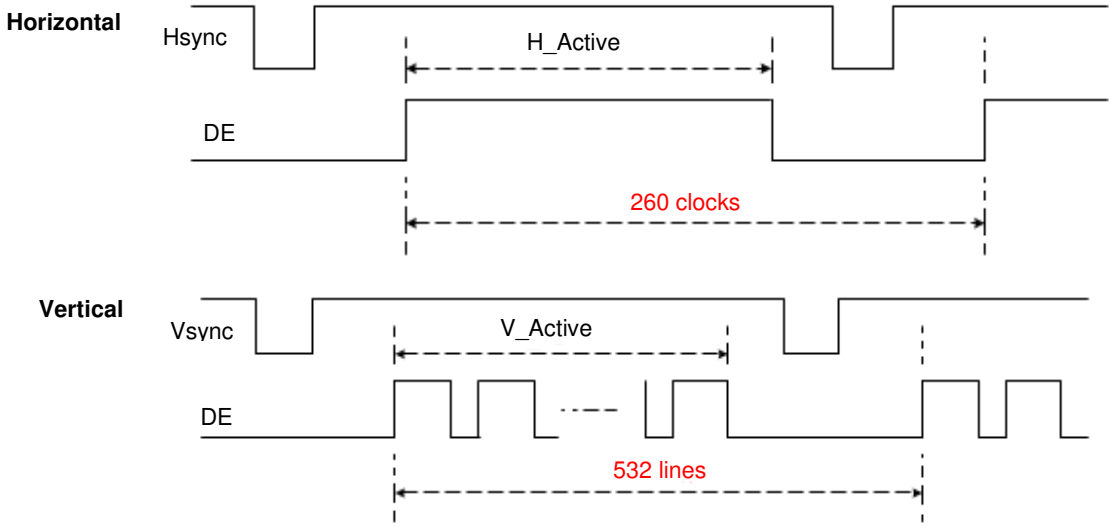
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30H
	0	1	-	-	-	-	FRS[3:0]				04H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[3:0]: Frame rate setting

FRS	Frame rate
0000	10Hz
0001	20Hz
0010	30Hz
0011	40Hz
0100	**50Hz**
0101	60Hz
0110	70Hz
0111	80Hz

FRS	Frame rate
1000	90Hz
1001	100Hz
1010	110Hz
1011	120Hz
1100	130Hz
1101	140Hz
1110	150Hz
1111	200Hz



(23) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temp. (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temp. (°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

P.S. Temperaure sensor is various at 85C.

(24) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calibration
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calibration
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(25) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(26) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(27) PANEL GLASS CHECK (PBC) (R44H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	44H
	1	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(28) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	BDZ	-	BDV[1:0]		N2OCP	-	DDX[1:0]		31h
	0	1	-	-	-	SDEND	CDI[3:0]				07H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

BDZ: Border Hi-Z control

0: Border output Hi-Z disabled (default) 1: Border output Hi-Z enabled

BDV[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

N2OCP: Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default) 1: Copy NEW data to OLD data enabled

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

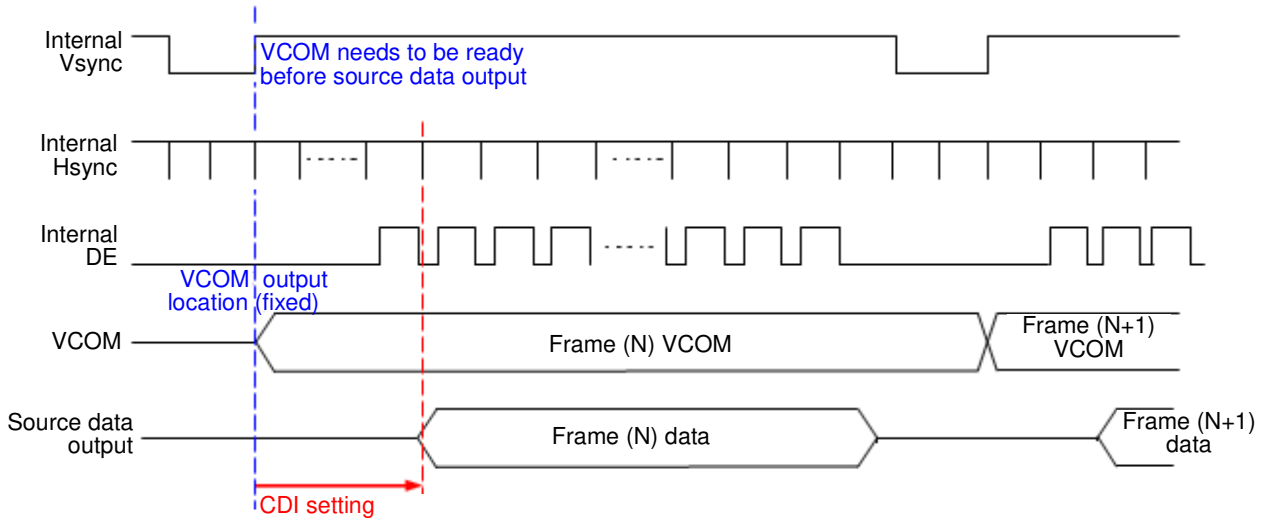
SDEND: source driving ending

0: source driver channels output 2-frame 0V at the end
1: source driver channels keep the last state at the end

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



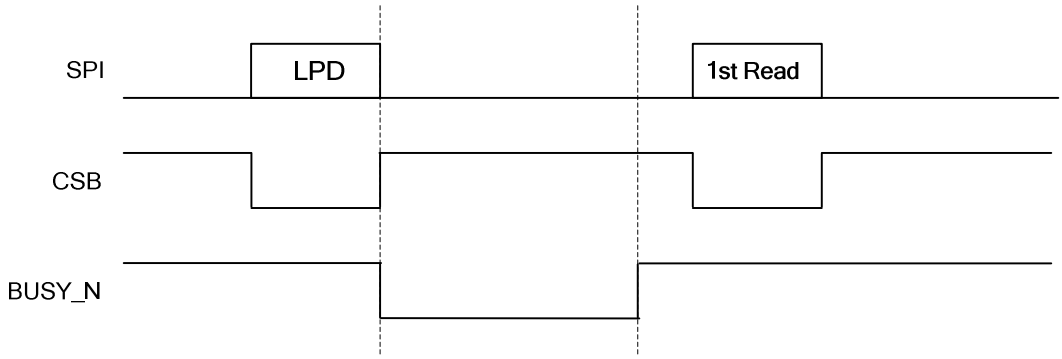
(29) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD} < 2.5V, 2.4V, 2.3V, or 2.2V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(30) END VOLTAGE SETTING (EVS) (R52H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
End Voltage Setting	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	52h
	0	1	-	-	-	-	VCEND	-	BDEND[1:0]		02h

This command selects source end voltage and border end voltage after LUTs are finished.

VCEND: VCOM end voltage selection

0b: VCOM_DC 1b: floating

BDEND[1:0]: Border end voltage selection

00b: 0V 01b: 0V **10b: VCOM_DC** 11b: floating

(31) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

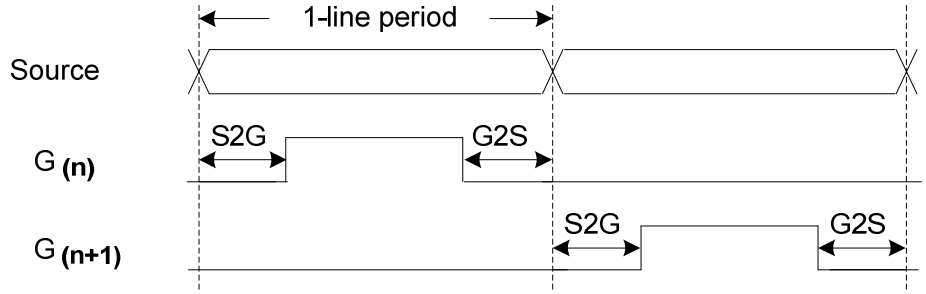
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 667 nS.



(32) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	HRES[7:3]					0	0	0	F0h
	0	1	-	-	-	-	-	-	VRES[9]	VRES[8]	02h
	0	1	VRES[7:0]								00h

This command defines resolution setting.

HRES[7:3]: Horizontal Display Resolution (Value range: 01h ~ 1Eh)

VRES[9:0]: Vertical Display Resolution (Value range: 01h ~ 200h)

Active channel calculation, assuming HST[7:0]=0, VST[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[9:0] – 1

Source: First active source = S0;
Last active source = HRES[7:3]*8 – 1

Example: 128 (source) x 272 (gate), assuming HST[7:0]=0, VST[8:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[8:0] = 272, 272 – 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[7:3]=16, 16*8 – 1 = 127)

(33) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source). (Value range: 00h ~ 1Dh)

VST[8:0]: Vertical Display Start Position (Gate). (Value range: 000h ~ 1FFh)

Example : For 128(Source) x 240(Gate)
HST[7:3] = 4 (HST[7:0] = 4*8 = 32),
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (VRES[8:0] = 240, VST[8:0] = 32, 240-1+32=271)

Source: First active source = S32 (HST[7:0]= 32),
Last active source = S239 (HRES[8:0] = 128, HST[7:0] = 32, 128-1+32=239)

(34) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	LUT_REV								FFh
	1	1	-	-	-	-	CHIP_REV[3:0]				0Ch

The LUT_REV is read from OTP address = 0x001 or 0xC01.

CHIP_REV[3:0]: Chip Revision, fixed at 1100b.

(35) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ Flag	I²C_ERR	I²C_ BUSYN	Data_ Flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_Flag: Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

Data_Flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(36) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(37) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[5:0]						00h

This command gets the VCOM value.

VV[5:0]: VCOM Value Output

VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05

(38) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	-	VDCS[5:0]						00h

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	others	-3.00

(39) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	1	0	0	0	0	90h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	HRED[7:3]					1	1	1	Efh
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	01h
	0	1	VRED[7:0]								FFh
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (Value range: 00h~1Dh)

HRED[7:3]: Horizontal end channel bank. (Value range: 00h~1Dh). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (Value range: 000h~1FFh)

VRED[8:0]: Vertical end line. (Value range: 000h~1FFh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(40) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(41) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(42) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(43) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

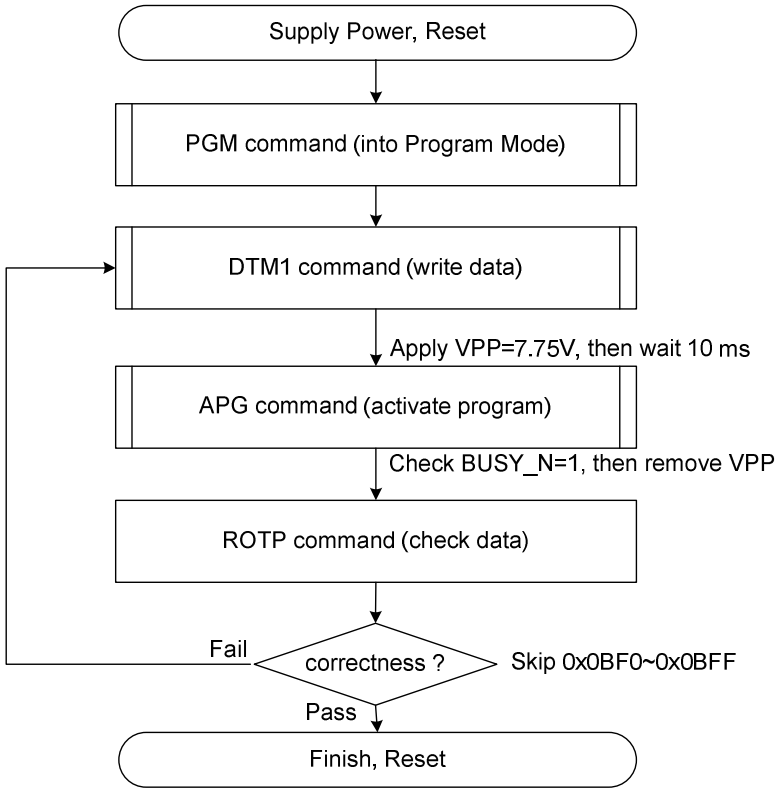
The BUSY_N flag would fall to 0 until the programming is completed.

(44) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



The sequence of programming OTP.

(45) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS_SET[7:0] registers.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

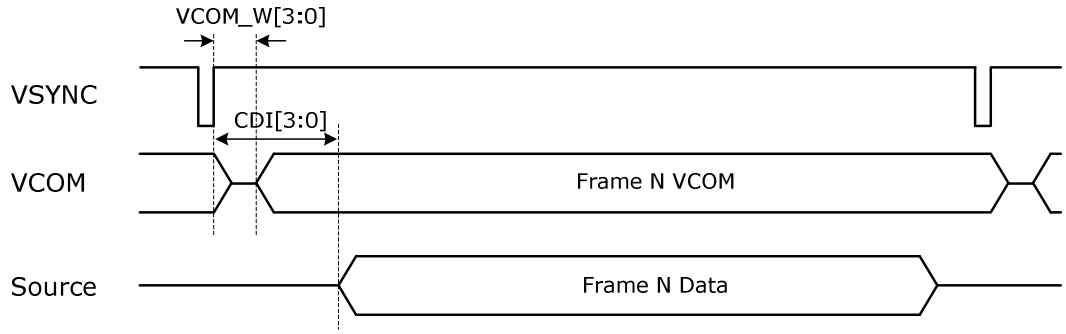
1: Output clock at CL pin to slave chip.

(46) POWER SAVING (PWS) (RE3H)

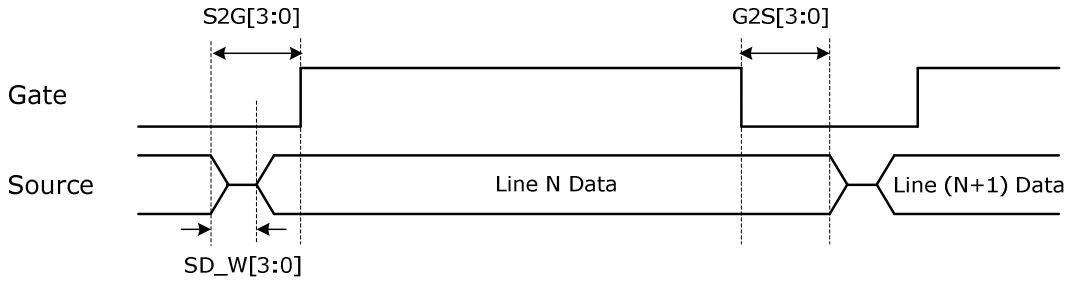
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (Unit: line period)



SD_W[3:0]: Source power saving width (Unit: 660nS)



(47) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(48) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

HOST INTERFACES

UC8171 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

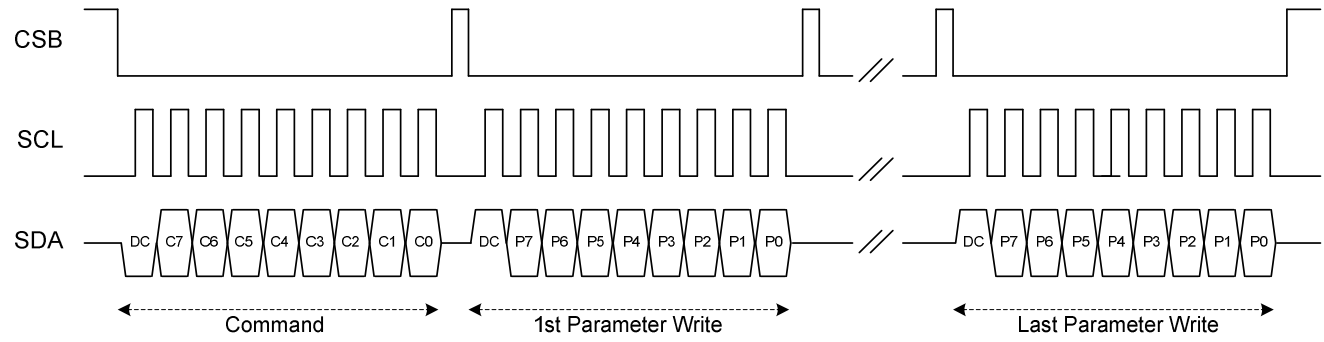


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

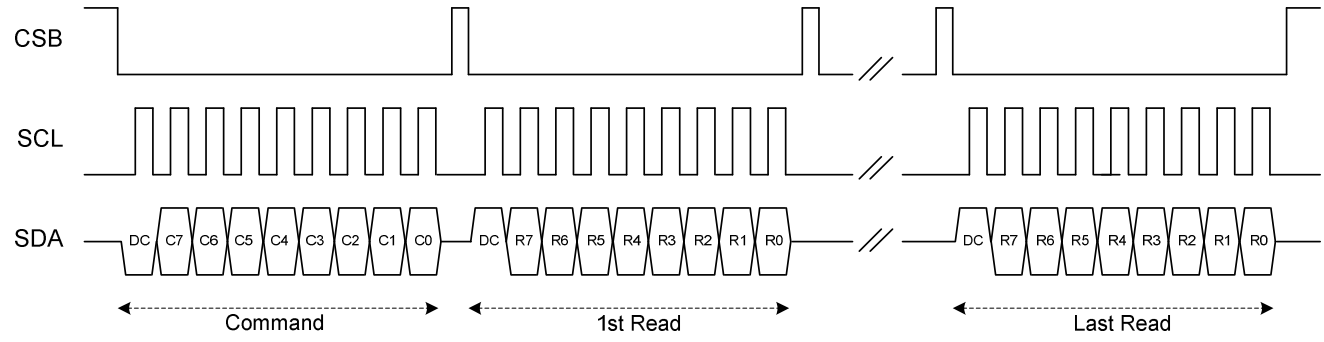


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

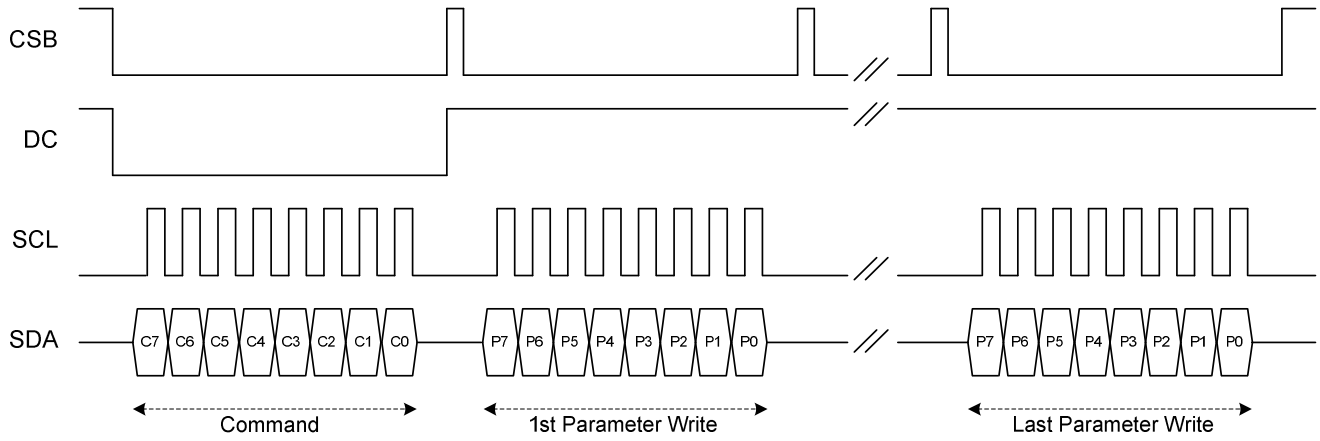


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

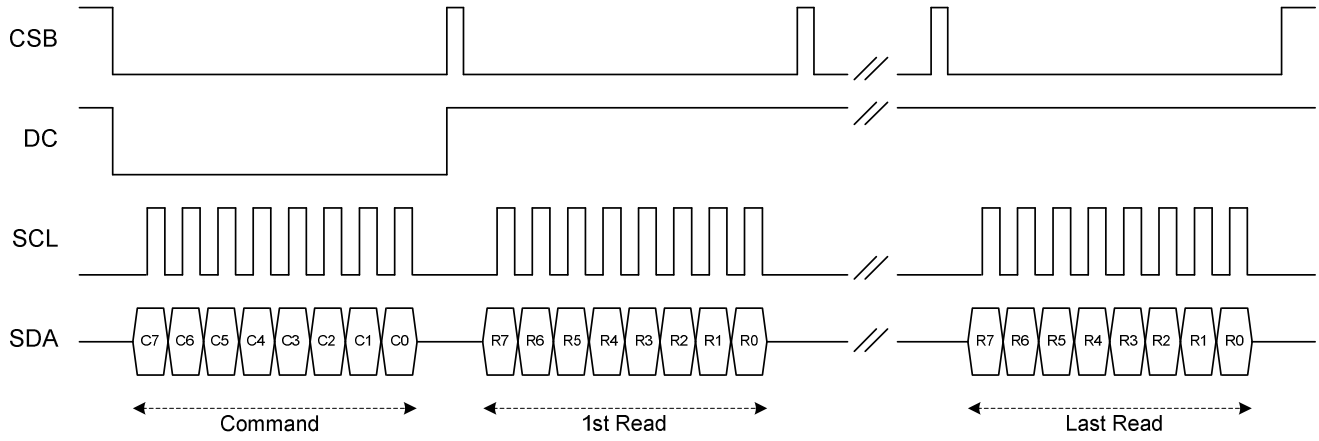
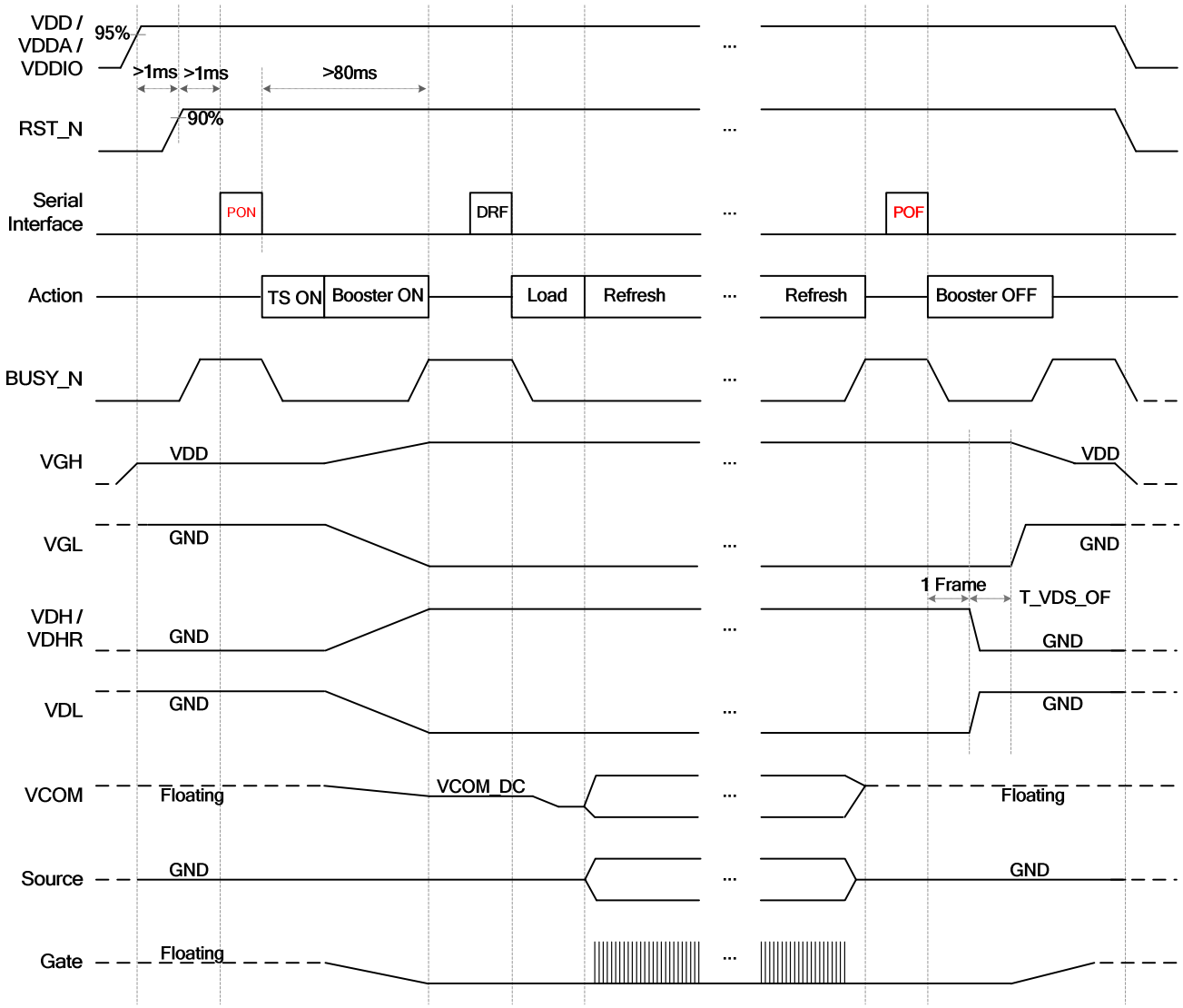


Figure: 4-wire SPI read operation

POWER MANAGEMENT

Power ON/OFF Sequence

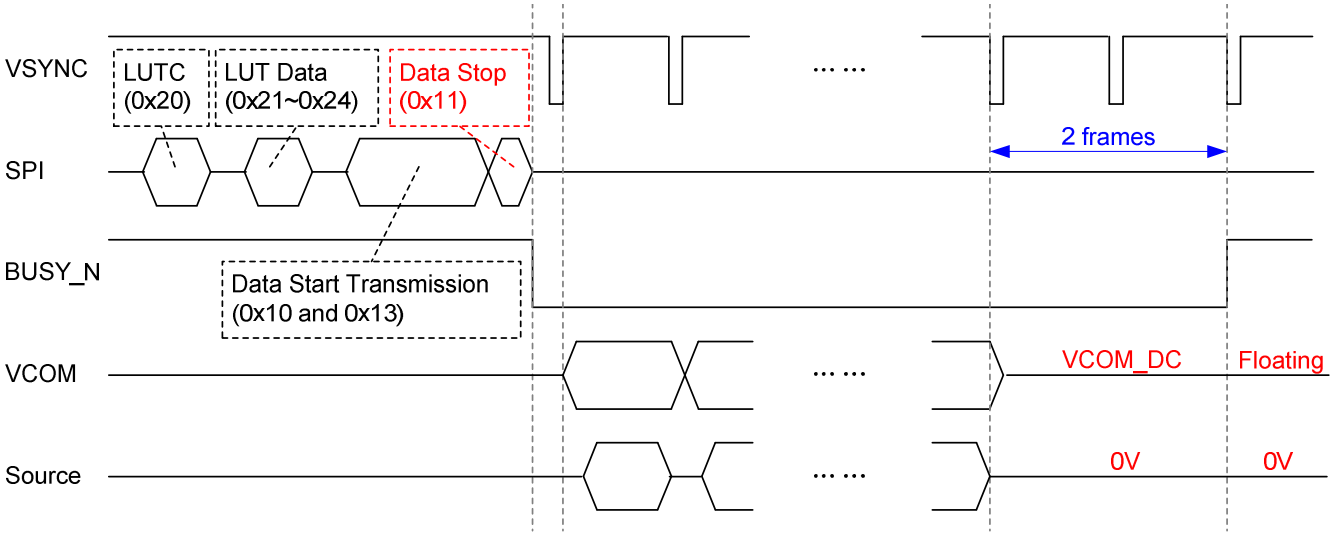
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



Data Transmission Waveform

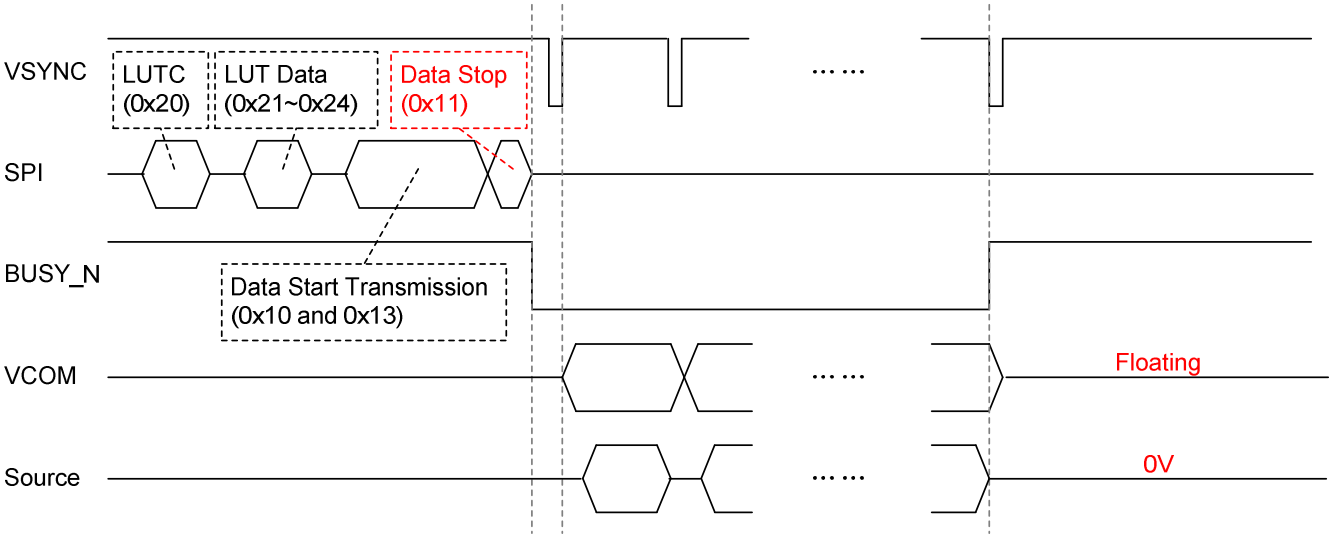
Example 1: After 3 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

1. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=0.
2. Meet the state whose Times to Repeat =0 and VCEND=0
3. Meet the state whose all Number of Frames =0 and VCEND=0



Example2: After 4 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

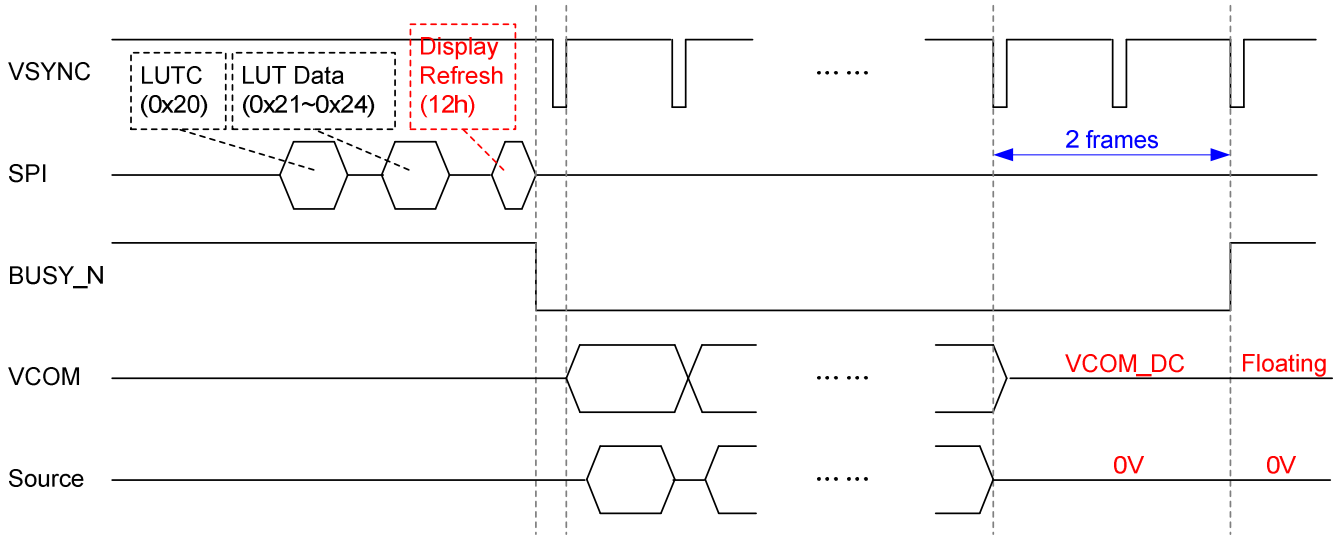
1. While level selection in LUT (LUTC only) is “1111_1111b”, all frame number are not ‘0’ and repeat times are not ‘0’, the driver will float VCOM.
2. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=1.
3. Meet the state whose Times to Repeat =0 and VCEND=1.
4. Meet the state whose all Number of Frames =0 and VCEND=1.



Display Refresh Waveform

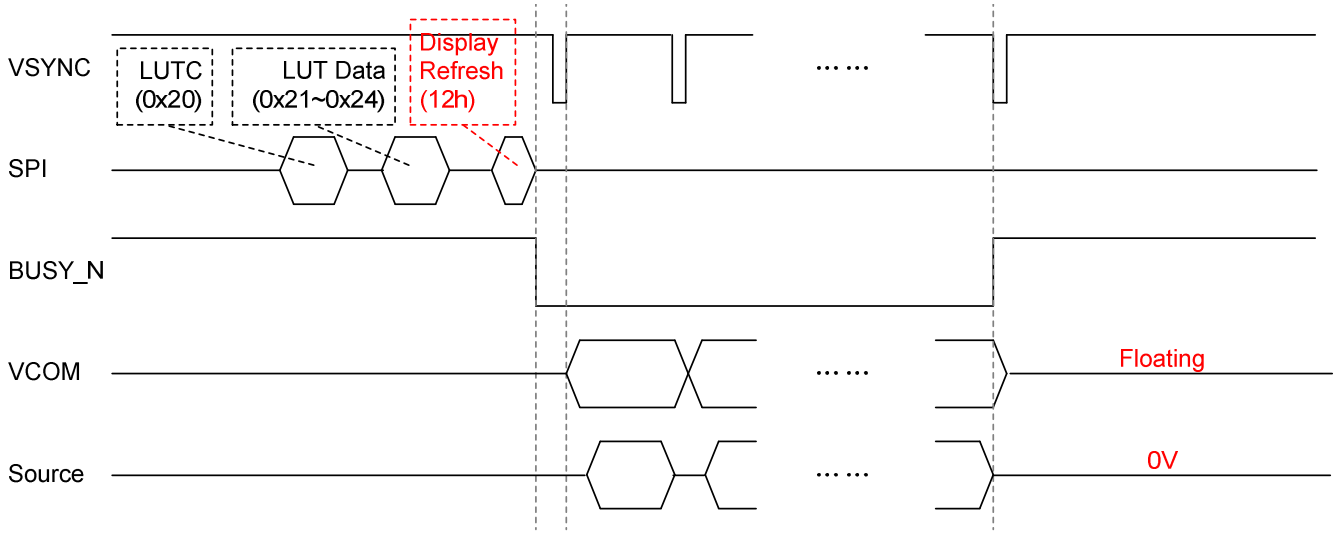
Example 1: After 3 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

1. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=0.
2. Meet the state whose Times to Repeat =0 and VCEND=0
3. Meet the state whose all Number of Frames =0 and VCEND=0



Example2: After 4 cases, the VCOM driver will send 2 frame VCOM_DC and then floating; and source drivers output 0V.

1. While level selection in LUT (LUTC only) is “1111_1111b”, all frame number are not ‘0’ and repeat times are not ‘0’, the driver will float VCOM.
2. All 7 LUT states (KW mode) or 10 LUT states (KWR mode) complete and VCEND=1.
3. Meet the state whose Times to Repeat =0 and VCEND=1.
4. Meet the state whose all Number of Frames =0 and VCEND=1.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
LUTC	X	No action
LUTWW	X	No action
LUTWB/LUTW	X	No action
LUTKW/LUTR	X	No action
LUTKK/LUTK	X	No action
LUTOPT	X	No action
KWOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
TSW	X	No action
TSR	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
EVS	X	No action
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action

V: Accepted, X: Ignored

OTP ADDRESS MAPPING

The size of the internal One Time Programmable (OTP) memory is 6K bytes, and the address is from 0x000 to 0x17FF. The unprogrammed bit is logic 1. Only the bit at logic 1 can be programmed to logic 0, but the bit at logic 0 can't be converted to logic 1.

There are 2 areas (0x0BDD~0x0BFF, 0x17DD~0x17FF) reserved for UltraChip only. Write all 0xFF of data to skip the 2 areas. The recommended voltage of VPP during programming is 7.75V. In conditions other than programming, let VPP float or be connected to GND. The maximum current of VPP during programming is 5mA.

There are 2 banks in the internal OTP, and each bank has 3K bytes storage memory. The formats of each bank are the same, and the selection of bank is controlled by Check Code (0x0000 and 0x0C00). The 2 banks are used for two times programming.

Table 1: OTP Address Map

Bank0		Bank1	
Address	Content	Address	Content
0x0000	Check Code (0xA5)	0x0C00	Check Code (0xA5)
0x0001	LUT Version	0x0C01	LUT Version
0x0002	Temperature Boundary 0 (TB0)	0x0C02	Temperature Boundary 0 (TB0)
0x0003	Temperature Boundary 1 (TB1)	0x0C03	Temperature Boundary 1 (TB1)
0x0004	Temperature Boundary 2 (TB2)	0x0C04	Temperature Boundary 2 (TB2)
0x0005	Temperature Boundary 3 (TB3)	0x0C05	Temperature Boundary 3 (TB3)
0x0006	Temperature Boundary 4 (TB4)	0x0C06	Temperature Boundary 4 (TB4)
0x0007	Temperature Boundary 5 (TB5)	0x0C07	Temperature Boundary 5 (TB5)
0x0008	Temperature Boundary 6 (TB6)	0x0C08	Temperature Boundary 6 (TB6)
0x0009	Temperature Boundary 7 (TB7)	0x0C09	Temperature Boundary 7 (TB7)
0x000A	Temperature Boundary 8 (TB8)	0x0C0A	Temperature Boundary 8 (TB8)
0x000B	Temperature Boundary 9 (TB9)	0x0C0B	Temperature Boundary 9 (TB9)
0x000C	Temperature Boundary 10 (TB10)	0x0C0C	Temperature Boundary 10 (TB10)
0x000D~0x001E	Command Defatult Setting (Note 1)	0x0C0D~0x0C1E	Command Defatult Setting (Note 1)
0x001F~0x0048	Border LUT	0x0C1F~0x0C48	Border LUT
0x0049~0x013F	TR0 (Note 2)	0x0C49~0x0D3F	TR0 (Note 2)
0x0140~0x0236	TR1 (Note 2)	0x0D40~0x0E36	TR1 (Note 2)
0x0237~0x032D	TR2 (Note 2)	0x0E37~0x0F2D	TR2 (Note 2)
0x032E~0x0424	TR3 (Note 2)	0x0F2E~0x1024	TR3 (Note 2)
0x0425~0x051B	TR4 (Note 2)	0x1025~0x111B	TR4 (Note 2)
0x051C~0x0612	TR5 (Note 2)	0x111C~0x1212	TR5 (Note 2)
0x0613~0x0709	TR6 (Note 2)	0x1213~0x1309	TR6 (Note 2)
0x070A~0x0800	TR7 (Note 2)	0x130A~0x1400	TR7 (Note 2)
0x0801~0x08F7	TR8 (Note 2)	0x1401~0x14F7	TR8 (Note 2)
0x08F8~0x09EE	TR9 (Note 2)	0x14F8~0x15EE	TR9 (Note 2)
0x09EF~0x0AE5	TR10 (Note 2)	0x15EF~0x16E5	TR10 (Note 2)
0x0AE6~0x0BDC	TR11 (Note 2)	0x16E6~0x17DC	TR11 (Note 2)
0x0BDD~0x0BEF	Blank (Note 3)	0x17DD~0x17FF	Blank (Note 3)
0x0BF0~0x0BFF	Reserved (Note 3)	--	--

Note:

(1) See section "COMMAND DEFAULT SETTING" for more detail.

(2) See section "LUT FORMAT IN OTP" for more detail.

(3) "Blank" is available for user, and "Reserved" is for UltraChip's definition.

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 11 temperature boundary settings (TBx) to determine 12 temperature ranges. The sequence of mechanism is from TB0 to TB10, as shown below. If less than 12 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x0000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1. Read 0x0C00	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x0002 / 0x0C02	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x0003 / 0x0C03	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x0004 / 0x0C04	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x0005 / 0x0C05	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x0006 / 0x0C06	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x0007 / 0x0C07	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x0008 / 0x0C08	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x0009 / 0x0C09	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x000A / 0x0C0A	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Read 0x000B / 0x0C0B	Real Temperature ≦ TB9	Use TR9's table & setting, exit
12. Read 0x000C / 0x0C0C	Real Temperature ≦ TB10	Use TR10's table & setting, exit
13. Other	Real Temperature > TB10	Use TR11's table & setting, finish

Note: TRx's content is defined in "LUT FORMAT IN OTP" section.

Example:

If temperature = -20 ºC, TR0 is selected.

If temperature = -10 ºC, TR1 is selected.

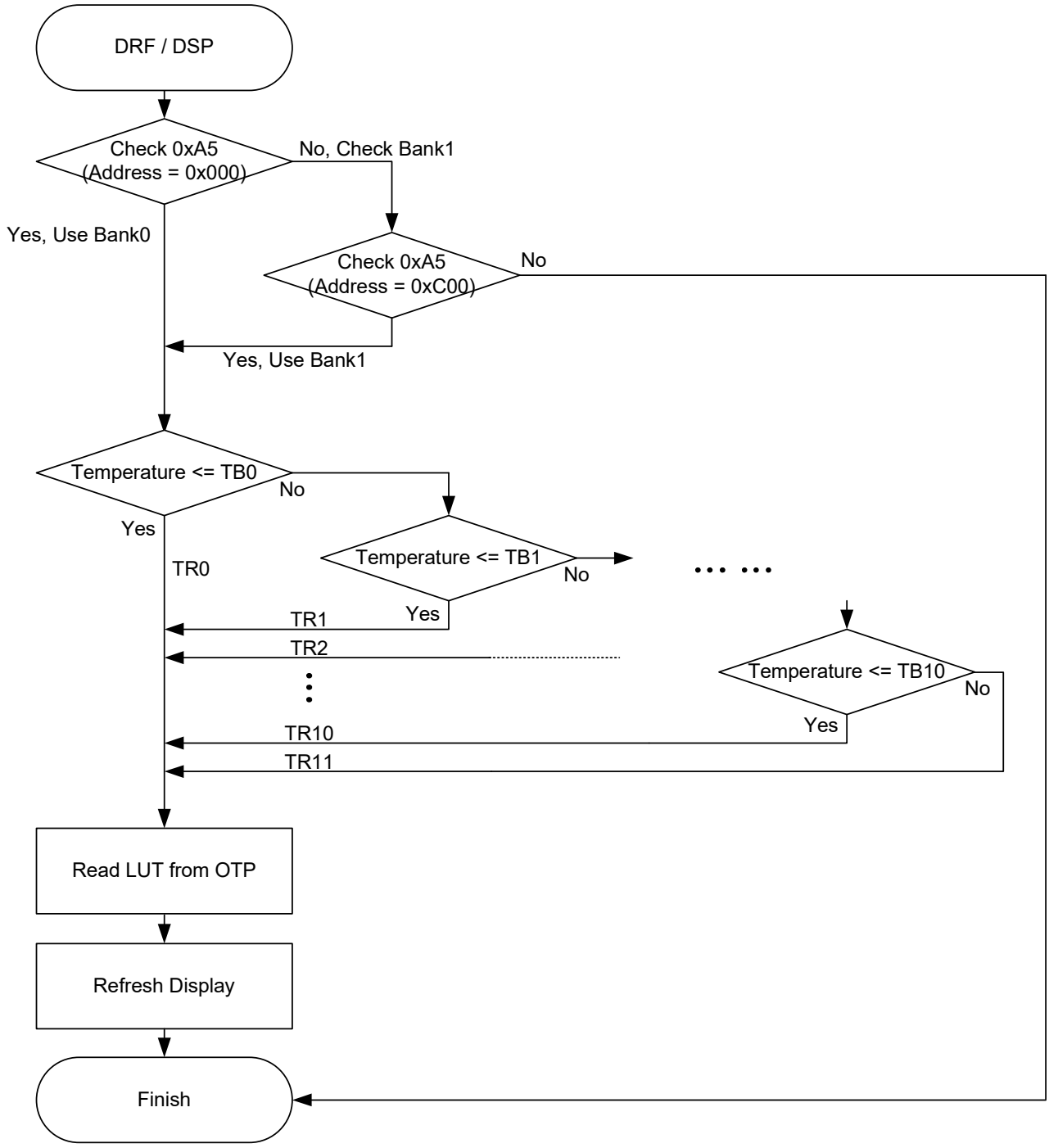
If temperature = 0 ºC, TR2 is selected.

If temperature = 20 ºC, TR4 is selected.

If temperature = 40 ºC, TR5 is selected.

If temperature > 40 ºC, TR5 is selected.

OTP Address	Content	
002h	0xF1	(-15 ºC)
003h	0xFB	(-5 ºC)
004h	0x00	(0 ºC)
005h	0x0A	(10 ºC)
006h	0x1E	(30 ºC)
007h	0x7F	-



Temperature Selection Mechanism

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x000D~0x001E (or 0x0C0D~0x0C1E). The data of address 0x000D (or 0x0C0D) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x000D	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x000E	--	--	#	#	#	#	--	--	PSR	REG, KW/R, UD, SHL	0x0F
0x000F	--	--	#	#	--	--	--	--	PFS	T_VDS_OFF[1:0]	0x00
0x0010	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x0011	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x0012	--	--	#	#	#	#	#	#		BT_PHC[5:0]	0x17
0x0013	--	--	--	--	--	--	#	#	KWOPT	ATRED, NORED	0x00
0x0014	#	--	#	#	#	--	#	#	CDI	BDZ, BDV[1:0], N2OCP, DDX[1:0]	0x31
0x0015	--	--	--	--	#	#	#	#		CDI[3:0]	0x07
0x0016	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x0017	#	#	#	#	#	0	0	0	TRES	HRES[7:3]	0xF0
0x0018	--	--	--	--	--	--	#	#		VRES[9:0]	0x02
0x0019	#	#	#	#	#	#	#	#			0x00
0x001A	#	#	#	#	#	0	0	0	GSST	HST[7:3]	0x00
0x001B	--	--	--	--	--	--	--	#		VST[8:0]	0x00
0x001C	#	#	#	#	#	#	#	#			0x00
0x001D	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x001E	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03

LUT FORMAT IN OTP

There are 12 TRs (temperature range) in a bank. Each TR has independant frame rate, voltage, XON settings, KW option enable setting and LUTs. The fomat of LUT is different in different mode. In KWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTK in TRs. LUTC, LUTR, LUTW and LUTK have 10 states. In KW mode, there are 5 LUTs including LUT, LUTWW, LUTKW, LUTWB and LUTKK in TRs. All LUTs have 7 states. Besides, there is 1 common border LUT, regardless of temperature range, in KWR mode or KW mode.

Common Border LUT Table

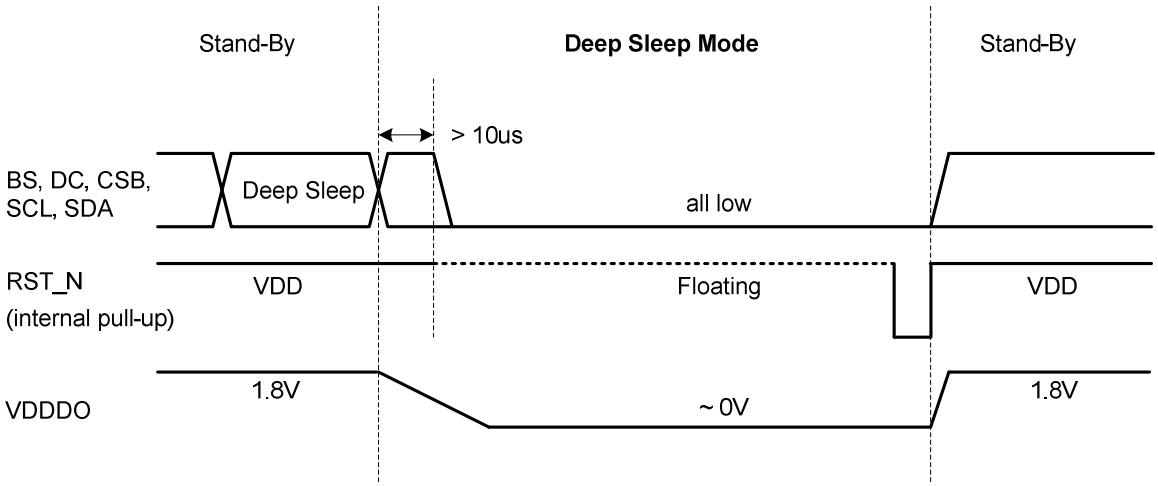
Common Border LUT Table	KWR Mode or KW Mode	
	Address (Bank0 / Bank1)	Content
	0x001F ~ 0x0048 / 0x0C1F ~ 0x0C48	LUTBD

Separate VCOM LUT and Source LUT (Example: Bank0 / TR0)

	KWR Mode (KW/R=0)		KW Mode (KW/R=1)	
	Address	Content	Address	Content
TR0	0x0049	Frame Rate[3:0], VCOM_HV, VG Voltage[2:0]	0x0049	Frame Rate[3:0],VCOM_HV,VG Voltage[2:0]
	0x004A	0b, VCEND, VDH Voltage[5:0]	0x004A	0b, VCEND, VDH Voltage[5:0]
	0x004B	BDEND[1:0], VDL Voltage [5:0]	0x004B	BDEND[1:0], VDL Voltage [5:0]
	0x004C	XON[9:8], VDHR Voltage [5:0]	0x004C	XON[9:8], VDHR Voltage [5:0]
	0x004D	XON [7:0]	0x004D	XON [7:0]
	0x004E	KWE[9:8], VCOM_DC[5:0]	0x004E	00b, VCOM_DC[5:0]
	0x004F	KWE[7:0]	0x004F | 0x0078	LUTC (7 states)
	0x0050 | 0x008B	LUTC (10 states)	0x0079 | 0x00A2	LUTWW (7 states)
	0x008C | 0x00C7	LUTR (10 states)	0x00A3 | 0x00CC	LUTKW (7 states)
	0x00C8 | 0x0103	LUTW (10 states)	0x00CD | 0x00F6	LUTWK (7 states)
	0x0104 | 0x013F	LUTK (10 states)	0x00F7 | 0x0120	LUTKK (7 states)
			0x0121 | 0x013F	Reserved

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, UC8171 enter “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

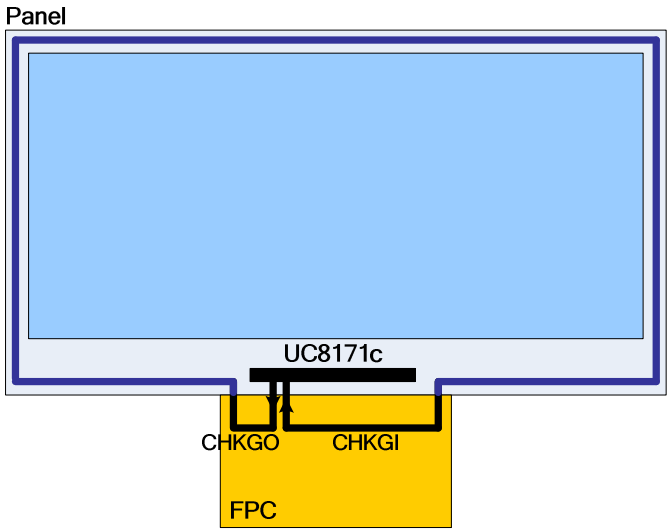


Figure: Panel break check layout example

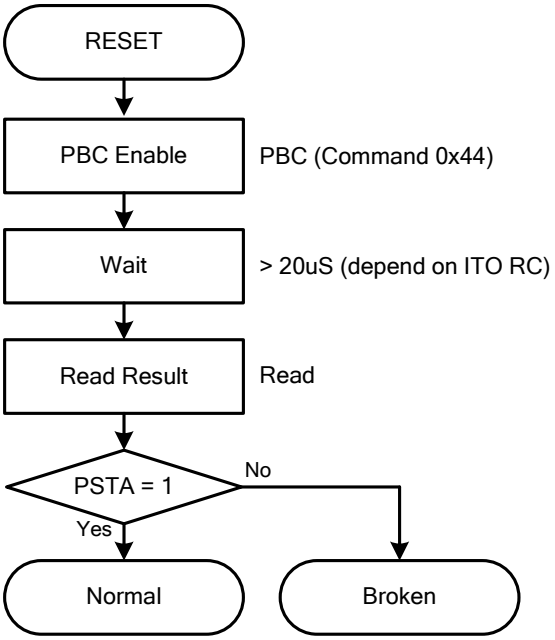
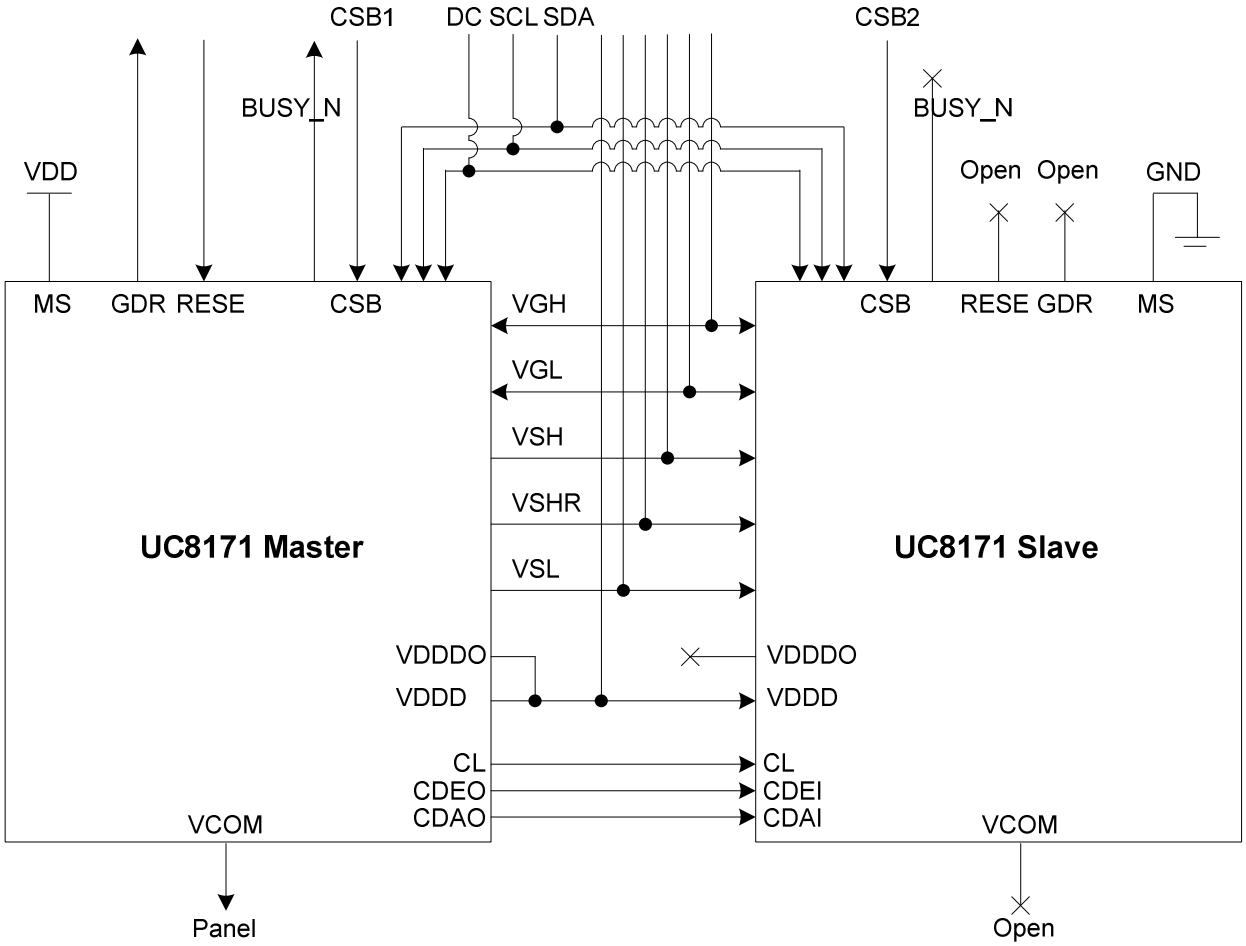


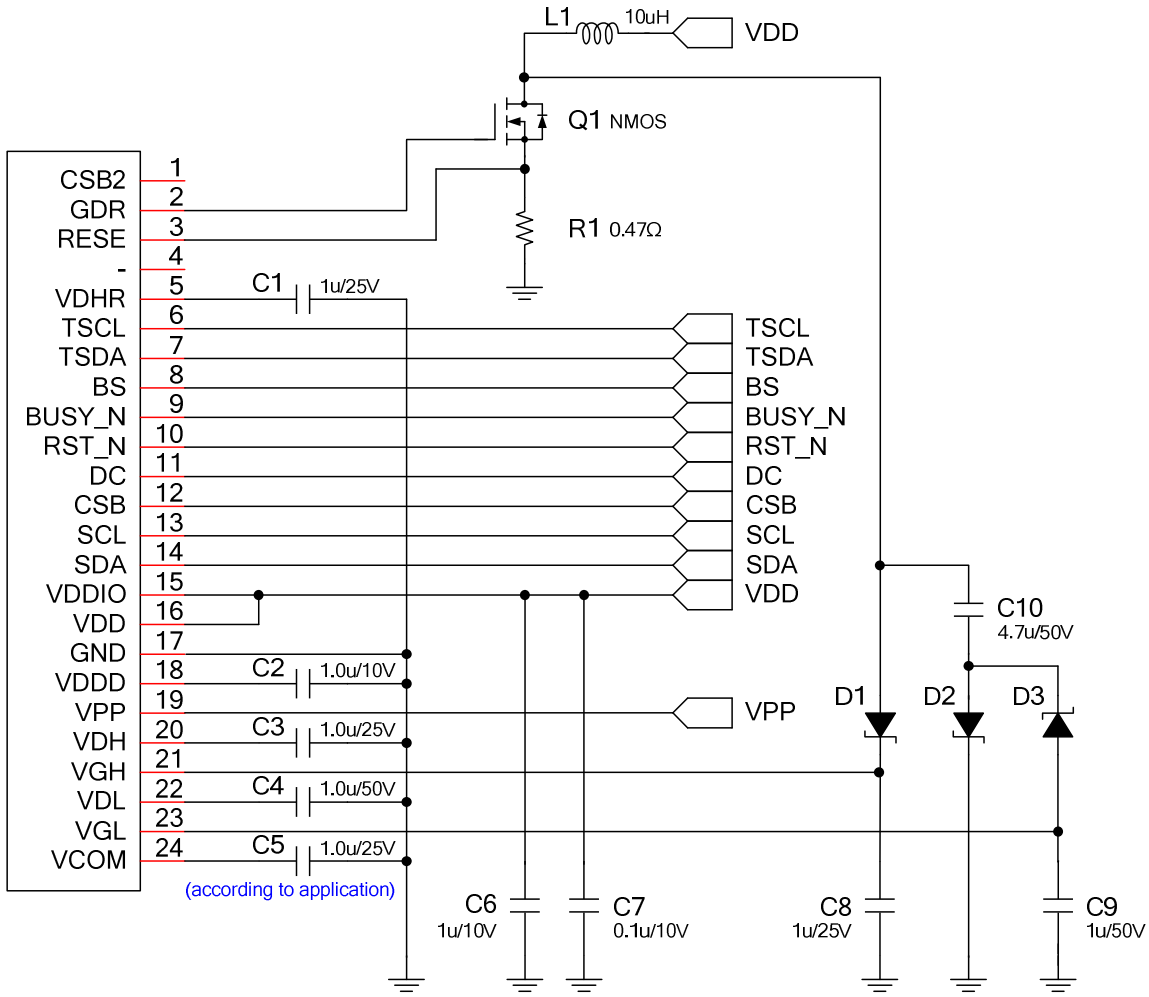
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT

All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.



BOOSTER APPLICATION CIRCUIT



Note:

1. The capacitor value of VGH/VGL must be equal or more than the one of VSH/VSL/VDHR.

Recommended Device

1. Switch MOS NMOS: Vishay Si1308EDL (V_{DS} > 25V, I_D > 500mA, V_{GS}(th) < 1.5V, C_{ISS} < 200pF, R_{DS}(on) < 400mΩ)
2. Schottky Diode: OnSemi MBR0530 (V_R > 25V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_A=100°C)

Recommended Resistor

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 10 Ω
Boosters	VGL, VGH, GDR, RESE	< 10 Ω
Regulators	VDH, VDL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, GDR, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{DDIO}, V_{DDA}	Logic Supply voltage	-0.3	+6.0	V
V_{PP}	OTP programming voltage	-0.3	+8.0	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VGH-VGL	Supply range	-	+44.0	V
Source				
VDH	Analog supply voltage – positive	+16		V
VDL	Analog supply voltage -- negative	-16		V
VDHR	Analog supply voltage – positive	+16		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+22	V
VGL	Analog supply voltage -- negative	-22	0.3	V
T_{STG}	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400uA	VDDIO-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85*	°C
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		40	V
dVDH	Supply voltage dev		-200	0	+200	mV
dVDL	Supply voltage dev		-200	0	+200	mV
dVDHR	Supply voltage dev		-200	0	+200	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
RON	Driver Output Resistance	For source driver, TOP=25°C, VOUT = ±15V		16.0	38.4	KΩ
		For gate driver, TOP=25°C, VOUT = ±20V		4.0	8	

*While IC operating is at 85C, the accuracy of temp.sensing is +/-5C

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
IVDD	Digital deep sleep current	VDDD OFF	--	0.3	0.5	uA
	Digital stand-by current	All stopped	--	8.2	10.0	uA
	Digital operating current		--	--	0.1	mA
IVDDIO	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.3	mA
IVDDA	DCDC deep sleep current	VDDD OFF	--	0.1	0.3	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VDH/VDL, Duty=0.5, Period =126us VCOM DC No load	--	--	5.0	mA
		Source output VDH/VDL, Duty=0.5, Period =126us, VCOM DC External cap: 415pF, NMOS=340pF	--	--	20.0	

AC CHARACTERISTICS

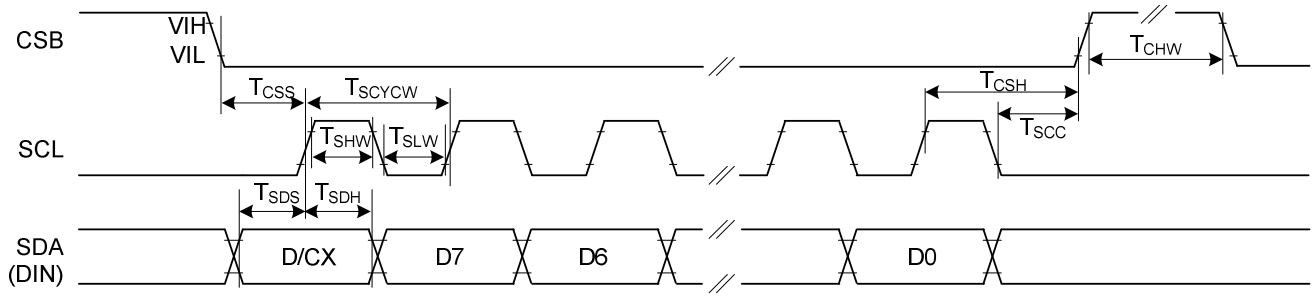


Figure: 3-wire Serial Interface Characteristics (Write mode)

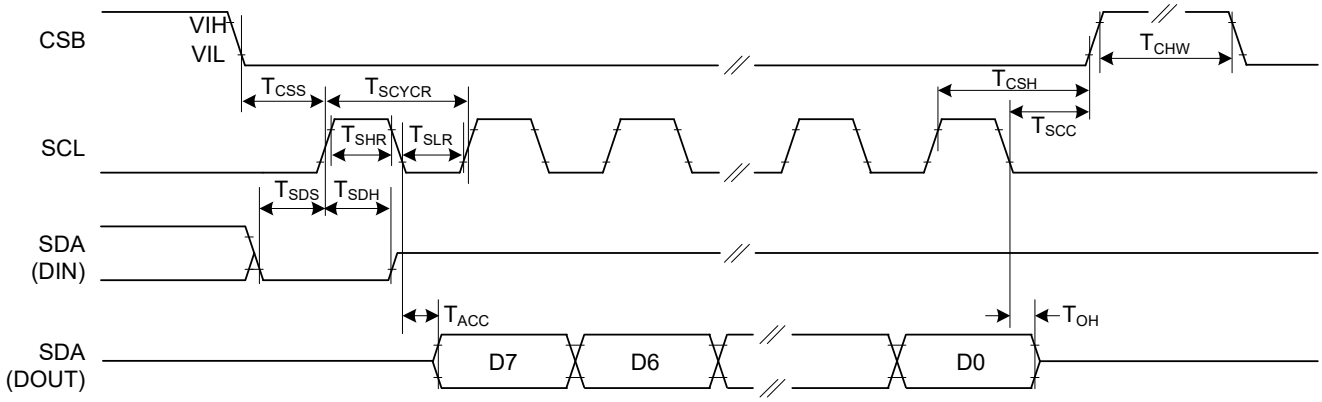


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL “H” pulse width (Read)	175			ns
T_{SLR}		SCL “L” pulse width (Read)	175			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			350	ns
T_{OH}		Output disable time	15			ns

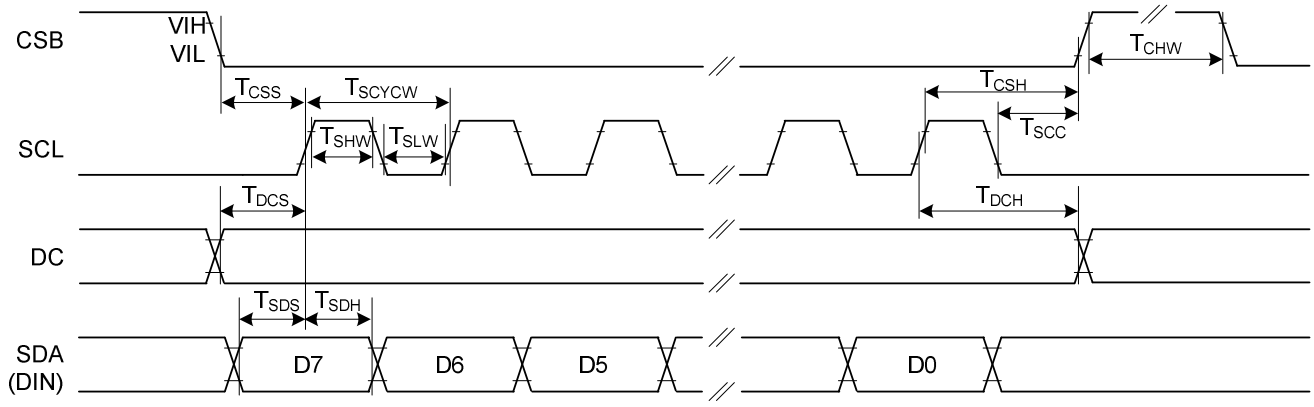


Figure: 4-wire Serial Interface Characteristics (Write mode)

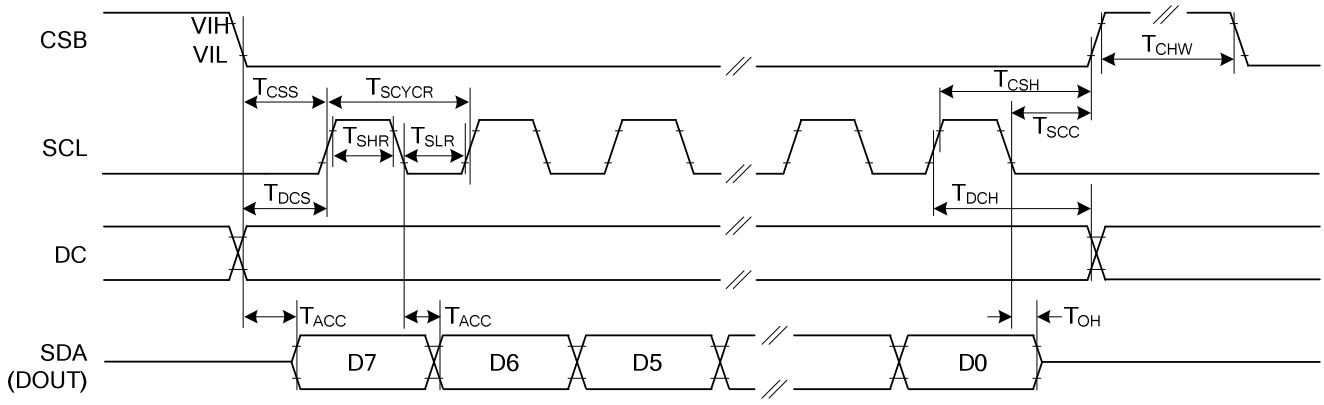
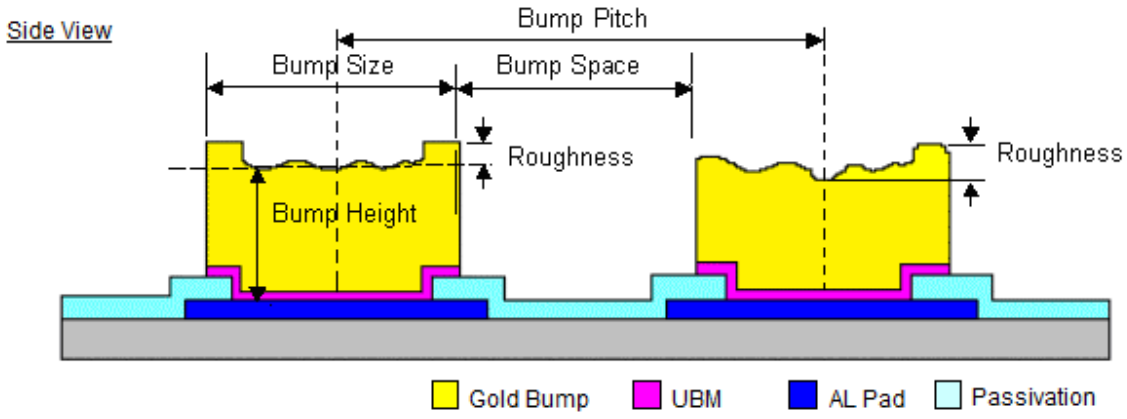


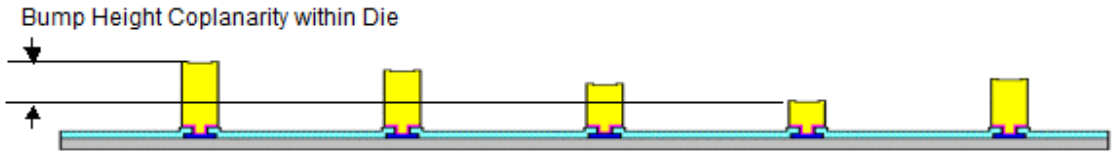
Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL “H” pulse width (Read)	175			ns
T_{SLR}		SCL “L” pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			350	ns
T_{OH}		Output disable time	15			ns

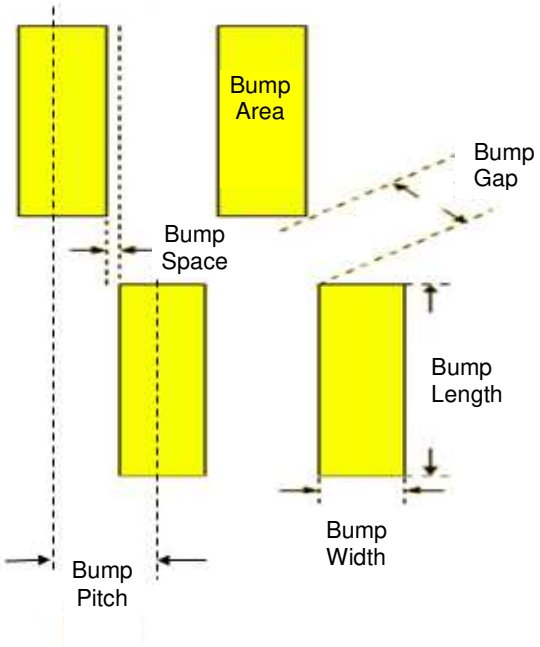
PHYSICAL DIMENSIONS

Die Size:	(11130 µM ± 40µM) x (1190 µM ± 40µM)
Die Thickness:	300 µM ± 20µM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2µM
Bump Height:	15 µM ± 3µM
	(H_{MAX} – H_{MIN}) within die ≤ 2µM
Bump Size:	16 µM x 75 µM ± 2µM
Bump Area:	1200 µM^2
Bump Pitch:	14 µM (output bump)
Bump Space:	0 µM (2uM stagger-overlapped)
Hardness:	65 Hv ± 15Hv
Shear:	/ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center



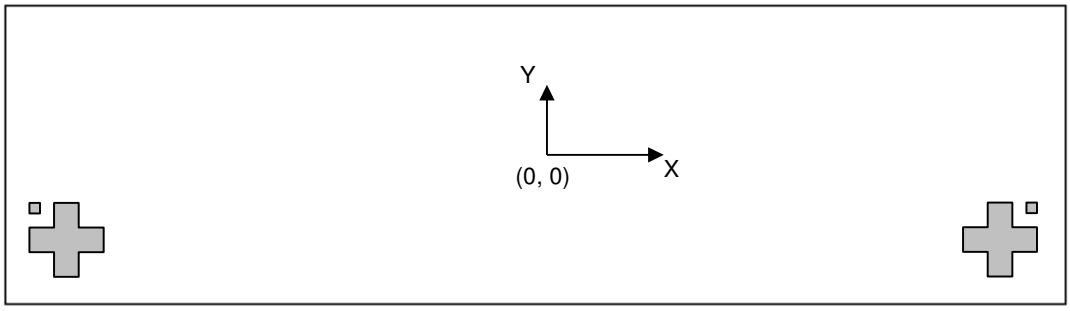


For Stagger Layout



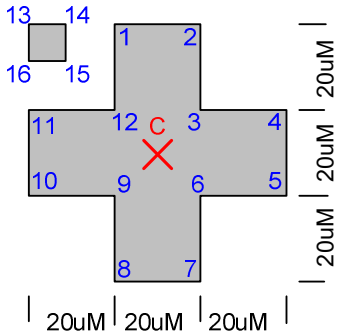
ALIGNMENT MARK INFORMATION

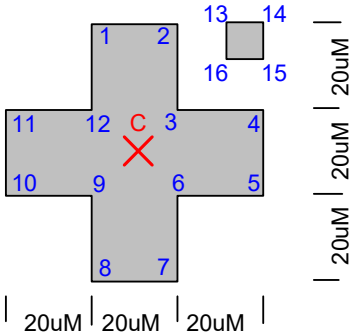
Location:



D-Left Mark D-Right Mark

Shapes and Points:





Point Coordinates:

Point	D-Left Mark		D-Right Mark	
	X	Y	X	Y
C (X)	-5440	-320	5440	-320
1	-5450	-290	5430	-290
2	-5430	-290	5450	-290
3	-5430	-310	5450	-310
4	-5410	-310	5470	-310
5	-5410	-330	5470	-330
6	-5430	-330	5450	-330
7	-5430	-350	5450	-350
8	-5450	-350	5430	-350
9	-5450	-330	5430	-330
10	-5470	-330	5410	-330
11	-5470	-310	5410	-310
12	-5450	-310	5430	-310
13	-5470	-290	5460	-290
14	-5460	-290	5470	-290
15	-5460	-300	5470	-300
16	-5470	-300	5460	-300

PAD COORDINATES

#	Pad	X	Y	W	H
1	NC	-5474	-503	28	70
2	VCOM	-5428	-503	28	70
3	VCOM	-5382	-503	28	70
4	VCOM	-5336	-503	28	70
5	VCOM	-5290	-503	28	70
6	VCOM	-5244	-503	28	70
7	VCOM	-5198	-503	28	70
8	VCOM	-5152	-503	28	70
9	VCOM	-5106	-503	28	70
10	VDM	-5060	-503	28	70
11	VDM	-5014	-503	28	70
12	VGL	-4968	-503	28	70
13	VGL	-4922	-503	28	70
14	VGL	-4876	-503	28	70
15	VGL	-4830	-503	28	70
16	VGL	-4784	-503	28	70
17	VGL	-4738	-503	28	70
18	VGL	-4692	-503	28	70
19	VGL	-4646	-503	28	70
20	VGL	-4600	-503	28	70
21	VGL	-4554	-503	28	70
22	VGL	-4508	-503	28	70
23	GNDA	-4462	-503	28	70
24	VDL	-4416	-503	28	70
25	VDL	-4370	-503	28	70
26	VDL	-4324	-503	28	70
27	VDL	-4278	-503	28	70
28	VDL	-4232	-503	28	70
29	VDL	-4186	-503	28	70
30	VDL	-4140	-503	28	70
31	VDL	-4094	-503	28	70
32	VDL	-4048	-503	28	70
33	GNDA	-4002	-503	28	70
34	VGH	-3956	-503	28	70
35	VGH	-3910	-503	28	70
36	VGH	-3864	-503	28	70
37	VGH	-3818	-503	28	70
38	VGH	-3772	-503	28	70
39	VGH	-3726	-503	28	70
40	VGH	-3680	-503	28	70
41	VGH	-3634	-503	28	70
42	VGH	-3588	-503	28	70
43	VGH	-3542	-503	28	70
44	VGH	-3496	-503	28	70
45	GNDA	-3450	-503	28	70
46	VDH	-3404	-503	28	70
47	VDH	-3358	-503	28	70
48	VDH	-3312	-503	28	70
49	VDH	-3266	-503	28	70
50	VDH	-3220	-503	28	70
51	VDH	-3174	-503	28	70
52	VDH	-3128	-503	28	70
53	VDH	-3082	-503	28	70
54	VDH	-3036	-503	28	70
55	GNDA	-2990	-503	28	70
56	VPP	-2944	-503	28	70
57	VPP	-2898	-503	28	70
58	VPP	-2852	-503	28	70
59	VPP	-2806	-503	28	70

#	Pad	X	Y	W	H
60	VPP	-2760	-503	28	70
61	VPP	-2714	-503	28	70
62	VPP	-2668	-503	28	70
63	VDDDO	-2622	-503	28	70
64	VDDDO	-2576	-503	28	70
65	VDDDO	-2530	-503	28	70
66	VDDDO	-2484	-503	28	70
67	VDDDO	-2438	-503	28	70
68	VDDDI	-2392	-503	28	70
69	VDDDI	-2346	-503	28	70
70	VDDDI	-2300	-503	28	70
71	VDDDI	-2254	-503	28	70
72	VDDDI	-2208	-503	28	70
73	VDM	-2162	-503	28	70
74	VDM	-2116	-503	28	70
75	GNDA	-2070	-503	28	70
76	GNDA	-2024	-503	28	70
77	GNDA	-1978	-503	28	70
78	GNDA	-1932	-503	28	70
79	GNDA	-1886	-503	28	70
80	GNDA	-1840	-503	28	70
81	GNDA	-1794	-503	28	70
82	GNDA	-1748	-503	28	70
83	GNDA	-1702	-503	28	70
84	GNDA	-1656	-503	28	70
85	GND	-1610	-503	28	70
86	GND	-1564	-503	28	70
87	GND	-1518	-503	28	70
88	GND	-1472	-503	28	70
89	GND	-1426	-503	28	70
90	GND	-1380	-503	28	70
91	GND	-1334	-503	28	70
92	GND	-1288	-503	28	70
93	GND	-1242	-503	28	70
94	GND	-1196	-503	28	70
95	GND	-1150	-503	28	70
96	GND	-1104	-503	28	70
97	VDDA	-1058	-503	28	70
98	VDDA	-1012	-503	28	70
99	VDDA	-966	-503	28	70
100	VDDA	-920	-503	28	70
101	VDDA	-874	-503	28	70
102	VDDA	-828	-503	28	70
103	VDDA	-782	-503	28	70
104	VDDA	-736	-503	28	70
105	VDDA	-690	-503	28	70
106	VDDA	-644	-503	28	70
107	VDD	-598	-503	28	70
108	VDD	-552	-503	28	70
109	VDD	-506	-503	28	70
110	VDD	-460	-503	28	70
111	VDD	-414	-503	28	70
112	VDD	-368	-503	28	70
113	VDD	-322	-503	28	70
114	VDDIO	-276	-503	28	70
115	VDDIO	-230	-503	28	70
116	VDDIO	-184	-503	28	70
117	VDDIO	-138	-503	28	70
118	DUMMY	-92	-503	28	70

#	Pad	X	Y	W	H
119	TEST1	-46	-503	28	70
120	TEST2	0	-503	28	70
121	TEST3	46	-503	28	70
122	VSYNC	92	-503	28	70
123	CL	138	-503	28	70
124	CDEO	184	-503	28	70
125	DUMMY	230	-503	28	70
126	DUMMY	276	-503	28	70
127	DUMMY	322	-503	28	70
128	CDAO	368	-503	28	70
129	DUMMY	414	-503	28	70
130	DUMMY	460	-503	28	70
131	CHKGI	506	-503	28	70
132	DUMMY	552	-503	28	70
133	DUMMY	598	-503	28	70
134	SDA	644	-503	28	70
135	DUMMY	690	-503	28	70
136	DUMMY	736	-503	28	70
137	SCL	782	-503	28	70
138	GND	828	-503	28	70
139	CSB	874	-503	28	70
140	VDDIO	920	-503	28	70
141	GND	966	-503	28	70
142	DC	1012	-503	28	70
143	VDDIO	1058	-503	28	70
144	RST_N	1104	-503	28	70
145	DUMMY	1150	-503	28	70
146	DUMMY	1196	-503	28	70
147	DUMMY	1242	-503	28	70
148	BUSY_N	1288	-503	28	70
149	DUMMY	1334	-503	28	70
150	GND	1380	-503	28	70
151	BS	1426	-503	28	70
152	VDDIO	1472	-503	28	70
153	MS	1518	-503	28	70
154	GND	1564	-503	28	70
155	GND	1610	-503	28	70
156	TSDA	1656	-503	28	70
157	TSDA	1702	-503	28	70
158	TSCL	1748	-503	28	70
159	TSCL	1794	-503	28	70
160	GND	1840	-503	28	70
161	GND	1886	-503	28	70
162	CHKGO	1932	-503	28	70
163	GND	1978	-503	28	70
164	GND	2024	-503	28	70
165	CDAI	2070	-503	28	70
166	CDEI	2116	-503	28	70
167	DUMMY	2162	-503	28	70
168	DUMMY	2208	-503	28	70
169	DUMMY	2254	-503	28	70
170	CL	2300	-503	28	70
171	DUMMY	2346	-503	28	70
172	VSYNC	2392	-503	28	70
173	DUMMY	2438	-503	28	70
174	DUMMY	2484	-503	28	70
175	DUMMY	2530	-503	28	70
176	TEST4	2576	-503	28	70
177	TEST5	2622	-503	28	70

#	Pad	X	Y	W	H
178	DUMMY	2668	-503	28	70
179	GND	2714	-503	28	70
180	DUMMY	2760	-503	28	70
181	TEST6	2806	-503	28	70
182	TEST7	2852	-503	28	70
183	GND	2898	-503	28	70
184	DUMMY	2944	-503	28	70
185	GND	2990	-503	28	70
186	TEST8	3036	-503	28	70
187	TEST9	3082	-503	28	70
188	DUMMY	3128	-503	28	70
189	GND	3174	-503	28	70
190	TEST10	3220	-503	28	70
191	DUMMY	3266	-503	28	70
192	TEST11	3312	-503	28	70
193	DUMMY	3358	-503	28	70
194	DUMMY	3404	-503	28	70
195	TEST12	3450	-503	28	70
196	DUMMY	3496	-503	28	70
197	TEST13	3542	-503	28	70
198	DUMMY	3588	-503	28	70
199	DUMMY	3634	-503	28	70
200	VDHR	3680	-503	28	70
201	VDHR	3726	-503	28	70
202	VDHR	3772	-503	28	70
203	VDHR	3818	-503	28	70
204	VDHR	3864	-503	28	70
205	VDHR	3910	-503	28	70
206	VDHR	3956	-503	28	70
207	VDHR	4002	-503	28	70
208	DUMMY	4048	-503	28	70
209	DUMMY	4094	-503	28	70
210	DUMMY	4140	-503	28	70
211	DUMMY	4186	-503	28	70
212	DUMMY	4232	-503	28	70
213	DUMMY	4278	-503	28	70
214	GNDA	4324	-503	28	70
215	FB	4370	-503	28	70
216	FB	4416	-503	28	70
217	GNDA	4462	-503	28	70
218	RESE	4508	-503	28	70
219	RESE	4554	-503	28	70
220	GNDA	4600	-503	28	70
221	GDR	4646	-503	28	70
222	GDR	4692	-503	28	70
223	GDR	4738	-503	28	70
224	GDR	4784	-503	28	70
225	GDR	4830	-503	28	70
226	GDR	4876	-503	28	70
227	GDR	4922	-503	28	70
228	GDR	4968	-503	28	70
229	VDM	5014	-503	28	70
230	VDM	5060	-503	28	70
231	VCOM	5106	-503	28	70
232	VCOM	5152	-503	28	70
233	VCOM	5198	-503	28	70
234	VCOM	5244	-503	28	70
235	VCOM	5290	-503	28	70
236	VCOM	5336	-503	28	70

#	Pad	X	Y	W	H
237	VCOM	5382	-503	28	70
238	VCOM	5428	-503	28	70
239	NC	5474	-503	28	70
240	NC	5453	518.5	16	75
241	GD<0>	5439	418.5	16	75
242	G<0>	5425	518.5	16	75
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246	G<8>	5369	518.5	16	75
247	G<10>	5355	418.5	16	75
248	G<12>	5341	518.5	16	75
249	G<14>	5327	418.5	16	75
250	G<16>	5313	518.5	16	75
251	G<18>	5299	418.5	16	75
252	G<20>	5285	518.5	16	75
253	G<22>	5271	418.5	16	75
254	G<24>	5257	518.5	16	75
255	G<26>	5243	418.5	16	75
256	G<28>	5229	518.5	16	75
257	G<30>	5215	418.5	16	75
258	G<32>	5201	518.5	16	75
259	G<34>	5187	418.5	16	75
260	G<36>	5173	518.5	16	75
261	G<38>	5159	418.5	16	75
262	G<40>	5145	518.5	16	75
263	G<42>	5131	418.5	16	75
264	G<44>	5117	518.5	16	75
265	G<46>	5103	418.5	16	75
266	G<48>	5089	518.5	16	75
267	G<50>	5075	418.5	16	75
268	G<52>	5061	518.5	16	75
269	G<54>	5047	418.5	16	75
270	G<56>	5033	518.5	16	75
271	G<58>	5019	418.5	16	75
272	G<60>	5005	518.5	16	75
273	G<62>	4991	418.5	16	75
274	G<64>	4977	518.5	16	75
275	G<66>	4963	418.5	16	75
276	G<68>	4949	518.5	16	75
277	G<70>	4935	418.5	16	75
278	G<72>	4921	518.5	16	75
279	G<74>	4907	418.5	16	75
280	G<76>	4893	518.5	16	75
281	G<78>	4879	418.5	16	75
282	G<80>	4865	518.5	16	75
283	G<82>	4851	418.5	16	75
284	G<84>	4837	518.5	16	75
285	G<86>	4823	418.5	16	75
286	G<88>	4809	518.5	16	75
287	G<90>	4795	418.5	16	75
288	G<92>	4781	518.5	16	75
289	G<94>	4767	418.5	16	75
290	G<96>	4753	518.5	16	75
291	G<98>	4739	418.5	16	75
292	G<100>	4725	518.5	16	75
293	G<102>	4711	418.5	16	75
294	G<104>	4697	518.5	16	75
295	G<106>	4683	418.5	16	75

#	Pad	X	Y	W	H
296	G<108>	4669	518.5	16	75
297	G<110>	4655	418.5	16	75
298	G<112>	4641	518.5	16	75
299	G<114>	4627	418.5	16	75
300	G<116>	4613	518.5	16	75
301	G<118>	4599	418.5	16	75
302	G<120>	4585	518.5	16	75
303	G<122>	4571	418.5	16	75
304	G<124>	4557	518.5	16	75
305	G<126>	4543	418.5	16	75
306	G<128>	4529	518.5	16	75
307	G<130>	4515	418.5	16	75
308	G<132>	4501	518.5	16	75
309	G<134>	4487	418.5	16	75
310	G<136>	4473	518.5	16	75
311	G<138>	4459	418.5	16	75
312	G<140>	4445	518.5	16	75
313	G<142>	4431	418.5	16	75
314	G<144>	4417	518.5	16	75
315	G<146>	4403	418.5	16	75
316	G<148>	4389	518.5	16	75
317	G<150>	4375	418.5	16	75
318	G<152>	4361	518.5	16	75
319	G<154>	4347	418.5	16	75
320	G<156>	4333	518.5	16	75
321	G<158>	4319	418.5	16	75
322	G<160>	4305	518.5	16	75
323	G<162>	4291	418.5	16	75
324	G<164>	4277	518.5	16	75
325	G<166>	4263	418.5	16	75
326	G<168>	4249	518.5	16	75
327	G<170>	4235	418.5	16	75
328	G<172>	4221	518.5	16	75
329	G<174>	4207	418.5	16	75
330	G<176>	4193	518.5	16	75
331	G<178>	4179	418.5	16	75
332	G<180>	4165	518.5	16	75
333	G<182>	4151	418.5	16	75
334	G<184>	4137	518.5	16	75
335	G<186>	4123	418.5	16	75
336	G<188>	4109	518.5	16	75
337	G<190>	4095	418.5	16	75
338	G<192>	4081	518.5	16	75
339	G<194>	4067	418.5	16	75
340	G<196>	4053	518.5	16	75
341	G<198>	4039	418.5	16	75
342	G<200>	4025	518.5	16	75
343	G<202>	4011	418.5	16	75
344	G<204>	3997	518.5	16	75
345	G<206>	3983	418.5	16	75
346	G<208>	3969	518.5	16	75
347	G<210>	3955	418.5	16	75
348	G<212>	3941	518.5	16	75
349	G<214>	3927	418.5	16	75
350	G<216>	3913	518.5	16	75
351	G<218>	3899	418.5	16	75
352	G<220>	3885	518.5	16	75
353	G<222>	3871	418.5	16	75
354	G<224>	3857	518.5	16	75

#	Pad	X	Y	W	H
355	G<226>	3843	418.5	16	75
356	G<228>	3829	518.5	16	75
357	G<230>	3815	418.5	16	75
358	G<232>	3801	518.5	16	75
359	G<234>	3787	418.5	16	75
360	G<236>	3773	518.5	16	75
361	G<238>	3759	418.5	16	75
362	G<240>	3745	518.5	16	75
363	G<242>	3731	418.5	16	75
364	G<244>	3717	518.5	16	75
365	G<246>	3703	418.5	16	75
366	G<248>	3689	518.5	16	75
367	G<250>	3675	418.5	16	75
368	G<252>	3661	518.5	16	75
369	G<254>	3647	418.5	16	75
370	G<256>	3633	518.5	16	75
371	G<258>	3619	418.5	16	75
372	G<260>	3605	518.5	16	75
373	G<262>	3591	418.5	16	75
374	G<264>	3577	518.5	16	75
375	G<266>	3563	418.5	16	75
376	G<268>	3549	518.5	16	75
377	G<270>	3535	418.5	16	75
378	G<272>	3521	518.5	16	75
379	G<274>	3507	418.5	16	75
380	G<276>	3493	518.5	16	75
381	G<278>	3479	418.5	16	75
382	G<280>	3465	518.5	16	75
383	G<282>	3451	418.5	16	75
384	G<284>	3437	518.5	16	75
385	G<286>	3423	418.5	16	75
386	G<288>	3409	518.5	16	75
387	G<290>	3395	418.5	16	75
388	G<292>	3381	518.5	16	75
389	G<294>	3367	418.5	16	75
390	G<296>	3353	518.5	16	75
391	G<298>	3339	418.5	16	75
392	G<300>	3325	518.5	16	75
393	G<302>	3311	418.5	16	75
394	G<304>	3297	518.5	16	75
395	G<306>	3283	418.5	16	75
396	G<308>	3269	518.5	16	75
397	G<310>	3255	418.5	16	75
398	G<312>	3241	518.5	16	75
399	G<314>	3227	418.5	16	75
400	G<316>	3213	518.5	16	75
401	G<318>	3199	418.5	16	75
402	G<320>	3185	518.5	16	75
403	G<322>	3171	418.5	16	75
404	G<324>	3157	518.5	16	75
405	G<326>	3143	418.5	16	75
406	G<328>	3129	518.5	16	75
407	G<330>	3115	418.5	16	75
408	G<332>	3101	518.5	16	75
409	G<334>	3087	418.5	16	75
410	G<336>	3073	518.5	16	75
411	G<338>	3059	418.5	16	75
412	G<340>	3045	518.5	16	75
413	G<342>	3031	418.5	16	75

#	Pad	X	Y	W	H
414	G<344>	3017	518.5	16	75
415	G<346>	3003	418.5	16	75
416	G<348>	2989	518.5	16	75
417	G<350>	2975	418.5	16	75
418	G<352>	2961	518.5	16	75
419	G<354>	2947	418.5	16	75
420	G<356>	2933	518.5	16	75
421	G<358>	2919	418.5	16	75
422	G<360>	2905	518.5	16	75
423	G<362>	2891	418.5	16	75
424	G<364>	2877	518.5	16	75
425	G<366>	2863	418.5	16	75
426	G<368>	2849	518.5	16	75
427	G<370>	2835	418.5	16	75
428	G<372>	2821	518.5	16	75
429	G<374>	2807	418.5	16	75
430	G<376>	2793	518.5	16	75
431	G<378>	2779	418.5	16	75
432	G<380>	2765	518.5	16	75
433	G<382>	2751	418.5	16	75
434	G<384>	2737	518.5	16	75
435	G<386>	2723	418.5	16	75
436	G<388>	2709	518.5	16	75
437	G<390>	2695	418.5	16	75
438	G<392>	2681	518.5	16	75
439	G<394>	2667	418.5	16	75
440	G<396>	2653	518.5	16	75
441	G<398>	2639	418.5	16	75
442	G<400>	2625	518.5	16	75
443	G<402>	2611	418.5	16	75
444	G<404>	2597	518.5	16	75
445	G<406>	2583	418.5	16	75
446	G<408>	2569	518.5	16	75
447	G<410>	2555	418.5	16	75
448	G<412>	2541	518.5	16	75
449	G<414>	2527	418.5	16	75
450	G<416>	2513	518.5	16	75
451	G<418>	2499	418.5	16	75
452	G<420>	2485	518.5	16	75
453	G<422>	2471	418.5	16	75
454	G<424>	2457	518.5	16	75
455	G<426>	2443	418.5	16	75
456	G<428>	2429	518.5	16	75
457	G<430>	2415	418.5	16	75
458	G<432>	2401	518.5	16	75
459	G<434>	2387	418.5	16	75
460	G<436>	2373	518.5	16	75
461	G<438>	2359	418.5	16	75
462	G<440>	2345	518.5	16	75
463	G<442>	2331	418.5	16	75
464	G<444>	2317	518.5	16	75
465	G<446>	2303	418.5	16	75
466	G<448>	2289	518.5	16	75
467	G<450>	2275	418.5	16	75
468	G<452>	2261	518.5	16	75
469	G<454>	2247	418.5	16	75
470	G<456>	2233	518.5	16	75
471	G<458>	2219	418.5	16	75
472	G<460>	2205	518.5	16	75

#	Pad	X	Y	W	H
473	G<462>	2191	418.5	16	75
474	G<464>	2177	518.5	16	75
475	G<466>	2163	418.5	16	75
476	G<468>	2149	518.5	16	75
477	G<470>	2135	418.5	16	75
478	G<472>	2121	518.5	16	75
479	G<474>	2107	418.5	16	75
480	G<476>	2093	518.5	16	75
481	G<478>	2079	418.5	16	75
482	G<480>	2065	518.5	16	75
483	G<482>	2051	418.5	16	75
484	G<484>	2037	518.5	16	75
485	G<486>	2023	418.5	16	75
486	G<488>	2009	518.5	16	75
487	G<490>	1995	418.5	16	75
488	G<492>	1981	518.5	16	75
489	G<494>	1967	418.5	16	75
490	G<496>	1953	518.5	16	75
491	G<498>	1939	418.5	16	75
492	G<500>	1925	518.5	16	75
493	G<502>	1911	418.5	16	75
494	G<504>	1897	518.5	16	75
495	G<506>	1883	418.5	16	75
496	G<508>	1869	518.5	16	75
497	G<510>	1855	418.5	16	75
498	GD<2>	1841	518.5	16	75
499	NC	1827	418.5	16	75
500	NC	1729	518.5	16	75
501	NC	1715	418.5	16	75
502	NC	1701	518.5	16	75
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505	S<1>	1659	418.5	16	75
506	S<2>	1645	518.5	16	75
507	S<3>	1631	418.5	16	75
508	S<4>	1617	518.5	16	75
509	S<5>	1603	418.5	16	75
510	S<6>	1589	518.5	16	75
511	S<7>	1575	418.5	16	75
512	S<8>	1561	518.5	16	75
513	S<9>	1547	418.5	16	75
514	S<10>	1533	518.5	16	75
515	S<11>	1519	418.5	16	75
516	S<12>	1505	518.5	16	75
517	S<13>	1491	418.5	16	75
518	S<14>	1477	518.5	16	75
519	S<15>	1463	418.5	16	75
520	S<16>	1449	518.5	16	75
521	S<17>	1435	418.5	16	75
522	S<18>	1421	518.5	16	75
523	S<19>	1407	418.5	16	75
524	S<20>	1393	518.5	16	75
525	S<21>	1379	418.5	16	75
526	S<22>	1365	518.5	16	75
527	S<23>	1351	418.5	16	75
528	S<24>	1337	518.5	16	75
529	S<25>	1323	418.5	16	75
530	S<26>	1309	518.5	16	75
531	S<27>	1295	418.5	16	75

#	Pad	X	Y	W	H
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533	S<29>	1267	418.5	16	75
534	S<30>	1253	518.5	16	75
535	S<31>	1239	418.5	16	75
536	S<32>	1225	518.5	16	75
537	S<33>	1211	418.5	16	75
538	S<34>	1197	518.5	16	75
539	S<35>	1183	418.5	16	75
540	S<36>	1169	518.5	16	75
541	S<37>	1155	418.5	16	75
542	S<38>	1141	518.5	16	75
543	S<39>	1127	418.5	16	75
544	S<40>	1113	518.5	16	75
545	S<41>	1099	418.5	16	75
546	S<42>	1085	518.5	16	75
547	S<43>	1071	418.5	16	75
548	S<44>	1057	518.5	16	75
549	S<45>	1043	418.5	16	75
550	S<46>	1029	518.5	16	75
551	S<47>	1015	418.5	16	75
552	S<48>	1001	518.5	16	75
553	S<49>	987	418.5	16	75
554	S<50>	973	518.5	16	75
555	S<51>	959	418.5	16	75
556	S<52>	945	518.5	16	75
557	S<53>	931	418.5	16	75
558	S<54>	917	518.5	16	75
559	S<55>	903	418.5	16	75
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655	S<151>	-441	418.5	16	75
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#	Pad	X	Y	W	H
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713	S<209>	-1253	418.5	16	75
714	S<210>	-1267	518.5	16	75
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716	S<212>	-1295	518.5	16	75
717	S<213>	-1309	418.5	16	75
718	S<214>	-1323	518.5	16	75
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720	S<216>	-1351	518.5	16	75
721	S<217>	-1365	418.5	16	75
722	S<218>	-1379	518.5	16	75
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724	S<220>	-1407	518.5	16	75
725	S<221>	-1421	418.5	16	75
726	S<222>	-1435	518.5	16	75
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728	S<224>	-1463	518.5	16	75
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730	S<226>	-1491	518.5	16	75
731	S<227>	-1505	418.5	16	75
732	S<228>	-1519	518.5	16	75
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734	S<230>	-1547	518.5	16	75
735	S<231>	-1561	418.5	16	75
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737	S<233>	-1589	418.5	16	75
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740	S<236>	-1631	518.5	16	75
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747	NC	-1729	418.5	16	75
748	NC	-1827	518.5	16	75
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758	G<495>	-1967	518.5	16	75
759	G<493>	-1981	418.5	16	75
760	G<491>	-1995	518.5	16	75
761	G<489>	-2009	418.5	16	75
762	G<487>	-2023	518.5	16	75
763	G<485>	-2037	418.5	16	75
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765	G<481>	-2065	418.5	16	75
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772	G<467>	-2163	518.5	16	75
773	G<465>	-2177	418.5	16	75
774	G<463>	-2191	518.5	16	75
775	G<461>	-2205	418.5	16	75
776	G<459>	-2219	518.5	16	75
777	G<457>	-2233	418.5	16	75
778	G<455>	-2247	518.5	16	75
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780	G<451>	-2275	518.5	16	75
781	G<449>	-2289	418.5	16	75
782	G<447>	-2303	518.5	16	75
783	G<445>	-2317	418.5	16	75
784	G<443>	-2331	518.5	16	75
785	G<441>	-2345	418.5	16	75
786	G<439>	-2359	518.5	16	75
787	G<437>	-2373	418.5	16	75
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789	G<433>	-2401	418.5	16	75
790	G<431>	-2415	518.5	16	75
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792	G<427>	-2443	518.5	16	75
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794	G<423>	-2471	518.5	16	75
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798	G<415>	-2527	518.5	16	75
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802	G<407>	-2583	518.5	16	75
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#	Pad	X	Y	W	H
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847	G<317>	-3213	418.5	16	75
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878	G<255>	-3647	518.5	16	75
879	G<253>	-3661	418.5	16	75
880	G<251>	-3675	518.5	16	75
881	G<249>	-3689	418.5	16	75
882	G<247>	-3703	518.5	16	75
883	G<245>	-3717	418.5	16	75
884	G<243>	-3731	518.5	16	75
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#	Pad	X	Y	W	H
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891	G<229>	-3829	418.5	16	75
892	G<227>	-3843	518.5	16	75
893	G<225>	-3857	418.5	16	75
894	G<223>	-3871	518.5	16	75
895	G<221>	-3885	418.5	16	75
896	G<219>	-3899	518.5	16	75
897	G<217>	-3913	418.5	16	75
898	G<215>	-3927	518.5	16	75
899	G<213>	-3941	418.5	16	75
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943	G<125>	-4557	418.5	16	75
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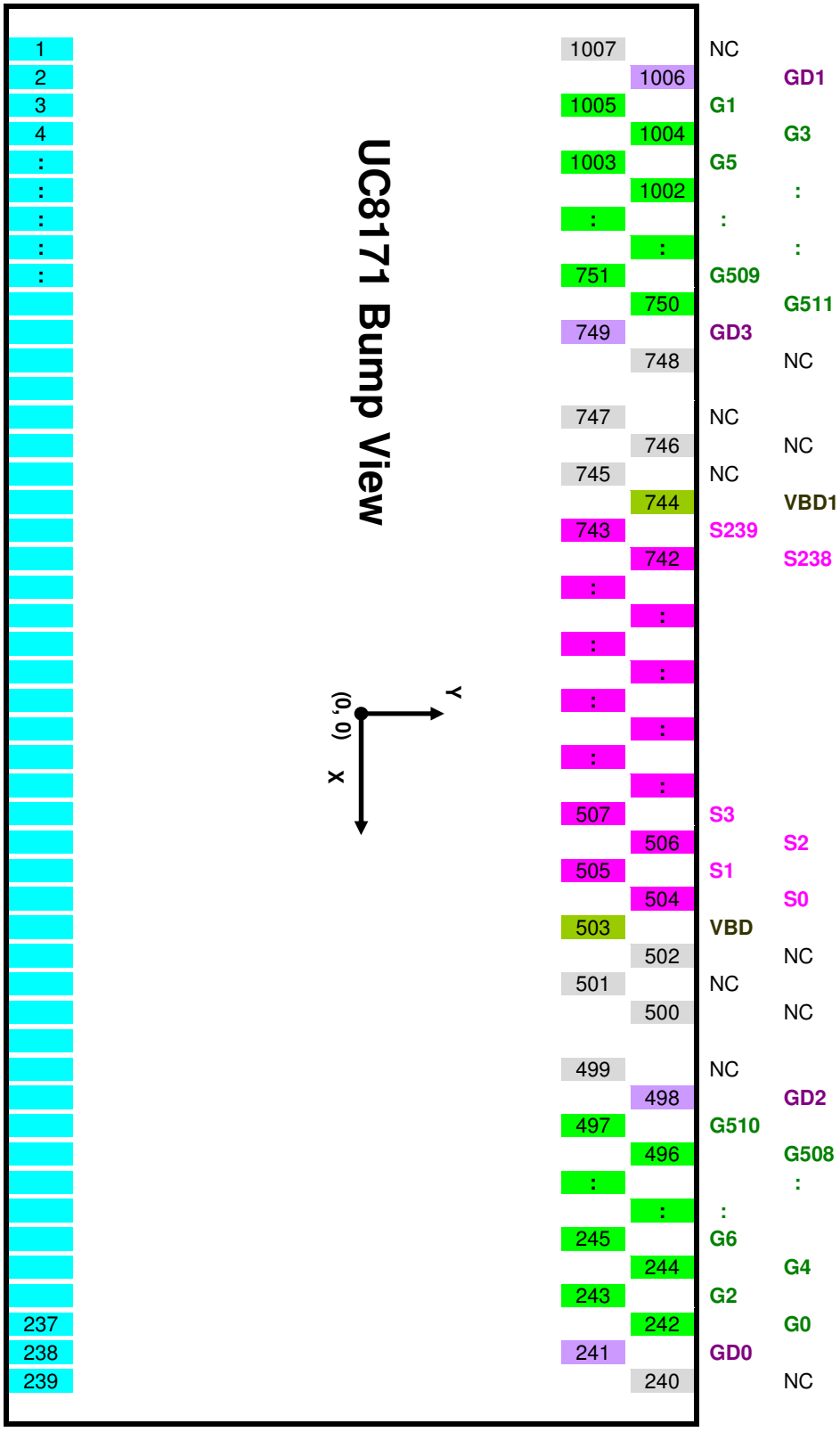
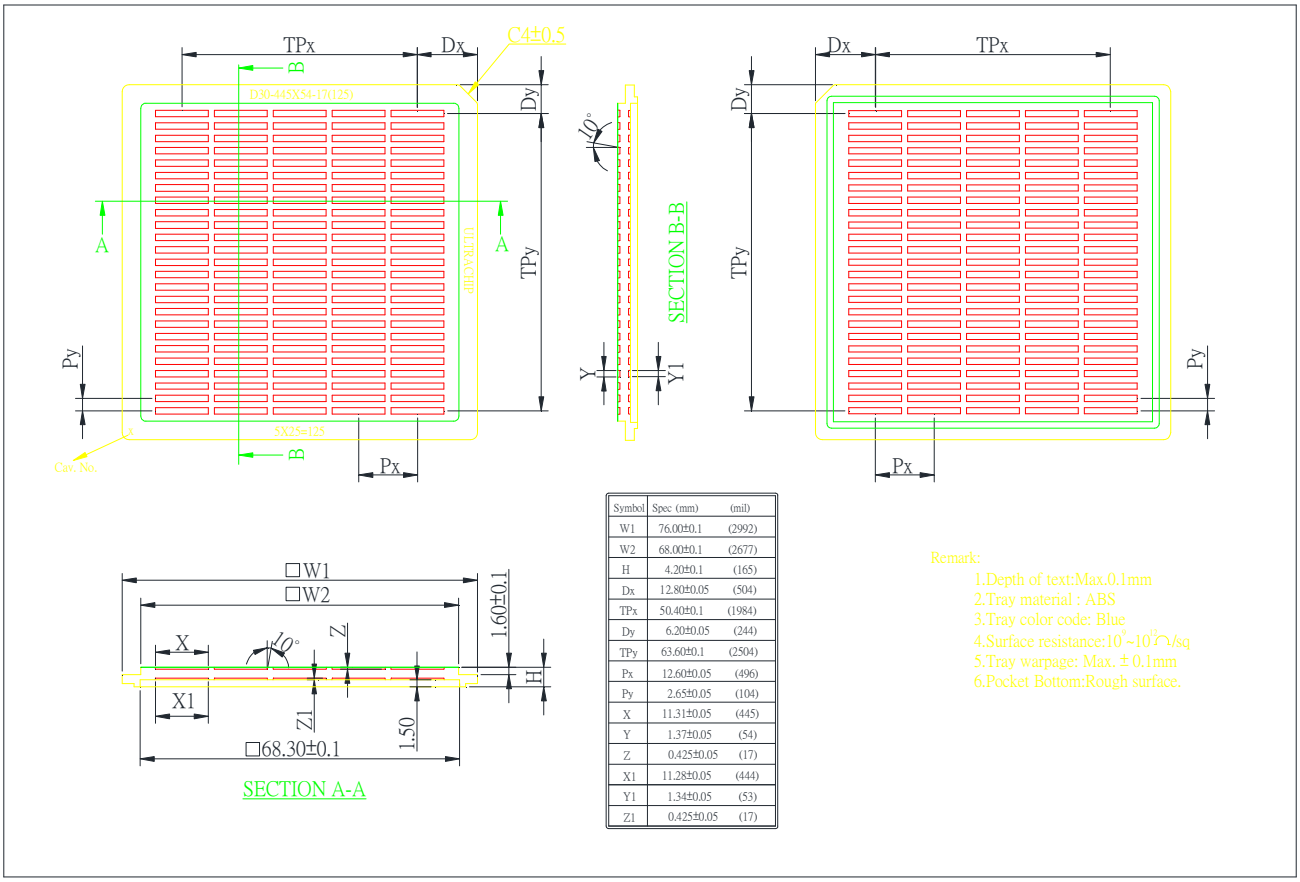
957	G<97>	-4753	418.5	16	75
958	G<95>	-4767	518.5	16	75
959	G<93>	-4781	418.5	16	75
960	G<91>	-4795	518.5	16	75
961	G<89>	-4809	418.5	16	75
962	G<87>	-4823	518.5	16	75
963	G<85>	-4837	418.5	16	75
964	G<83>	-4851	518.5	16	75
965	G<81>	-4865	418.5	16	75
966	G<79>	-4879	518.5	16	75
967	G<77>	-4893	418.5	16	75
968	G<75>	-4907	518.5	16	75
969	G<73>	-4921	418.5	16	75
970	G<71>	-4935	518.5	16	75
971	G<69>	-4949	418.5	16	75
972	G<67>	-4963	518.5	16	75
973	G<65>	-4977	418.5	16	75
974	G<63>	-4991	518.5	16	75
975	G<61>	-5005	418.5	16	75
976	G<59>	-5019	518.5	16	75
977	G<57>	-5033	418.5	16	75

#	Pad	X	Y	W	H
978	G<55>	-5047	518.5	16	75
979	G<53>	-5061	418.5	16	75
980	G<51>	-5075	518.5	16	75
981	G<49>	-5089	418.5	16	75
982	G<47>	-5103	518.5	16	75
983	G<45>	-5117	418.5	16	75
984	G<43>	-5131	518.5	16	75
985	G<41>	-5145	418.5	16	75
986	G<39>	-5159	518.5	16	75
987	G<37>	-5173	418.5	16	75
988	G<35>	-5187	518.5	16	75
989	G<33>	-5201	418.5	16	75
990	G<31>	-5215	518.5	16	75
991	G<29>	-5229	418.5	16	75
992	G<27>	-5243	518.5	16	75
993	G<25>	-5257	418.5	16	75
994	G<23>	-5271	518.5	16	75
995	G<21>	-5285	418.5	16	75
996	G<19>	-5299	518.5	16	75
997	G<17>	-5313	418.5	16	75
998	G<15>	-5327	518.5	16	75
999	G<13>	-5341	418.5	16	75
1000	G<11>	-5355	518.5	16	75
1001	G<9>	-5369	418.5	16	75
1002	G<7>	-5383	518.5	16	75
1003	G<5>	-5397	418.5	16	75
1004	G<3>	-5411	518.5	16	75
1005	G<1>	-5425	418.5	16	75
1006	GD<1>	-5439	518.5	16	75
1007	NC	-5453	418.5	16	75

Output Pad Location



TRAY INFORMATION



Symbol	Spec (mm)	(mil)
W1	76.00±0.1	(2992)
W2	68.00±0.1	(2677)
H	4.20±0.1	(165)
Dx	12.80±0.05	(504)
TPx	50.40±0.1	(1984)
Dy	6.20±0.05	(244)
TPy	63.60±0.1	(2504)
Px	12.60±0.05	(496)
Py	2.65±0.05	(104)
X	11.31±0.05	(445)
Y	1.37±0.05	(54)
Z	0.425±0.05	(17)
X1	11.28±0.05	(444)
Y1	1.34±0.05	(53)
Z1	0.425±0.05	(17)

REVISION HISTORY

Revision	Contents	Date
0.6	Frist release	April 30, 2018
0.8	1.page 51 , recommend device , VDS 20V→25V and VR 20V→25V Add Note: The capacitor value of VGH/VGL must be equal or more than the one of VSH/VSL/VDHR. 2. page 53, modify DC characteristic , data of RON , VDDIO (active current max.) , VDDA (active current max.) Add*:at 85C, the accuracy of TPS is +/-5C 3.page 54 , modify the data of SCL (read) data and SDA access time 4.page 55 , modify the diagram of 4-wire Serial Interface Characteristics (Read mode) and the data of SCL (read) data and SDA access time.	December 5, 2019