



3.7 inch E-paper Display Series

GDEM037F51

Product Specifications



Customer	Standard
Description	3.7" E-PAPER DISPLAY
Model Name	GDEM037F51
Date	2023/09/25
Revision	1.0

	Design Engineering		
	Approval	Check	Design

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1. Over View

GDEM037F51 is an all-in-one Active Matrix EPD module with built-in timing control for ESL applications. It supports 2-bit grayscale per pixel, allowing for white, black, red, and yellow colors. The active area measures 3.7 inches and comprises 416 X 240 pixels. This module utilizes TFT technology and electrophoresis display, featuring integrated components like gate drivers, source drivers, MCU interface, timing controller, oscillator, DC-DC converter, SRAM, LUT, and VCOM.

It is ideal for use in portable electronic devices, particularly Electronic Shelf Label (ESL) Systems.

2. Features:

- 416 X 240 pixels display
- High contrast and high reflectance
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape and portrait modes
- Hard-coat anti-glare display surface
- Ultra-low current deep sleep mode
- On-chip display RAM
- Waveform can be stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator for generating VCOM, Gate, and Source driving voltage
- I2C signal interface for external temperature sensor
- Built-in temperature sensor

3. Mechanical and Optical Specification

Parameter	Specifications		Unit	Remark
Screen Size	3.7		Inch	
Display Resolution	416(V) × 240(H)		Pixel	DPI:130
Active Area	47.04×81.54		mm	
Pixel Pitch	0.196×0.196		mm	
Pixel Configuration	Square			
Outline Dimension	53.00(H)×92.99 (V) ×1.0(D)		mm	
Weight	8.88±0.5		g	

Temperature Range(°C)	0-9	10-19	20-29	30-40	Units
White State	TYP L*	64	63	63	
	MIN L*	62	62	62	
	a*	≤0	≤0	≤0	
	b*	≤2.5	≤2.5	≤2.5	
Black State	TYP L*	9	9	9	
	MAX L*	11	11	11	
	a*	≤9	≤9	≤8	
Red State	MIN L*	23	23	24	
	TYP a*	36	38	40	
	MIN a*	34	34	38	
	MAX b*	34	34	34	
Yellow State	MIN L*	50	50	54	
	TYP b*	55	63	66	
	MIN b*	53	56	60	
	MAX a*	18	18	18	
Ghosting		≤2	≤2	≤2	delta E

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

4. Mechanical Drawing of EPD Module

Confirmation:		DATE	REV.	MODIFICATION												
		2023-07-04	A	FIRST ISSUE												
<p>FRONT VIEW</p> <p>SIDE VIEW</p> <p>BACK VIEW</p> <table border="1"> <tr> <td>MODEL NO.</td> <td>BATCH NO.</td> </tr> <tr> <td colspan="2"> </td> </tr> </table>					MODEL NO.	BATCH NO.										
MODEL NO.	BATCH NO.															
<p>NOTE</p> <p>1 DISPLAY MODULE 3.7" ARRAY FOR EPD 2 DRIVER IC:IST7163 3 RESOLUTION:416gateX240source 4 PIXEL SIZE:0.196mmX0.196mm 5 FOR LO</p>																
<table border="1"> <tr> <td>TOLERANCES UNMARKED ANGLES+5° .X=±0.4mm .XX=±0.20mm .XXX=±0.20mm</td> <td>TITLE: EPD</td> <td>PROJECT: GDEM037F51</td> <td>REV: A</td> <td>DATE: 23.07.04</td> <td>CUST. P/N: 1/1</td> </tr> <tr> <td>DWN: H GONG</td> <td>CHK: JD CHEN</td> <td>APPR: JH LU</td> <td>UNIT: mm</td> <td>3RD ANGLE: </td> <td>PAGE:</td> </tr> </table>					TOLERANCES UNMARKED ANGLES+5° .X=±0.4mm .XX=±0.20mm .XXX=±0.20mm	TITLE: EPD	PROJECT: GDEM037F51	REV: A	DATE: 23.07.04	CUST. P/N: 1/1	DWN: H GONG	CHK: JD CHEN	APPR: JH LU	UNIT: mm	3RD ANGLE: 	PAGE:
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5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	Note 5-6
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	Note 5-6
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

Note 5-6: This pin connect to the VSS if there is no external temperature sensor.

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to +70	°C.
Optimal Storage Temp	TSTGo	23±2	°C.
Optimal StorageHumidity	HSTGo	55±10	%RH

Note:

1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. The storage time is within 10 days for -25°C ~ 70°C.

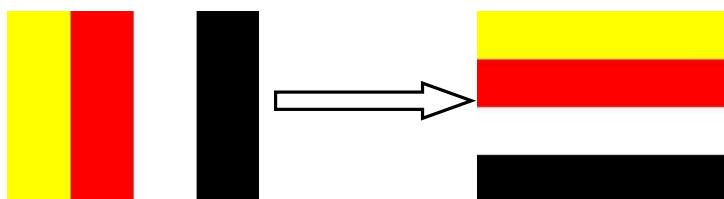
The display screen should be kept white and face up.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	Vss	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.3	3.0	3.6	V
Core logic voltage	VDD		VDD	2.3	3.0	3.6	V
High level input voltage	VIH	-	-	0.8 VCI	-	VCI	V
Low level input voltage	VIL	-	-	0	-	0.2 VCI	V
High level output voltage	VOH	IOH = -100Ma	-	VCI -0.8	-	-	V
Low level output voltage	VOL	IOL = 100Ma	-	-	-	GND +0.2	V
Typical power	PTYP	VCI =3.0V	-	-	13.5	-	mW
Deep sleep mode	PSTPY	VCI =3.0V	-	-	0.0012	-	mW
Typical operating current	Iopr_VC_I	VCI =3.0V	-	-	4.5	-	mA
Image update time	-	23 °C	-	-	20	-	sec
Deep sleep mode current	Idslp_VC_I	DC/DC off No clock No input load Ram data not retain	-	-	0.4	1	uA

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display
4. Electrical measurement: Tektronix oscilloscope - MDO3024,
Tektronix current probe - TCP0030A.

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

Table 6-3-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

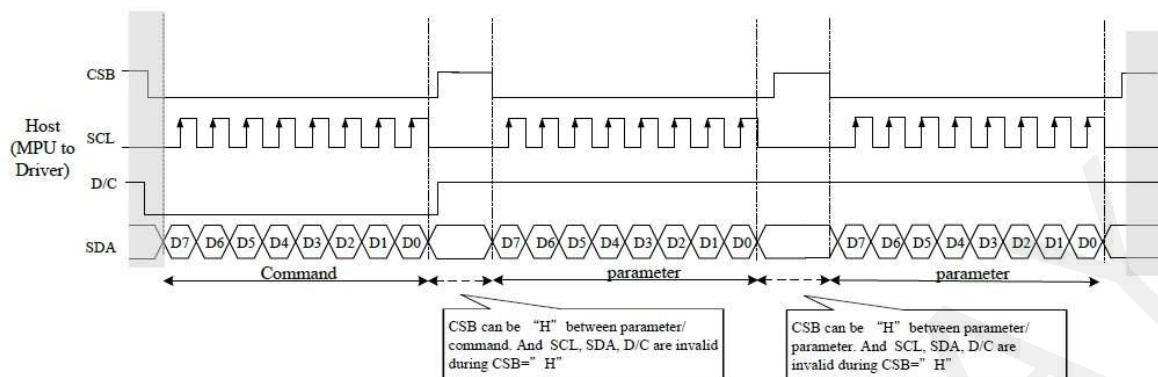
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Table 6-3-2: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

Figure 6-3-1: 4-wire SPI mode



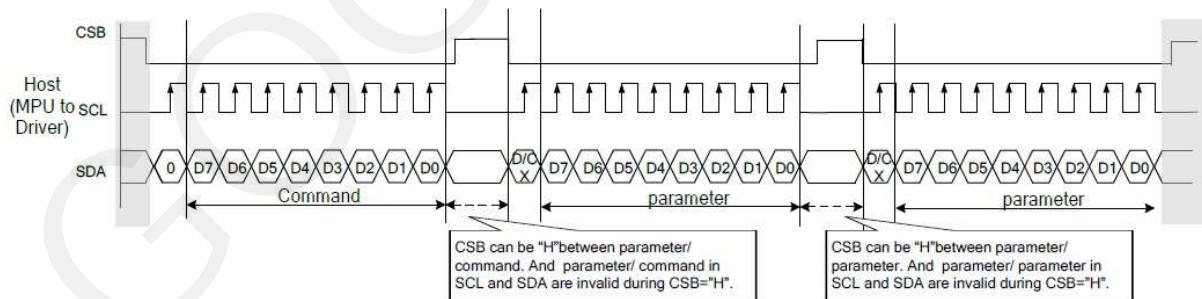
6.3.3 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Table 6-3-3: Control pins of 4-wire Serial Peripheral interface

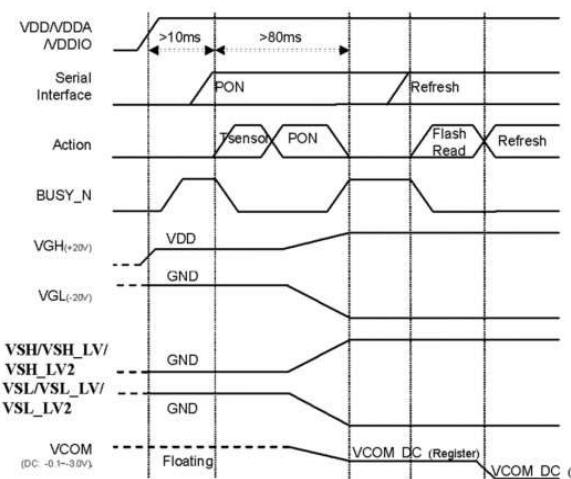
Note: ↑ stands for rising edge of signal

Figure 6-3-2: 3-wire SPI mode

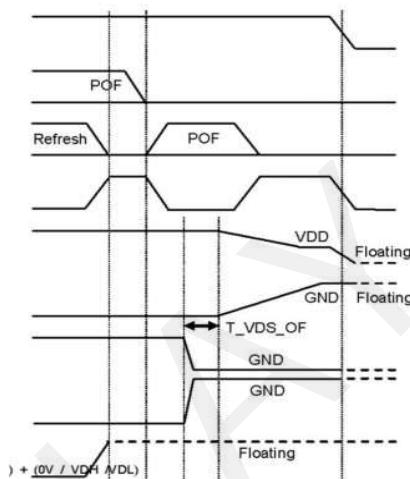


6.3.4 Interface Timing

Power on sequence



Power off sequence



When EPD Power off Must be follow sequence : Firstly VCOM OFF VSH/VSL OFF VGH/VGL OFF
Must no cross when VCOM/VSL /VGL

7.Command Table

R00H(PSR): Panel setting Register

Inst / Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PSR	W	0	0	0	0	0	0	0	0	0	{00H}
1 st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	1	{0FH}
2 nd Parameter	W	1	LUT_EN	0	FOPT	VCOMZ	1	TIEG	NORG	VC_LUTZ	{09H}

1st Parameter:

Bit7-6	Resolution setting
00b	Display resolution is 200x200 (default)
01b	Display resolution is 200x128
10b	Display resolution is 128x200
11b	Display resolution is 128x128

Bit5	Power switch operation mode
0	Power switching time in the period of frame scanning.(default).
1	Power switching time in the external period before frame scanning.

Bit3	UD function(*1)
0	Scandown; First line=Gn,Gn-1, ... G2, Last line=G1
1	Scanup; First line=G1,G2, ... ,Gn-1, Last line=Gn.(default)

Bit2	SHL function(*2)
0	Shift left; First data=S _n ,S _{n-1} , ... ,S ₂ , Last data=S ₁ .
1	Shift right; First data=S ₁ ,S ₂ , ... ,S _{n-1} , Last data=S _n . (default)

Bit1	SHD_N function(*3)
0	Booster OFF, register data are kept, and Source/Border/VCOM are kept OV or floating
1	Booster ON.(default)

2nd Parameter:

Bit0	VC_LUTZ function
0	NO effect.
1	After refreshing display, the output of VCOM is set to floating automatically.(default)

Bit1	NORG function
0	NO effect.(default)
1	After refreshing display, VCOM is tied to GND before power off

Bit2	TIEG function
0	NO effect.(default)
1	After power off booster, VGL will be tied to GND.

Bit4	VCMZ function
0	NO effect.(default)
1	VCOM is always floating.

Bit5	FOPT function
0	Scan 1 frame after waveform finished (Default)
1	No Scan after waveform finished and switch the source channel output to HiZ

Bit7	LUT_EN
0	LUT from OTP(default)
1	LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.

FOPT: Power off floating.

Notes:

1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Inactive source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R01H(PWR): Power Setting Register

Inst / Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWR	W	0	0	0	0	0	0	0	0	1	(01H)
1 st Parameter	W	1	-	-	-	-	-	VSC_EN	VS_EN	VG_EN	(07H)
2 nd Parameter	W	1	-	-	-	-	-	-	VG[1]	VG[0]	(00H)
3 rd Parameter	W	1	-	VDHR [6]	VDHR [5]	VDHR [4]	VDHR [3]	VDHR [2]	VDHR [1]	VDHR [0]	(00H)
4 th Parameter	W	1	-	VDH [6]	VDH [5]	VDH [4]	VDH [3]	VDH [2]	VDH [1]	VDH [0]	(00H)
5 th Parameter	W	1	-	VDL [6]	VDL [5]	VDL [4]	VDL [3]	VDL [2]	VDL [1]	VDL [0]	(00H)
6 th Parameter	W	1	-	VDHR1 [6]	VDHR1 [5]	VDHR1 [4]	VDHR1 [3]	VDHR1 [2]	VDHR1 [1]	VDHR1 [0]	(00H)

Power mode switch mapping:

Mode 0 : 0V & +15V & -15V & VDHR (+3V~+15V)

Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)

1st Parameter:

Bit2	Source LV power selection.
0	External source LV power from VDHR pins.
1	Internal DC/DC function for generate VDHR.

Bit1	Source power selection.
0	External source power from VDH/VDL pins.
1	Internal DC/DC function for generate VDH/VDL.

Bit0 Gate power selection.

0	External gate power from VGH/VGL pins.
1	Internal DCDC function for generate VGH/VGL.

2nd Parameter:

Bit1-0	VGHL Voltage Level.
00	VGH=20v, VGL=-20v(default)
01	VGH=17v, VGL=-17v
10	VGH=15v, VGL=-15v
11	VGH=10v, VGL=-10v

3rd & 4th Parameter: Internal VDHR/VDH power selection (Default value: 0000000b)

5th & 6th Parameter: Internal VDL/VDHR1 power selection (Default value: 0000000b)

Bit6-0	Internal VDH selection.	Internal VDL selection.	Bit6-0	Internal VDH selection.	Internal VDL selection.
0000000	3V	-3V	0110010	8.0V	-8.0V
0000001	3.1V	-3.1V
0000010	3.2V	-3.2V	0111100	9.0V	-9.0V
0000011	3.3V	-3.3V
0000100	3.4V	-3.4V	1000110	10.0V	-10.0V
0000101	3.5V	-3.5V
0000110	3.6V	-3.6V	1010000	11.0V	-11.0V
0000111	3.7V	-3.7V
0001000	3.8V	-3.8V	1011010	12.0V	-12.0V
0001001	3.9V	-3.9V
0001010	4.0V	-4.0V	1100100	13.0V	-13.0V
0001011	4.1V	-4.1V
0001100	4.2V	-4.2V	1101110	14.0V	-14.0V
0001101	4.3V	-4.3V
0001110	4.4V	-4.4V	1111000	15.0V	-15.0V
0001111	4.5V	-4.5V			
0010000	4.6V	-4.6V			
...			
0010100	5.0V	-5.0V			
...			
0011110	6.0V	-6.0V			
...			
0101000	7.0V	-7.0V			
...			

Notes:

1. If gate voltage is set to +/-17v, +/-15v, +/-10v, IC will auto correct source voltage as follows:
2. VGH-VDH/VDH/VDHR1 \geq 2v
3. VGL-VDL \geq -2v

R02H(POF): Power OFF Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
POF	W	0	0	0	0	0	0	0	1	0	(02H)
1st Parameter	W	1	-	-	-	-	-	-	-	EDSE	(00H)

After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will become "0".

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register will keep until VDD become off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R03H(POFS): Power on/off Sequence Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PFS	W	0	0	0	0	0	0	0	1	1	(03H)
1st Parameter	W	1	-	-	T_VDPG_OFF	-	-	-	T_VDS_OFF	-	(00H)

1st Parameter:

Bit1-0	Power off sequence of VDH and VDL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

Bit5-4	Power off sequence of VGH and VGL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

R04H(PON):Power ON Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PON	W	0	0	0	0	0	0	1	0	0	(04H)

After power on command, the driver will power ON base on Power ON sequence.

After power on command and all power sequence are ready (based on PWR command), then BUSY_N

signal will become "1". This command only active when BUSY_N="1".

R06H(BTST): Booster Soft Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUTO	W	0	0	0	0	0	0	1	1	0	(06H)
1# Parameter	W	1	BT_PHA1	BT_PHA0	0	0	0	0	0	0	(00H)
2# Parameter	W	1	BT_PHB1	BT_PHB0	0	0	0	0	0	0	(00H)
3# Parameter	W	1	BT_PHC1	BT_PHC0	0	0	0	0	0	0	(00H)

D7-D6		soft start period
00		10ms (default)
01		20ms
10		30ms
11		40ms

R07H(DSLP): Deep Sleep Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSLP	W	0	0	0	0	0	0	1	1	1	(07H)
1# Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

R10H(DTM): Data Start Transmission Register

	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DTM	W	0	0	0	0	1	0	0	0	0	{10H}
2-bit mode											
1 st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		{00H}
:	W	1	:		:		:		:		{00H}
N th Parameter	W	1	Pixel[n-3]		Pixel[n-2]		Pixel[n-1]		Pixel(n)		{00H}

NOTE: "-" Don't care, can be set to VDD or GND level. "X": Dummy data, it would not be stored in frame buffer.

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

Pixel[1~n][1:0](2-bitmode):

ImageData	Source Driver Output			
	DDX=1(Default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00	Gray0	ogram00	Gray3	ogram03
01	Gray1	ogram01	Gray2	ogram02
10	Gray2	ogram02	Gray1	ogram01
11	Gray3	ogram03	Gray0	ogram00

Data mapping example:

When DDX=1, Pixel[1:0]= 01 -> Gray level select = Gray1, follow LUT data output from IP output port "ogram01".

When DDX=0, Pixel[1:0] = 11 -> Gray level select = Gray 0, follow LUT data output from IP output port "ogram00".

R11H(DSP): DataStop Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSP	W	0	0	0	0	1	0	0	0	1	(11H)
1 st Parameter	R	1	data_flag	-	-	-	-	-	-	-	(00H)

To stop data transmission, this command must be issued to check the data_flag.

1st Parameter:

Bit7	Data flag of receiving user data.
0	Driver didn't receive all the data.
1	Driver has already received all the one frame data.

After "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

This command only active when BUSY_N = "1".

R12H(DRF): Display Refresh Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DRF	W	0	0	0	0	1	0	0	1	0	(12H)
1 st Parameter	W	1	-	-	-	-	-	-	-	AC/DCVCOM	(00H)

While user sent this command, driver will refresh display(data/VCOM) base on SRAM data and LUT.

AC/DCVCOM: AC,DCVCOM select.

0: ACVCOM,VCOM will follow LUTC when updating image. (default)

1: DCVCOM,VCOM will always be VCOMDC when updating image

After display refresh command, BUSY_N signal will become "0"

This command only active when BUSY_N = "1".

R17H(AUTO): Auto Sequence Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Auto Sequence	W	0	0	0	0	1	0	1	1	1	{17H}
	W	1	1	0	1	0	0	1	0	1	{A5H}

The command can enable the internal sequence to execute several commands continuously.

The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO(0x17)+Code{0xA5}=(PON → DRF → POF)

AUTO(0x17)+Code{0xA7}=(PON → DRF → POF → DSLP)

R30H(PLL): PLL Control Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PLL	W	0	0	0	1	1	0	0	0	0	{30H}
1# Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	{02H}

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

Bit3	Dynamic frame rate (Elink use only)
0	Disable(default)
1	Enable

FR[2:0]	Framerate
000	12.5 Hz
001	25 Hz
010	50 Hz (default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

R40H(TSC): Temperature Sensor Command Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	0	0	0	0	0	0	(40H)
1 st Parameter	R	1	TS[7]	TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	(00H)

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads temperature sensor value.

BUSY_N become low after TSC command. When BUSY_N become high, Parameter can be read.

This command only active when BUSY_N="1"

Temperature boundary: -25C~60

TS[7:0]/D[10:3]	Temperature (°C)	TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25	0000_0000	0
1110_1000	-24	0000_0001	1
1110_1001	-23	0000_0010	2
1110_1010	-22	0000_0011	3
1110_1011	-21	0000_0100	4
1110_1100	-20	0000_0101	5
1110_1101	-19	0000_0110	6
...
1111_1110	-2	0011_1011	59
1111_1111	-1	0011_1100	60

R41H(TSE): Temperature Sensor Enable Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSE	W	0	0	1	0	0	0	0	0	1	(41H)
1 st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	(00H)

This command indicates the driver IC temperature sensor enable and calibration function.

1st Parameter:

Bit3-0	Temperature level	Bit3-0	Temperature level
0000	+0°C (Default)	1000	-4°C
0001	+0.5°C	1001	-3.5°C
...
0111	+3.5°C	1111	-0.5°C

Bit[3:0]: Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean "+" or "-" while 0 is "+"; 1 is "-"

2. TO[2:0]: mean temperature offset value

R44H(GPI Sensing): GPIO Input Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	{44H}
	W	1	-	-	-	-	-	-	-	GPIS	{00H}

This command will indicate status of GPI

GPIS : 0 detected low logic on GPIO

1 detected high logic on GPIO

R50H(CDI): VCOM and DATA Interval Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CDI	W	0	0	1	0	1	0	0	0	0	{50H}
1# Parameter	W	1	VBD[2]	VBD[1]	VBD[0]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	{97H}

This command can set 2 kinds of parameters,1.VCOM to data output interval(CDI) 2.Boarer pin output.

VBD[2:0]: Border data selection (from LUT output by IP port border_w[1:0]).

This register will make boarder pin output being mapped to a certain grayscale.

DDX[0]	VBD[2:0]	Gray level select	IP setting for Border LUT select
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (Default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating(Default)	N/A

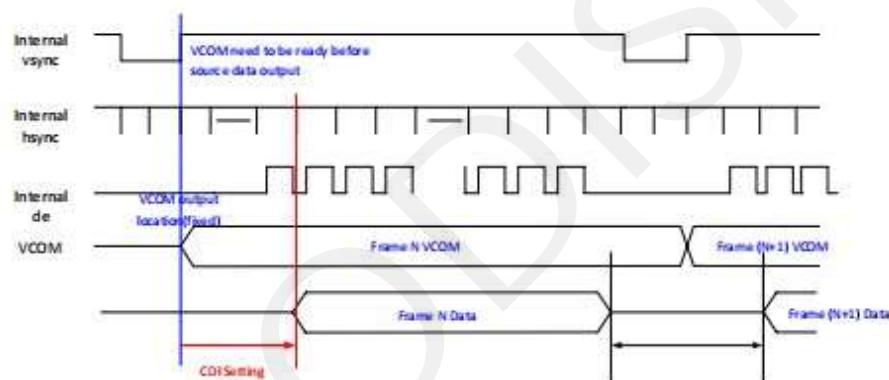
Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V, without VCOM offset,the real output on Boarder pin shall be 15V.

Boarder output will follow FOPT definition being defined in R00h

This command indicates the interval of Vcom and data output. When setting the vertical backporch, the total blanking will be kept as a default value (count by HSYNC)

Bit3	Bit2	Bit1	Bit0	VCOM and data interval
0	0	0	0	17 hsync
0	0	0	1	16 hsync
0	0	1	0	15 hsync
0	0	1	1	14 hsync
0	1	0	0	13 hsync
0	1	0	1	12 hsync
0	1	1	0	11 hsync
0	1	1	1	10 hsync (Default)
1	0	0	0	9 hsync.
1	0	0	1	8 hsync
1	0	1	0	7 hsync
1	0	1	1	6 hsync
1	1	0	0	5 hsync
1	1	0	1	4 hsync
1	1	1	0	3 hsync
1	1	1	1	2 hsync



R51H(LPD): Lower Power Detection Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LPD	W	0	0	1	0	1	0	0	0	1	(51H)
1#Parameter	R	1	-	-	-	-	-	-	-	LPD	(01H)

This command indicates the input power condition. Host can read this data to understand the battery condition.

When LPD="1", system input power is normal.

When LPD="0", Low power input (VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL)

Bit0	LPD
0	Lowpowerinput.
1	Normalstatus.(Default)

This command only active when BUSY_N="1".

R60H (TCON): TCON setting Register

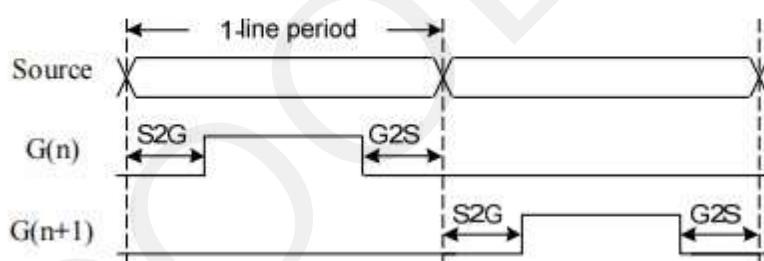
Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	1	0	0	0	0	0	{60H}
1 st Parameter	W	1	-	-	S2G[5]	S2G[4]	S2G[3]	S2G[2]	S2G[1]	S2G[0]	{02H}
2 nd Parameter	W	1	-	-	G2S[5]	G2S[4]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	{02H}

The command define as Non-overlap period of gate and source and as below:

S2G[5:0] or G2S[5:0]	Period
0	1unit
1	2unit
2	3unit(Default)
3	4unit
4	5unit
5	6unit
6	7unit
7	8unit
8	9unit
9	10unit
10	12unit
11	14unit
12	16unit
13	18unit
....	...
63	118unit

1 unit = 500ns

Gon_T= 1 line period - S2G -G2S, minimum Gon_T = 2 units. If(1line period - S2G -G2S) < 2 units , Gon_T = 2 units



R61H(TRES): Resolution Setting Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TRES	W	0	0	1	1	0	0	0	0	1	{61H}
1 st Parameter	W	1	-	-	-	-	-	-	HRES[9]	HRES[8]	
2 nd Parameter	W	1	HRES[7]	HRES[6]	HRES[5]	HRES[4]	HRES[3]	HRES[2]	0	0	{00H}
3 rd Parameter	W	1	-	-	-	-	-	-	VRES[9]	VRES[8]	{00H}
4 th Parameter	W	1	VRES[7]	VRES[6]	VRES[5]	VRES[4]	VRES[3]	VRES[2]	VRES[1]	VRES[0]	{00H}

Note: HRES \leq Horizontal line of PSR, VRES \leq Vertical line of PSR.

No matter what value being set in D1 and D0 of 1st parameter(HRES[1] and HRES[0]), the register shall be kept as 0

When using register:

Horizontal display resolution = HRES

Vertical display resolution = VRES

HRES[9]=0,HRES[8]=0, and VRES[9]=0 ,VRES[8]=0

Channel disable calculation:

GD: First G active=G0; LAST active GD = first active+VRES[7:0]-1

SD: First active channel:=S0; LAST activeSD = first active+HRES[7:2]*4-1

R65H(GSST): GATE/SOURCE START SETTING

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GSST	W	0	0	1	1	0	0	1	0	1	{65H}
1 st Parameter	W	1	-	-	-	-	-	-	-	-	{00H}
2 nd Parameter	W	1	HST(7)	HST(6)	HST(5)	HST(4)	HST(3)	HST(2)	0	0	{00H}
3 rd Parameter	W	1	-	-	-	-	-	-	-	-	{00H}
4 th Parameter	W	1	VST(7)	VST(6)	VST(5)	VST(4)	VST(3)	VST(2)	VST(1)	VST(0)	{00H}

This command defines resolution start gate/source position.

HST[7:2]: Horizontal Display Start Position (Source)

VST[7:0]:Vertical Display Start Position (Gate)

R70H(REV): Chip Revision Register

Inst./Para.	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REV	W	0	0	1	1	1	0	0	0	0	{70H}
1 st Parameter	R	1	REVO[7]	REVO[6]	REVO[5]	REVO[4]	REVO[3]	REVO[2]	REVO[1]	REVO[0]	{08H}
2 nd Parameter	R	1	REV1[7]	REV1[6]	REV1[5]	REV1[4]	REV1[3]	REV1[2]	REV1[1]	REV1[0]	{04H}
3 rd Parameter	R	1	REV2[7]	REV2[6]	REV2[5]	REV2[4]	REV2[3]	REV2[2]	REV2[1]	REV2[0]	{01H}

 1st Parameter:

Bit7-0	REVO
-	Elink internal number

 2nd Parameter:

Bit7-0	REV1
-	Elink internal number

 3rd Parameter:

Bit7-0	REV2
-	Increased each revision

R80H(AMV): Auto Measurement VCOM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	{Code}
AMV	W	0	1	0	0	0	0	0	0	0	(80H)
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	AMVX	AMVS	AMV	AMVE	(00H)

This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit7-6	The sensing points of sampling time
00	2(default)
01	4
10	8
11	16

Sampling time= the last quarter of sensing time (T)

VCOM = average of N points. N=2,4,8,16

Bit5-4	The sensing time of VCOM detection
00	5s(default)
01	10s
10	15s
11	20s

Bit3	XON setting for all Gate ON of AMV
0	Gate scan normally during Auto Measure VCOM period.(default)
1	All Gate ON during Auto Measure VCOM period.

Bit2	AMVS setting for Source output of AMV
0	Source output OV during Auto Measure VCOM period.(default)
1	Source output VSPL during Auto MeasureVCOM period.

Bit1	Analogy signal
0	Get VCOM value by R81H(default)
1	Gate scan only. Measure VCOM externally by probing the VCOM pad.

Bit0	Auto Measure VCOM setting
0	Auto measure VCOM disble (default)
1	Auto measure VCOM enable

R81H(VV): VCOM Value Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1 [#] Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	(00H)

This command gets Vcom value.

1st Parameter:

Bit6-0	VCOM value
0000000	0V
0000001	-0.05V
0000010	-0.10V
:	:
1010000	-4.00V
Others	-

R82H(VDCS): VCM_DC Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VDCS	W	0	1	0	0	0	0	0	1	0	(82H)
1 [#] Parameter	W	1	OTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	(00H)

This command set the VCOMDC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit7	Follow OTP VCOM value in OTP mode
0	IP output value(default)
1	From the setting register

Bit6-0	VCOM value
0000000	0V(default)
0000001	-0.05V
0000010	-0.10V
:	:
1010000	-4.00V
Others	-

R90H(PGM): Program Mode

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Enter Program Mode	W	0	1	0	0	1	0	0	0	0	{90H}

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

R91H(APG): Active Program

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Active Program OTP	W	0	1	0	0	1	0	0	0	1	{91H}

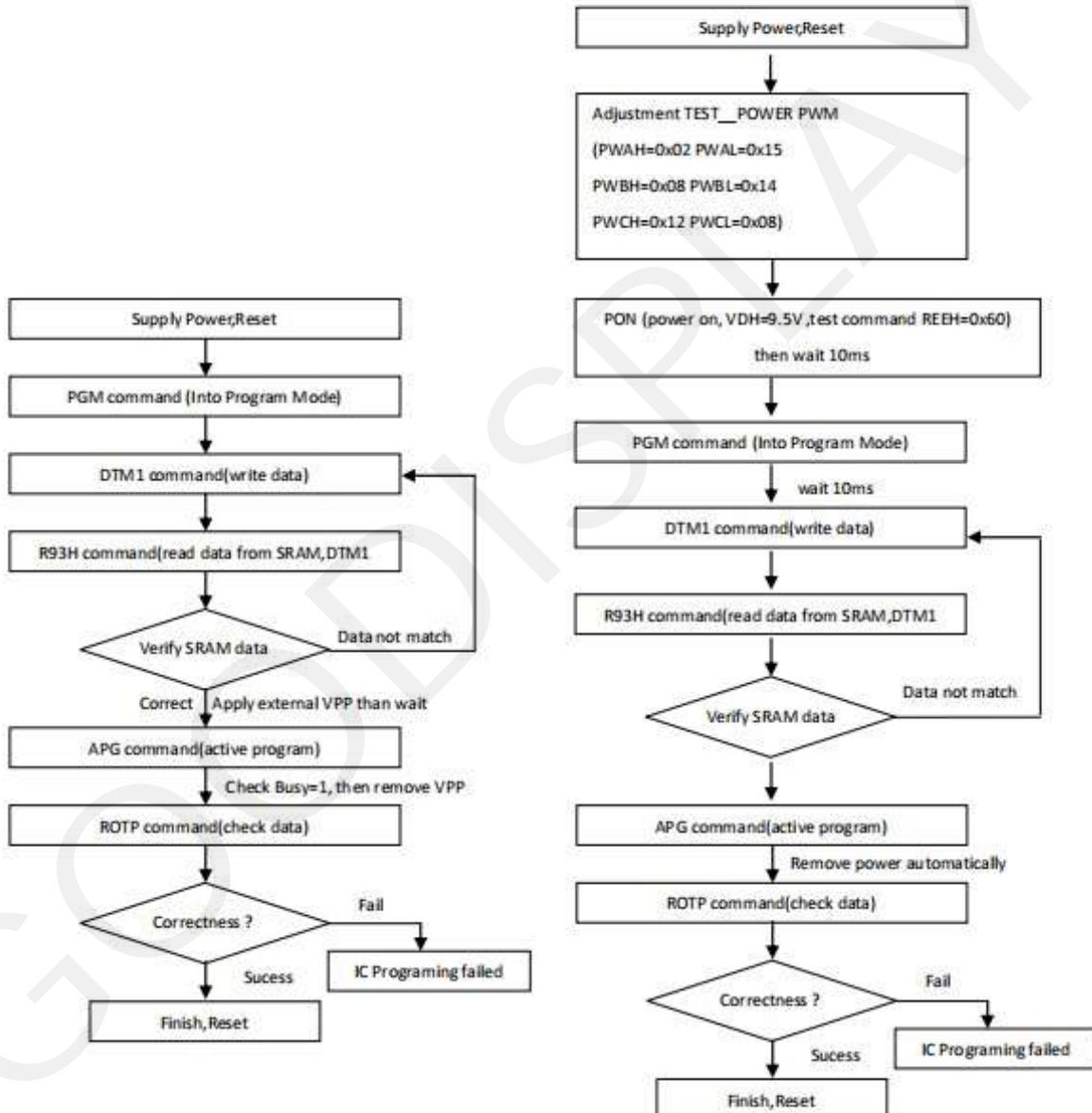
After this command is transmitted, the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

This command only active when BUSY_N="1"

R92H(ROTP): Read OTP Data

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read OTP Data	W	0	1	0	0	1	0	0	1	0	(92H)
	R	1									(00H)
	R	1									(00H)
	R	1									(00H)
	R	1									(00H)



OTP Programming Flow (External VPP)

OTP Programming Flow (Internal VPP)

R93H(RSRAM):Read SRAM Register

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read SRAM Data	W	0	1	0	0	1	0	0	1	1	{93H}
	R	1	-	-	-	-	-	-	-	-	{00H}
	R	1	-	-	-	-	-	-	-	-	{00H}
	R	1	-	-	-	-	-	-	-	-	{00H}
	R	1	-	-	-	-	-	-	-	-	{00H}

RA2H(PGM_CFG):OTP Program Config Register

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Config	W	0	1	0	1	0	0	0	1	0	{A2H}
1 st Parameter	W	1	-	-	-	VPPSEL	-	-	-	-	{00H}
2 nd Parameter	W	1	-	-	-	-	PGM_SADDR[15:8]	-	-	-	{00H}
3 rd Parameter	W	1	-	-	-	-	PGM_SADDR[7:0]	-	-	-	{00H}
4 th Parameter	W	1	-	-	-	-	PGM_DSIZE[15:8]	-	-	-	{15H}
5 th Parameter	W	1	-	-	-	-	PGM_DSIZE[7:0]	-	-	-	{DFH}

This command is to set the configuration of OTP

1st Parameter

Bit4	VPPSEL
0	External VPP (default)
1	Internal VPP

2nd and 3rd Parameters: Program start address PGM_SADDR[15:0]

4th and 5th Parameters: Program data size PGM_DSIZE[15:0]

RA3H(PGM_STAT):OTP Program Status Register

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Status	W	0	1	0	1	0	0	0	1	1	{A3H}
1 st Parameter	W	1	-	-	-	-	-	-	PGM_VER_E RR	PGM_EXE_E RR	{00H}

This command is to read OTP Program status

1st Parameter:

Bit1	Data verification of APG
0	OK
1	NOK

Bit0	OTP program execution status
0	Normal
1	Invalid APG setting

RE0H(CCSET):Chip Temperature Input Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Temperature Input	W	0	1	1	1	0	0	0	0	0	{E0H}
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	0	{00H}

This command is control input path of temperature value

1st Parameter:

Bit0	Temperature Input Selection
0	Use temperature sensor (default)
1	Use TSSET[7:0] value

RE4H(LVSEL): LVD Voltage Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Select LVD Voltage	W	0	1	1	1	0	0	1	0	0	{E4H}
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		{03H}

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVDvalue
00	<2.2V
01	<2.3V
10	<2.4V
11	<2.5V (default)

RE6H(TSSET): Force Temperature Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Force Temperature	W	0	1	1	1	0	0	1	1	0	{E6H}
1st Parameter	W	1	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	{03H}

TS[7:0]: Temperature boundary: -25C~60C

When TSFIX=1, Internal TS is disable, Temperature value will be set by TS[7:0].

TS[7:0]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
...	...
1111_1110	-2
1111_1111	-1

TS[7:0]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
...	...
0011_1011	59
0011_1100	60

RFFH(TEST): TEST MODE Register

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	{FFH}
1 st Parameter	W	1									{A5H}

Enter TEST MODE

TEST(0xFF)+Code(0xA5)=ENTER TEST MODE

TEST(0xFF)+Code(0xE3)=QUIT TEST MODE

RA8H(TEST): VDHROS_EN

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	0	1	0	1	0	0	0	{A8H}
1 st Parameter	W	1	0	0	1	1	1	1	1	1	VDHROS_EN {3EH}

The enable signal of VDHROS discharge offset

Bit0	VDHROS discharge offset enable
0	ON(default)
1	OFF

RC9H(TEST): GDROTP

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	1	0	0	1	{C9H}
1 st Parameter	W	1									{F8H}

Bit7-6	GDR driving within BT_PHA
Bit5-4	GDR driving within BT_PHB
Bit3-2	GDR driving within BT_PHC
Bit1-0	GDR driving within DISP_PHD

RDAH(TEST): Driving Select

Inst./Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	0	1	0	{DAH}
1 st Parameter	W	1	0	0	0	0	1	VDHR_SEL	VDH_SEL	VDL_SEL	{0FH}

The clamping ability selection of VDH/VDL/VDHR

Bit2	VDHR driving	0:weak	1:strong(default)
Bit1	VDH driving	0:weak	1:strong(default)
Bit0	VDL driving	0:weak	1:strong(default)

RDCH(TEST): CPCK SET enable

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	0	{DCH}
1 st Parameter	W	1	0	0	0	0	0	0	CPCDFEN	CPCKEN	{03H}

Bit0	CPCKEN : CPCK enable 0:OFF 1:ON
Bit1	CPCDFEN : CPCK PWL SET & CPCK PWL SET enable 1:follow default 0:follow RDDH & RDEH

RDDH(TEST): CPCK PWL SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	1	{DDH}
1 st Parameter	W	1									{DBH}

Set duration time of VDH/VDL/VDHR clamping.

Bit7-0	
00H	0 ns
01H	125 ns(default)
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns

RDEH(TEST): CPCK PWL SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	0	{DEH}
1 st Parameter	W	1									{08H}

Set duration time of VDH/VDL/VDHR discharge.

Bit7-0	
00H	0 ns
01H	125 ns(default)
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns

RE8H(TEST): VDLOS_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	0	0	0	(EBH)
1 st Parameter	W	1	0	0	0	0	0	0	VDLOS_SEL		(01H)

The discharge ability selection of VDL

Bit1-0	00>01>10>11
--------	-------------

REEH(TEST POWER MODE): TEST POWER MODE Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	1	1	0	(EEH)
1 st Parameter	W	1	0	OPWRMD	1	0	0	0	0	0	(20H)

OPWRMD= 1: Enter POWER MODE

Just for OTP PRG

RFDH(TEST): VDLOS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	0	1	(FDH)
1 st Parameter	W	1	0	0	0	0	0	0	0	VDLOS_EN	(00H)

The enable signal of VDL discharge offset

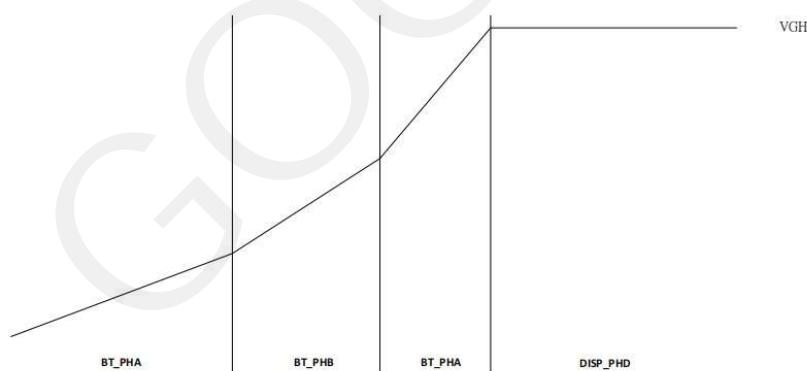
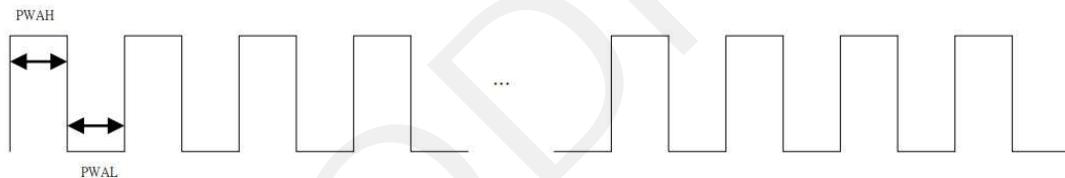
Bit0	The enable signal of VDL discharge offset
0	ON(default)
1	OFF

REFH(TEST_POWER_PWM):TEST_POWER PWM Register

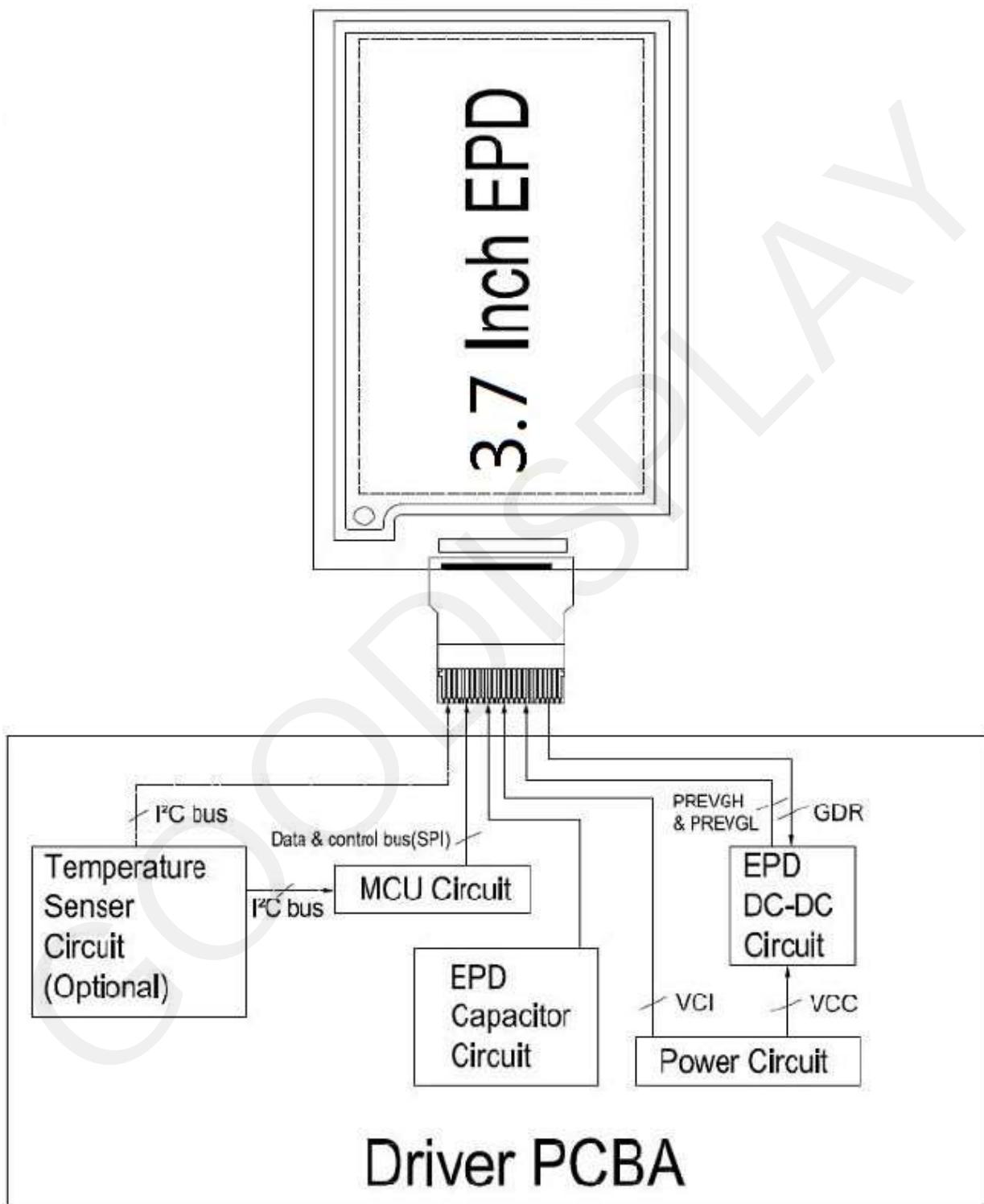
Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	1	1	1	(EFH)
1 st Parameter	W	1									(02H)
2 nd Parameter	W	1									(88H)
3 rd Parameter	W	1									(02H)
4 th Parameter	W	1									(1AH)
5 th Parameter	W	1									(04H)
6 th Parameter	W	1									(24H)
7 th Parameter	W	1									(08H)
8 th Parameter	W	1									(6EH)

1nd Parameter:

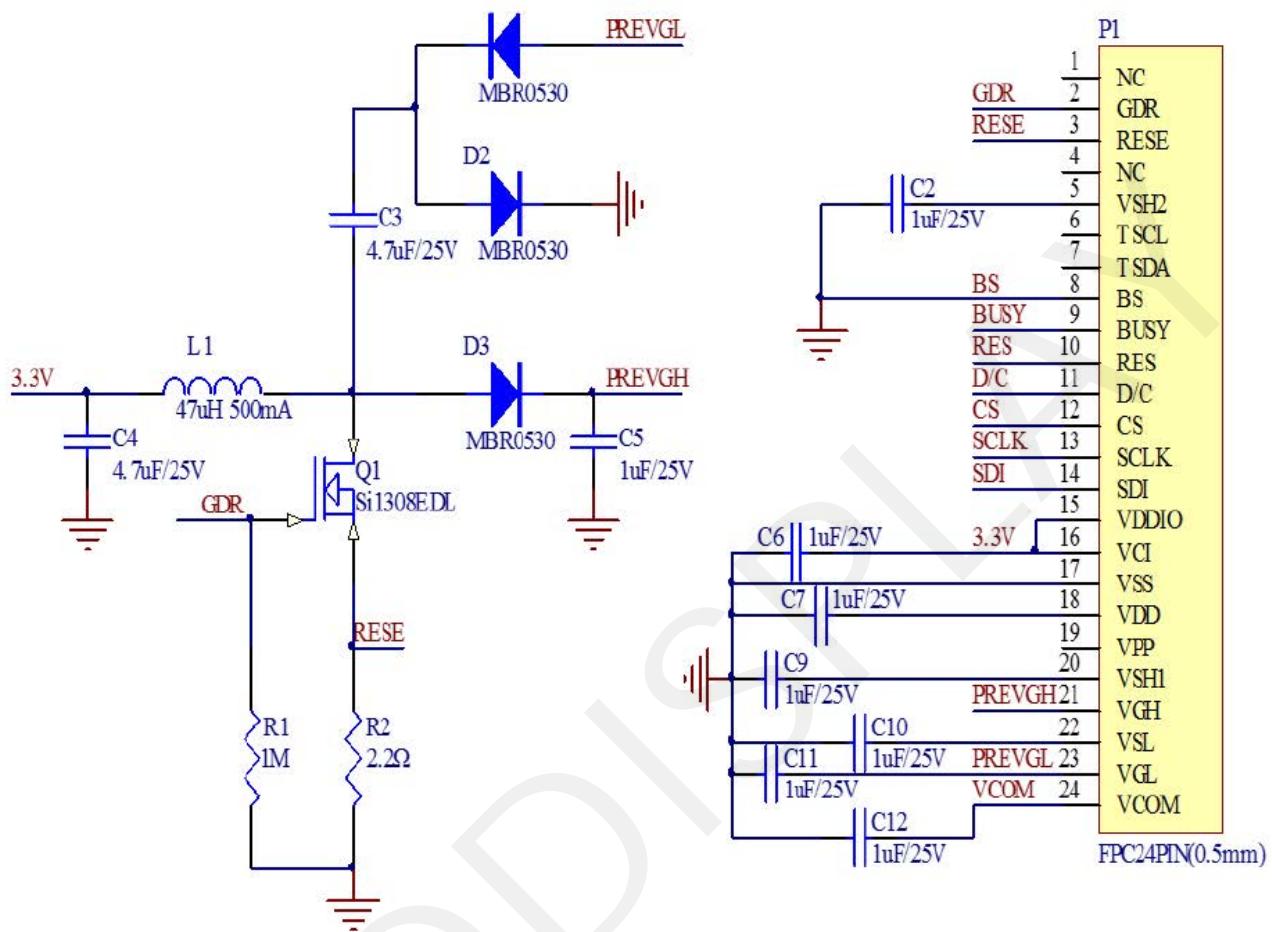
Bit7-0	PWxH/L time
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



8. Block Diagram

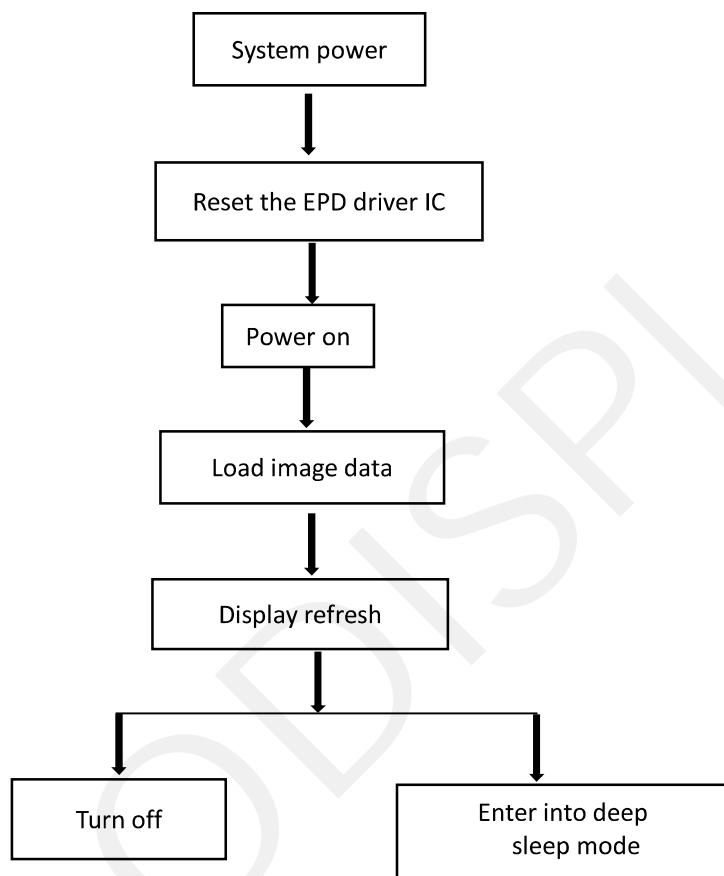


9. Typical Application Circuit with SPI Interface

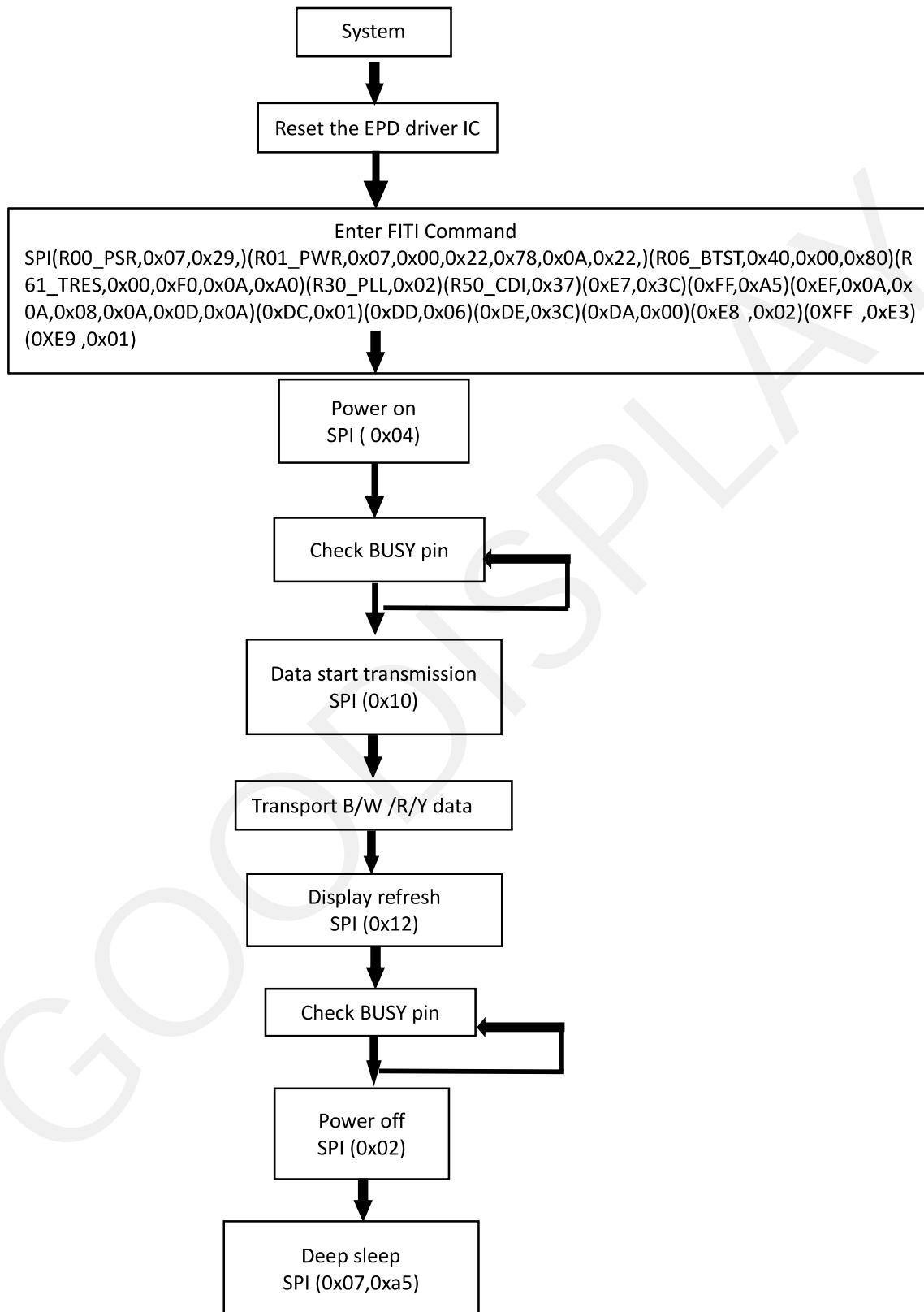


10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



10.2 OTP Operation Reference Program Code



11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBMC:100pF;R:1.5kohm) Contact+/-200V(MMC:200pF;R:0ohm) (Naked EPD display,including IC and FPC area)
9	UV exposure Resistance	762W/m ² for 168 hrs,40°C Test in white pattern

Note:

1. Stay white pattern for storage and non-operation test.
2. Operation is black→white→red→yellow pattern, the interval is 150s.
3. Put in 20°C--25°C for 1hour after test finished, The function ,appearance and display performance is OK.

12.Quality Assurance

12.1 Environment

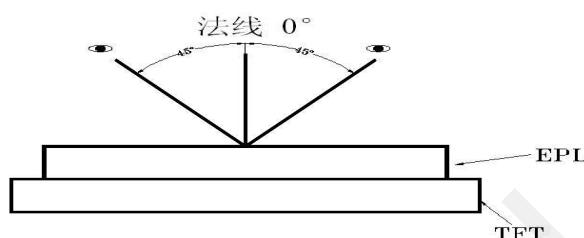
Temperature: $18 \pm 28^\circ\text{C}$

Humidity: 40%~70%RH

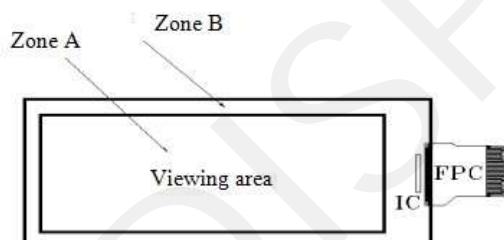
12.2 Illuminance

Brightness: 800 ~ 1500LUX; Angle: Relate $45 \pm 5^\circ$ surround; Function check when 150 ~ 200 LUX visual distance module surface 30CM

12.3 Inspect method



12.4 Display area



12.5 Ghosting test method

Three-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by DKE.



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

W ghosting: $\Delta E = \text{Max} (\Delta Eab(Y-W, R-W), \Delta Eab(Y-W, W-W), \Delta Eab(Y-W, B-W), \Delta Eab(R-W, W-W), \Delta Eab(R-W, B-W), \Delta Eab(W-W, B-W))$

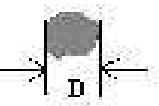
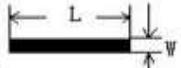
K ghosting: $\Delta E = \text{Max} (\Delta Eab(Y-K, R-K), \Delta Eab(Y-K, W-K), \Delta Eab(Y-K, B-K), \Delta Eab(R-K, W-K), \Delta Eab(R-K, B-K), \Delta Eab(W-K, B-K))$

R ghosting: $\Delta E = \text{Max} (\Delta Eab(Y-R, R-R), \Delta Eab(Y-R, W-R), \Delta Eab(Y-R, B-R), \Delta Eab(R-R, W-R), \Delta Eab(R-R, B-R), \Delta Eab(W-R, B-R))$

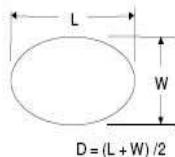
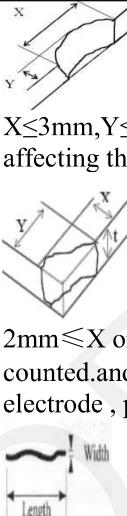
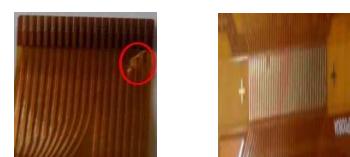
Y ghosting: $\Delta E = \text{Max} (\Delta Eab(Y-Y, R-Y), \Delta Eab(Y-Y, W-Y), \Delta Eab(Y-Y, B-Y), \Delta Eab(R-Y, W-Y), \Delta Eab(R-Y, B-Y), \Delta Eab(W-Y, B-Y))$

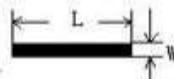
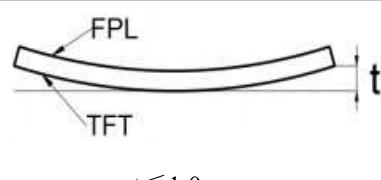
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA		
2	Black/White spots	 $D \leq 0.25\text{mm}$, Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$. $N \leq 4$ allowable $D > 0.4\text{mm}$ is not allowed	MI	Visual inspection	
3	Black/White lines (No switch)	 $L \leq 0.4\text{mm}, W \leq 0.1\text{mm}$ negligible $0.4\text{mm} < L \leq 1.0\text{mm}$ $0.1\text{mm} < W \leq 0.4\text{mm}$ $N \leq 4$ allowable $L > 1.0\text{mm}, W > 0.4\text{mm}$ is not allowed	MI	Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 $D \leq 0.25\text{mm}$ negligible $0.25\text{mm} < D \leq 0.4\text{mm}$ $N \leq 4$ allowable $D > 0.4\text{mm}$ is not allowed	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A
3	\Dirty	Allowed if can be removed	MI		Zone B
4	Chips/Scratch/ Edge crown	 $X \leq 3\text{mm}, Y \leq 0.5\text{mm}$ And without affecting the electrode is permissible $2\text{mm} \leq X$ or $2\text{mm} \leq Y$ $t = \text{not counted}$.and without affecting the electrode , permissible $W \leq 0.1\text{mm}, L \leq 5\text{mm}$, without affecting the electrode , $n \leq 2$	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	 Not Allow	MA	Visual / Microscope	Zone B

8	B/W Line	 <p> $L \leq 0.4\text{mm}$, $W \leq 0.1\text{mm}$ negligible $0.4\text{mm} < L \leq 1.0\text{mm}$ $0.1\text{mm} < W \leq 0.4\text{mm}$ $N \leq 4$ allowable $L > 1.0\text{mm}$, $W > 0.4\text{mm}$ is not allowed </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	<p>TFT edge bulge: $X \leq 3\text{mm}$, $Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed</p>	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	<p> $D \leq 0.2\text{mm}$, allow $0.2\text{mm} < D \leq 0.35\text{mm}$, $n \leq 4$ allow $D > 0.35\text{mm}$ is not allowed ($n \leq 5$ items are allowed within 5 mm in diameter) </p>	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	<p>PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$</p>	MI		
12	Edge glue height/ Edge glue bubble	<p>Edge Adhesives $H \leq PS$ surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 5.0\text{mm}$. $n \leq 5$</p>	MI	Visual / Ruler	Zone B
13	Protect film	<p>Surface scratch but not effect protect function, Allow</p>	MI	Visual Inspection	
14	Silicon glue	<p>Thickness $\leq PS$ surface(With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.</p>	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 <p> FPL TFT $t \leq 1.0\text{mm}$ </p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

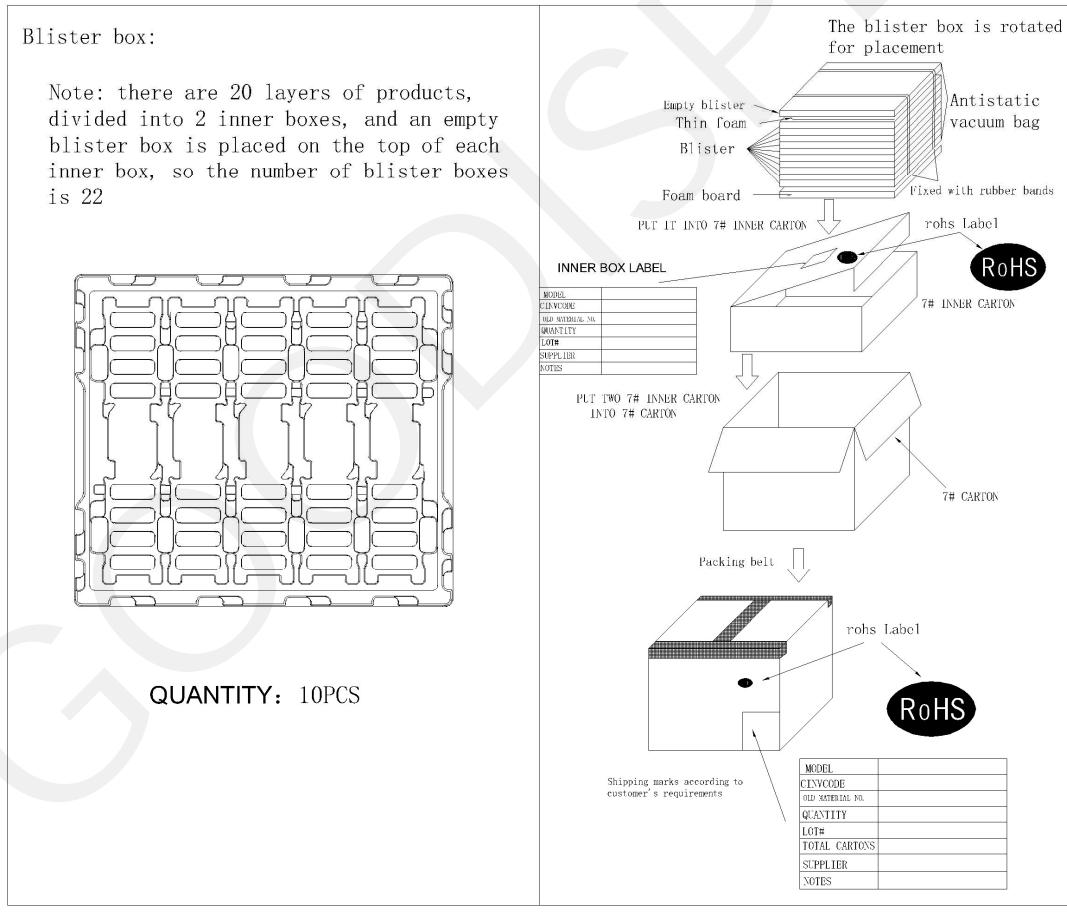
13.Packaging

PACKING INSTRUCTION

P/N	Customer Code	Ref. P/N	Type	PKG Method	Marking	Surface Marks	Pull Tape	
			GLASS	Blister	BACK	None	YES	

Packing Materials List					10PCS/LAYER, 20LAYER/CTN, TOTAL 200PCS/CTN.			
List	Model	Materials	Q'ty	Unit				
Carton	7# 417*362*229 mm	corrugate	1	Piece				
Inner Carton	7#(INNER) 400*343 *95 mm	corrugate	2	Piece				
Blister		PET	22	Piece				
Thin foam	305.61*257.18 T1.5-1.8MM	EPE	20	Piece				
Antistatic vacuum bag	450*590*0.075		2	Piece				
Foam board		EPE	3	Piece				
PULL TAPE	16*5*T0.05		200	Piece				

Detail:



14. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.

Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32 <https://www.good-display.com/product/219.html>

ESP32 <https://www.good-display.com/product/338.html>

ESP8266 <https://www.good-display.com/product/220.html>

Arduino UNO <https://www.good-display.com/product/222.html>

15. Handling, Safety and Environmental Requirements

WARNING

The display glass may break when it is dropped or bumped on a hard surface. Handle with care.

Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status

Product specification | The data sheet contains final product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).

Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification

RoHS

16. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.