HK32M063C Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinout of HK32M063C series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32M063C.

Audience

This document is intended for:

- HK32M063C developers
- HK32M063C testers
- HK32M063C users

Release Notes

This document is applicable to HK32M063C series MCUs.

Revision History

Version	Date	Description
1.0	2023/08/31	The initial release.

Contents

1 Introduction

This document is the datasheet for HK32M063C series MCUs. HK32M063C is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun) specifically for motors. This MCU family includes:

- HK32M063CK8U7 (QFN32 package)

For more details of HK32M063C, see *HK32M06x User Manual*.

2 Product overview

HK32M063C is a family of MCUs developed specifically for motors. It adopts the ARM® Cortex®-M0 core and incorporates the patented electric motor acceleration (EMACC) unit of Hangshun. The maximum operating frequency of HK32M063C can reach 48 MHz. Each HK32M063C MCU has 64 Kbytes of Flash and eight Kbytes of SRAM.

HK32M063C embeds a 5 V low dropout (LDO) regulator and a gate driver driving three sets of P&N-channel MOSFETs.

HK32M063C embeds a 16-bit advanced timer (three PWM output channels in total, which all have complementary PWM outputs with programmable inserted dead-times), a 32-bit general-purpose timer, a 16-bit general-purpose timer, and a 16-bit basic timer.

A simple RTC with the alarm function is embedded in HK32M063C. It can operate in low-power modes and provides wakeup sources for the MCU.

The analog circuitry embedded in HK32M063C includes a 12-bit ADC (simultaneous sample and hold by two sample and hold units, with up to eight external channels), three operational amplifiers (OPAMPs) that can operate in PGA mode, four voltage comparators (comparator threshold output from DAC), a power-on reset (POR)/power-down reset (PDR)/brown-out reset (BOR) circuitry, and an internal reference voltage (sampled by ADC on chip).

Except for the power pins, ground pins, NRST pin, high-side output pins, and low-side output pins, all the other pins of HK32M063C can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32M063C supports the conventional Flash read/write protection and also offers the patented Flash code encryption function of Hangshun.

HK32M063C incorporates several communication interfaces: two UART interfaces, a high-speed SPI, and an I2C interface.

HK32M063C also integrates the division and square root (DVSQ) calculation unit which provides higher performance than software and faster responses to external interrupts.

HK32M063C provides the Sleep and Stop low-power modes that can meet the requirements of power consumption-sensitive applications.

With the diversified peripherals, HK32M063C is best suited for the square wave control and field-oriented control (FOC) of brushless direct current (BLDC) motor and permanent magnet synchronous motor (PMSM):

- Electric tools
- Industrial fans
- Compressors
- Electric vehicles
- Range hoods
- Vacuum cleaners
- Water pumps
- Ceiling fans
- Air conditioners

2.1 Feature

- CPU core

- ARM® Cortex®-M0
- Maximum frequency: 48 MHz
- 24-bit SysTick timer

- Operating voltage range
  - Single power supply (main power supply V_M): 7 V to 28 V
    - V_M supplies power to the high-voltage domain.
    - V_M supplies power to the low-voltage domain after being processed by the 5 V LDO regulator.
- 5 V LDO regulator output
  - Input operating voltage range: 7 V to 28 V
  - Output voltage: 5 V; drive current: 100 mA
- Operating temperature range: –40°C to +105°C
- Memory
  - 64-Kbyte Flash
    - No wait states to access Flash when the CPU frequency is 24 MHz or lower
    - Separate read and write protection for Flash data
    - Encryption for instructions and data stored in the Flash, preventing the damage caused by physical attacks
  - 8-Kbyte SRAM
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz
  - High-speed internal clock (HSI): 8/12/48 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL output clock: 6 MHz to 48 MHz
  - GPIO external input clock: 5 MHz to 30 MHz
- Reset
  - External pin reset (NRST pin)
  - Option byte loading (OBL) reset
  - Window watchdog counting terminates (WWDG reset)
  - Independent watchdog counting terminates (IWDG reset)
  - Power reset (POR/PDR/BOR)
  - Software reset (SW Reset)
  - Low-power management reset
- GPIO
  - Provides up to 22 GPIOs
- 1 × DMA controller
  - With five channels for the selection of different request sources
  - Can be triggered by multiple peripherals such as the timer, SPI, I2C, UART, and ADC
- Data communication interfaces
  - 2 × UARTs
  - 1 × I2C

- 1 MHz/400 kHz/100 kHz transmission modes
- Wakes up the MCU from Stop mode when receiving data

◦ 1 × high-speed SPI

- Transmission rate at up to 18 Mbit/s

- Timer
  - ◦ 1 × 16-bit advanced timer: TIM1
    - Three PWM outputs with programmable inserted dead-times
    - Supports the break function triggered by signals output from external pins or internal comparators
    - The outputs of CC1 to CC6 can trigger ADC at multiple points in time.
  - ◦ 2 × general-purpose timers
    - 1 × 32-bit general-purpose timer: TIM2
    - 1 × 16-bit general-purpose timer: TIM3
  - ◦ 1 × 16-bit basic timer: TIM6
- Division and square root (DVSQ) calculation unit
  - ◦ Supports 32-bit fixed point division, with the quotient and remainder calculated
  - ◦ Supports 32-bit fixed point high-precision root calculation
- Electric motor acceleration (EMACC)
  - ◦ Supports the coordinate rotation digital computer (CORDIC) algorithm for sine and cosine
  - ◦ Supports Clarke, Park, and Inverse Park transformations
  - ◦ Supports space vector pulse width modulation (SVPWM)
  - ◦ Supports 1 × high-speed motor data transmission channel (Trace)
- Half-bridge gate driver driving three sets of P&N-channel MOSFETs
  - ◦ Three-phase gate driver
  - ◦ Over-temperature protection embedded
  - ◦ LDO shutdown protection embedded
  - ◦ Dead-time embedded
- On-chip analog circuitry
  - ◦ 1 × 12-bit SAR ADC with two sample and hold units (up to eight external analog input channels)
    - 12-bit resolution
    - Maximum frequency: 1.7 MSPS
    - Two independent sample and hold units, which can sample two signals simultaneously
    - Supports the conversion by four independent regular queues and a test queue
    - Supports automatic continuous conversion and scan conversion
    - Supports the channel replacement function of regular queues
    - Supports multiple hardware trigger sources (such as TIM1_TRGO, TIM1_CCx, and GPIO input events)
    - Supports the function of averaging the data of multiple channels in regular queues
    - Independent register for each channel to save data
  - ◦ Internal reference voltage

- The output of the internal reference voltage is connected to an independent ADC channel.

◦ 4 × voltage comparators (COMPs)

- The reference voltage of comparators is from the external signal input or internal 8-bit DAC.
- The output of comparators can be used as the break of the advanced timer.

◦ 3 × operational amplifiers (OPAMPs)

- Programmable amplification factor
- The output signal of amplifiers can be output to pins or an ADC sampling channel.

- 96-bit unique ID (UID) of each MCU
  - Used as the serial number and security key
  - Used to activate the secure boot process
- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Reliability
  - Passed HBM5500V/CDM2000V/LU250mA level tests.

2.2 Device overview

Table 2-1 HK32M063C series features

Feature		HK32M063CK8U7
GPIO		22
Package		QFN32
Operating voltage		7 V – 28 V
Operating temperature		–40°C to +105°C
Memory	Flash (Kbyte)	64
	SRAM (Kbyte)	8
CPU	Core	Cortex®-M0
	Frequency	48 MHz
DMA (channels)		1 (5 channels)
Division and square root (DVSQ) calculation unit		1
Clock	LSI	40 kHz
	HSI	8 MHz/12 MHz/48 MHz
	PLL clock	Supported
	HSE	4 MHz – 32 MHz
	PLL output clock	6 MHz – 48 MHz
	GPIO input clock	5 MHz – 30 MHz
Timer	Advanced timer	1 (16-bit): TIM1
	General-purpose timer	1 (32-bit): TIM2 1 (16-bit): TIM3
	Basic timer	1 (16-bit): TIM6
	Simple RTC	An independent 32-bit counter (can operate in low-power modes)
	SysTick timer	1
	IWDG	1

Feature		HK32M063CK8U7
	WWDG	1
Communication peripheral	UART	2
	I2C	1
	SPI	1
ADC	ADC (external analog channels)	1 (8)
	Reference selection	Internal reference voltage
	ADC conversion frequency	1.7 MSPS
	ADC accuracy	12-bit
P&N-channel MOSFET gate driver		Three half bridges, driving three P-channel power MOSFETs and three N-channel power MOSFETs
Voltage comparator (COMP)		4
Operational amplifier (OPAMP)		3
EMACC		1
96-bit UID		1

3 Function description

3.1 Block diagram

HK32M063C integrates a Flash memory of 64 Kbytes to store programs and data.

ARM® Cortex®-M0 is a 32-bit RISC processor, which delivers outstanding computational performance and advanced system responses to interrupts. With the ARM® Cortex®-M0 core embedded, the HK32M063C family is compatible with all ARM tools and software.

The following figure shows the block diagram of HK32M063CK8U7:

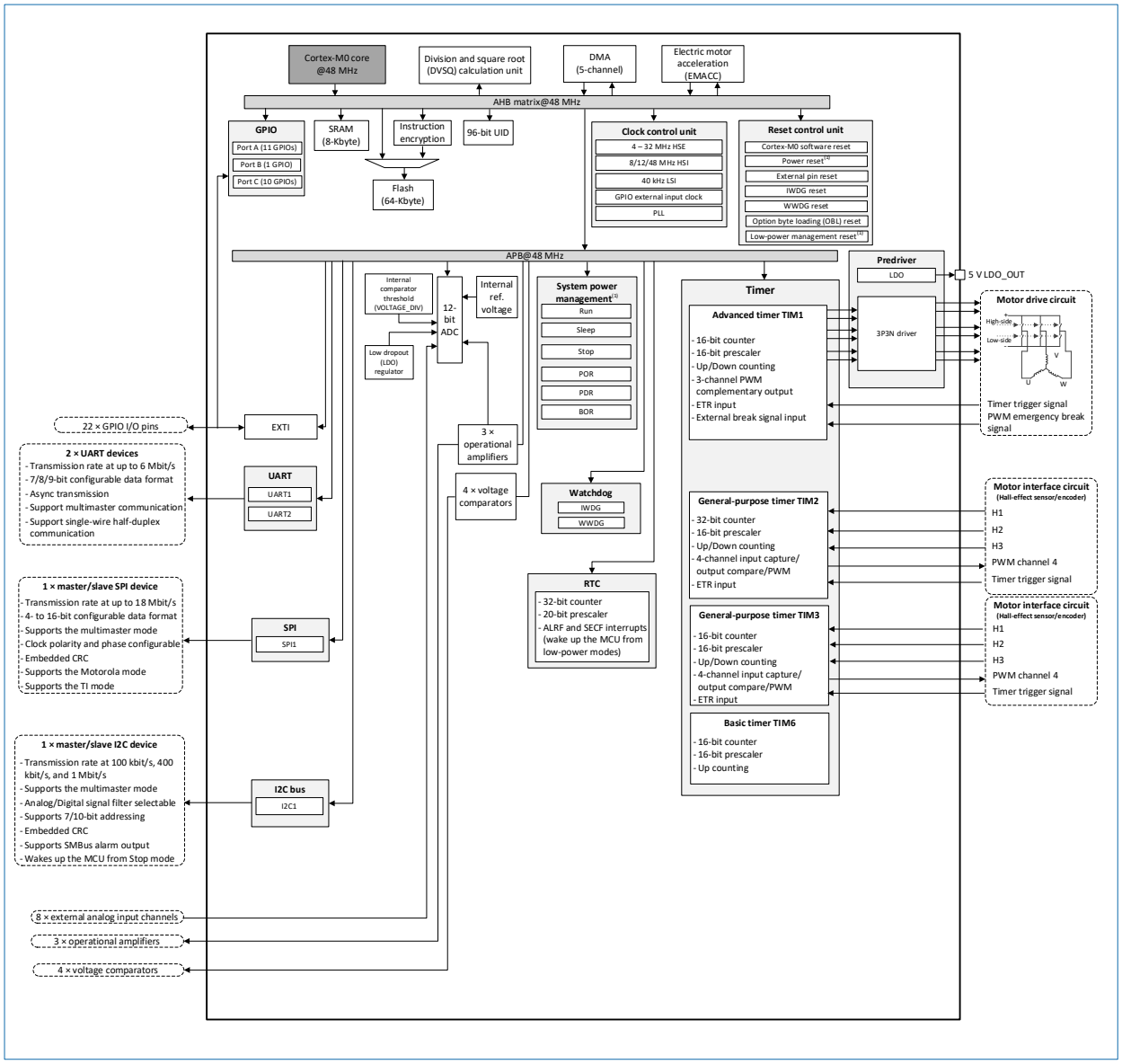

Figure 3-1 HK32M063CK8U7 block diagram

Note of Figure 3-1*:*

(1). HK32M063C is supplied by a high voltage. Therefore, it is recommended that you do not use functions such as system power management, power reset, and low-power management reset that are designed for MCUs supplied by a low voltage.

3.2 Memory mapping

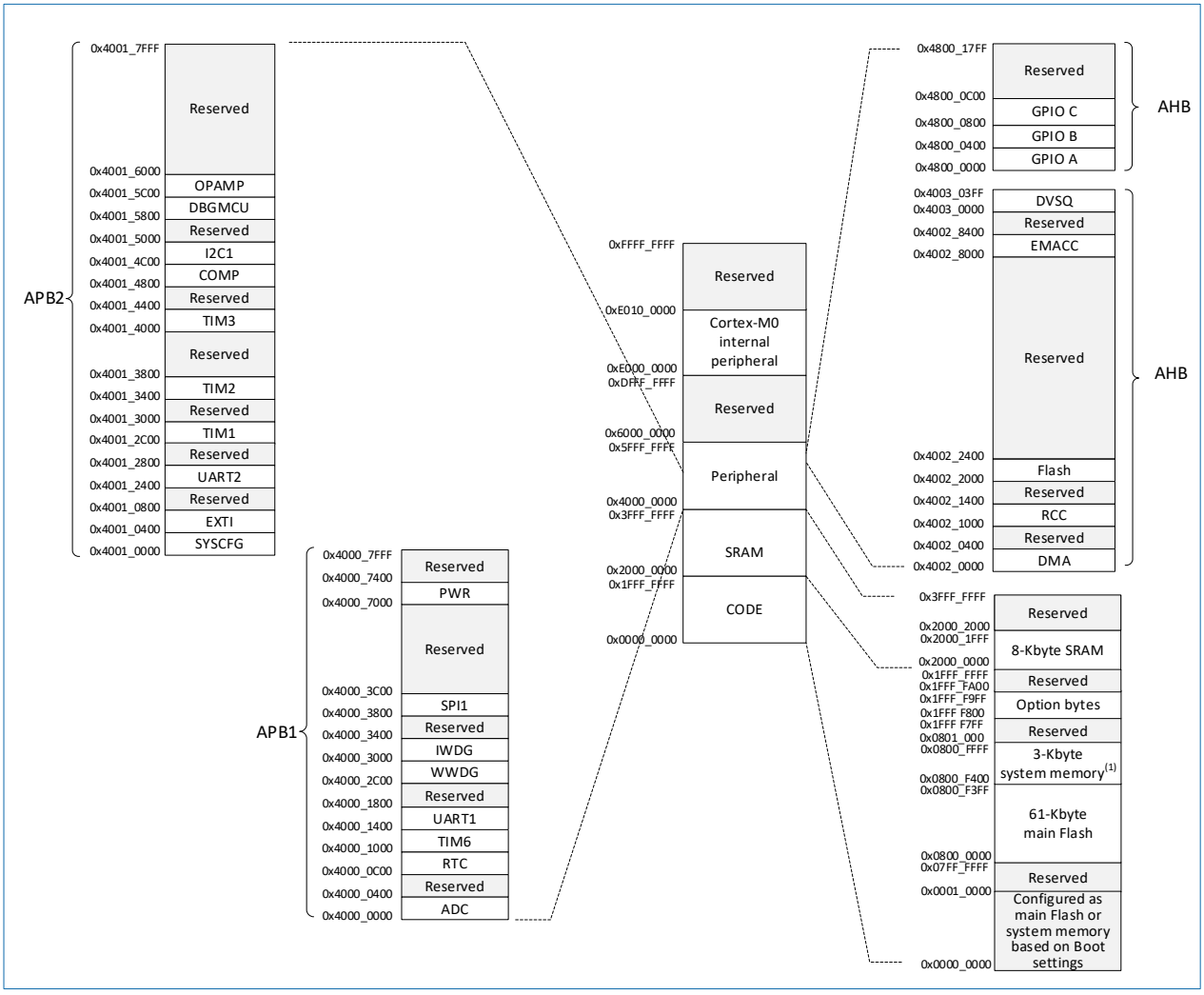

Figure 3-2 HK32M063CK8U7 memory mapping

Note of Figure 3-2*:*

(1). The 64-Kbyte Flash comprises 61-Kbyte main Flash and 3-Kbyte system memory. The 3-Kbyte system memory can also be used to store user code. If the 3-Kbyte system memory is reserved, only the 61-Kbyte main Flash can be used to store programs and data.

3.3 Memory

3.3.1 Flash

HK32M063C integrates a Flash memory of 64 Kbytes to store programs and data. The 64-Kbyte Flash comprises 61-Kbyte main Flash and 3-Kbyte system memory. The 3-Kbyte system memory can also be used to store user code.

You can configure the Flash controller register to remap interrupt vectors in the 64-Kbyte space.

3.3.2 SRAM

HK32M063C integrates an 8-Kbyte SRAM that can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.4 Power supply scheme

- V_M = 7 V to 28 V. The input operating voltage is from 7 V to 28 V, with LDO shutdown protection embedded. It supplies power to the internal 5 V LDO regulator and three-channel gate driver.
- $V_{LDO05}/V_{DD}/V_{DDA}$ = 4.5 V to 5.5 V. The output of the internal 5 V LDO regulator supplies power to the low-

power domain of the MCU, with over-temperature protection embedded, as shown in Figure 5-1.

- V_{REFP} = 2.2 V to 5.5 V. V_{REFP} supplies power to the analog circuitry, such as the ADC, voltage comparators, and operational amplifiers.

Note: V_{REFP} is an independent pin.

3.5 Reset

3.5.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR. You can identify the reset source by checking reset status flags in the RCC_CSR register.

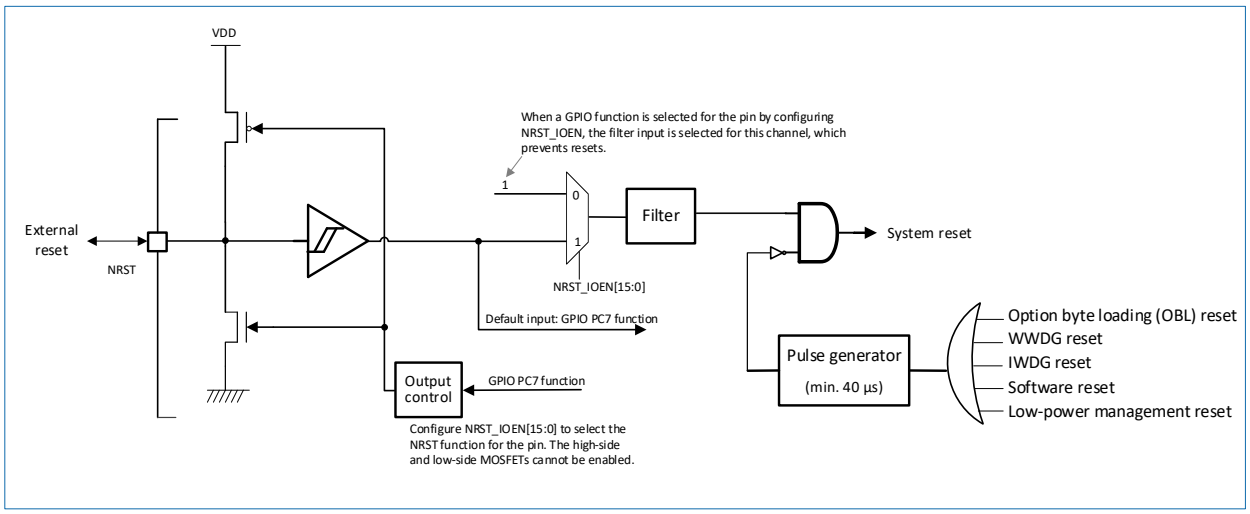

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Option byte loading (OBL) reset
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset

The reset sources of other resets eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset entry vector is fixed on address 0x00000004. The internal reset signals (except for the power reset) are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.6 Clocks and clock tree

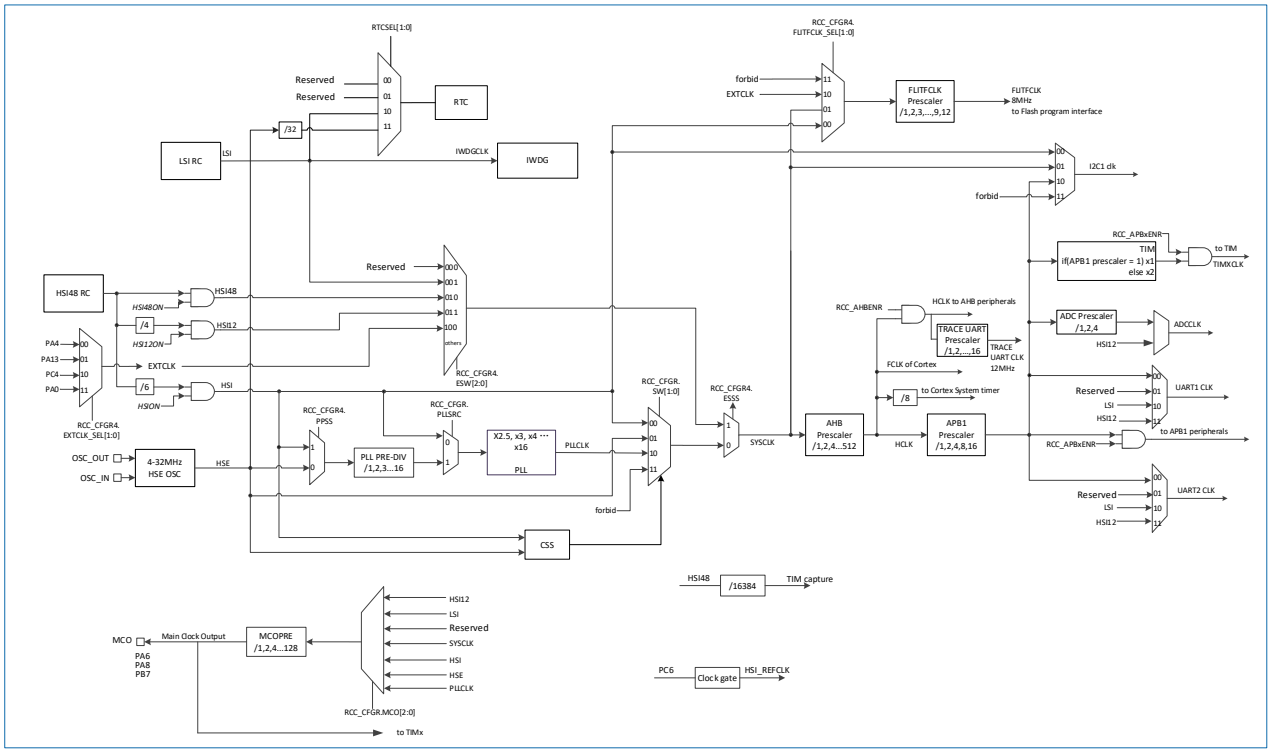

Figure 3-4 Clock tree

Note of Figure 3-4:

(1). LSE is not available in HK32M063C.

As the figure shows, HSI48 and ADCCLK are generated by the same internal oscillator operating at 48 MHz. Therefore, when HSI48 or ADCCLK is used, disabling the other clock cannot reduce power consumption.

HK32M063C MCUs use SYSCLK as the CPU clock when they start. The internal oscillator outputs a 48 MHz clock. The HSI divided from this 48 MHz clock is used as the default system clock when the MCU is powered on. HSI/HSE can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI/HSE together with PLL to configure different system clock frequencies.

HK32M063C provides more clock sources for the system clock and offers convenient, flexible, and diverse operating modes to customers. The following clocks can act as the system clock:

- High-speed external clock (HSE): 4 MHz to 32 MHz
- High-speed internal clock (HSI): 8/12/48 MHz
- Low-speed internal clock (LSI): 40 kHz
- PLL clock: 48 MHz (maximum value)
- GPIO external input clock: 5 MHz to 30 MHz

The clock frequency of the AHB and the APB domain can be configured by using several prescalers. The maximum clock frequency of the AHB can be 48 MHz. The maximum clock frequency of the APB domain can be 48 MHz.

The clock security system (CSS) supervises the HSE and switches to another clock source when it detects faults.

3.7 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by the digital and analog alternate functions. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed by performing a specific operation, which helps avoid unexpected writes to the I/O registers.

3.8 SYSCFG

The HK32M063C MCU has a set of system configuration registers. SYSCFG provides the following functions:

- Enable or disable fast mode plus of I2C on some I/O ports.
- Remap the memory areas.
- Manage external interrupts connected to the GPIOs.
- Manage the remapping of LSI and HSI signals to TIM3_CH4.
- Manage the switch of controlling the output of some internal analog signals to I/Os.
- Configure the internal voltage divider (8-bit DAC).

3.9 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from Flash memory
- Boot from system memory

The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the UART1 (PC8/PC9) interface.

3.10 DMA

The direct memory access (DMA) controller is used for high-speed data transfer from peripherals to memory and from memory to memory. DMA can quickly move data to the destination without CPU intervention, saving CPU resources for other applications.

HK32M063C integrates a DMA controller which is used to manage the access requests from one or more peripherals. The DMA controller has an arbiter to handle the priorities of different DMA requests.

- Provides five configurable independent channels.
- Each channel is connected to dedicated hardware and triggered by the hardware. The software trigger is also supported.
- Supports circular buffer management.
- TIM1/2/3, SPI1, UART1/2, I2C1, and ADC can generate DMA requests.

3.11 Interrupts and events

3.11.1 NVIC

HK32M063C incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 22 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities while maintaining the lowest interrupt latency.

- The closely coupled NVIC ensures low latency in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

3.11.2 EXTI

The extended interrupt/event controller (EXTI) manages asynchronous interrupts and events. It outputs event requests to the CPU, outputs interrupt requests to the interrupt controller, and outputs wakeup requests to the power supply management module.

EXTI can be categorized into edge-configurable EXTI and edge-fixed EXTI. For the edge-fixed EXTI, only the rising edge is the trigger edge. The EXTI only operates in Stop mode and is used to wake up the core from Stop mode.

- Manages up to 22 interrupt/event requests.
  - 22 configurable EXTI lines.
    - The trigger edge is configurable (the rising edge or falling edge).
    - The dedicated flag for the interrupt status bit.
    - Interrupts and events can be triggered by software.
  - One fixed EXTI line.
- Each interrupt/event line can be triggered and masked independently.
- Detects external signals whose pulse width is shorter than the APB2 clock period.

3.12 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator (LSI). The RC oscillator is independent of the main clock, so it can operate in Stop mode. The IWDG can reset the system when a problem occurs or work as a free-running timer to provide timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use IWDG in window mode.

3.13 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.14 Timers

The HK32M063C MCU has an advanced timer, two general-purpose timers, and a basic timer. The following table describes the features of timers.

Table 3-1 Functions of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	1 to 65536	Yes	Yes	No	3
General-purpose timer	TIM2	32-bit	Up, down, up/down	1 to 65536	Yes	No	4	No
	TIM3	16-bit	Up, down, up/down	1 to 65536	Yes	No	4	No
Basic timer	TIM6	16-bit	Up	1 to 65536	No	No	No	No

3.14.1 Advanced timer

HK32M063C integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The three independent channels of TIM1 can be used for:

- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output
- The three channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a 16-bit timer, it has the same functions as a basic timer. If TIM1 is configured as a 16-bit PWM generator, it has full modulation capability (0–100%). Many functions of TIM1 are the same as those of general-purpose timers. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

The advanced timer provides the update event shifting function and simple data migration function which can be adopted in motor control.

In debug mode, the counter can be frozen.

3.14.2 General-purpose timer

HK32M063C integrates two general-purpose timers.

- TIM2 and TIM3

TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have four independent channels respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output.

TIM2 and TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

3.14.3 Basic timer

HK32M063C integrates a basic timer TIM6.

TIM6 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. In debug mode, the counter can be frozen.

3.14.4 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.15 ADC

HK32M063C incorporates a 12-bit analog-to-digital converter (ADC) which has a total of eight external channels and six internal channels. The A/D conversions of the channels can be performed in single, continuous, scan, or discontinuous mode.

- 12-bit resolution
- The maximum ADC clock frequency is 24 MHz, and the maximum ADC conversion frequency is 1.7 MSPS.

- Two independent sample and hold units whose inputs are from the 12 analog input channels
- The ADC can be served by the DMA controller.
- Flexible queue configuration: four independent regular queues and a test queue
- The queue operating modes include single-sample and hold, dual-sample and hold, single-sample and hold scan, and BK modes.
- Flexible arbitration mechanism: a priority from 0 to 3 for each queue. A larger number indicates a higher priority.
- Independent register for each channel to store the conversion result
- Channels can be changed: The conversion request of a channel can be redirected to another channel. This feature can be used to test the inputs to the same channel and save the conversion results to different registers.
- The data window comparison function enables the ADC conversion results to be compared with the preset values.
- The data averaging function performs data pre-processing.
- Supports the configuration of trigger latency. The ADC conversion starts after the latency elapsed from when the trigger signal is generated.
- The events generated by advanced timer (TIM1) and general-purpose timers (TIM2/TIM3) can be internally connected to the ADC start trigger to trigger A/D conversions.

3.15.1 Internal reference voltage

The internal reference voltage V_{REFINT} provides a stable voltage output (bandgap voltage reference) for the ADC.

3.16 COMP

HK32M063C has four built-in voltage comparators (COMPs): COMP1, COMP2, COMP3, and COMP4. The four comparators can be used independently or used with timers.

The four comparators can be used:

- To wake up the MCU from low-power modes after being triggered by the analog signal.
- For analog signal conditioning.
- Together with the timer PWM output to form the cycle-by-cycle current control loop.

3.17 OPAMP

HK32M063C integrates three operational amplifiers (OPAMPs). They can operate in Standalone, Follower, and PGA modes.

The outputs of OPAMPs can be output to pins, internally connected to the inverting input node, or strobed in the internal ADC for sampling.

3.18 EMACC

Electric motor acceleration (EMACC) can be used on brushless direct current (BLDC) motors controlled by the field-oriented control (FOC) algorithm. EMACC accelerates the mathematical operations of motor drives. Mathematical operations can be completed at a speed higher than that of software-based mathematical operations while occupying less CPU resources. The EMACC-embedded MCUs support higher motor rotation speeds and improved drive frequencies under the same CPU frequency.

On HK32M063C MCUs, the coordinate rotation digital computer (CORDIC) algorithm, Clarke, Park, and Inverse Park transformations, proportional-integral-derivative (PID) control, and space vector pulse width modulation (SVPWM) module of the FOC algorithm are based on hardware. This helps free up CPU resources and speed up

computing. Users input Ia, Ib, and the θ electrical angle. After the processing by EMACC, the output of SVPWM, such as the PWM duty cycle of A, B, and C phases, can be obtained. EMACC further decreases the time consumed by the FOC algorithm.

HK32M063C contains a data tracker (EMACC_TRACE) which is a hardware high-speed serial interface module. During the motor commissioning or high-speed running process, EMACC_TRACE outputs EMACC parameters in real time. In addition, four bytes are provided for the output of user-defined data, which facilitates motor commissioning.

EMACC can significantly increase algorithm efficiency.

3.19 P&N-channel MOSFET gate driver (Predriver)

Three half bridges drive three P-channel power MOSFETs and three N-channel power MOSFETs. Each MOSFET output is controlled by a corresponding logic input signal. The logic input signal is controlled by TIM1. The dead-time and shoot-through protection embedded in the driver prevent the high-side and low-side power MOSFETs from being switched on concurrently.

3.20 DVSQ

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - Supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports divide-by-zero interrupt and overflow interrupt.

3.21 I2C bus

HK32M063C has an I2C bus interface that can work in multimaster mode or slave mode. The I2C interface supports the standard mode (up to 100 kHz), fast mode (up to 400 kHz), and fast mode plus (up to 1 MHz).

The I2C interface provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, host notify protocol, hardware CRC (PEC) generation and verification, timeout verification, and ALERT protocol management.

The I2C interface has a clock independent of the CPU clock domain, so it can wake up the MCU from Stop mode when the address is matched.

Table 3-2 I2C features

I2C Feature	I2C1
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast/Fast mode plus	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
DMA transmission	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

3.22 UART

Two UARTs (UART1/UART2) are embedded in the HK32M063C MCU. They can communicate at up to 6 Mbit/s. The UARTs provide hardware management of the RS485 DE signals, multiprocessor communication mode, and single-wire half-duplex communication mode. The UARTs can be served by the DMA controller.

Table 3-3 UART features

UART Mode/Feature	UART1/UART2
Data word length	7/8/9-bit
DMA transmission	Supported
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported
RS232 hardware flow control	No supported
RS485 driver enable	Supported

3.23 SPI

One serial peripheral interface (SPI) is embedded in each HK32M063C MCU. The SPI interface supports full-duplex and half-duplex communication in master or slave mode. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4-bit to 16-bit.

Table 3-4 SPI features

SPI Feature	SPI1
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported
DMA transmission	Supported
I2S	Not supported

3.24 RTC

The real-time clock (RTC) has a set of continuously running counters and can provide the clock function via software. In addition, the RTC provides the alarm interrupt and seconds interrupt which can be the wakeup sources in Stop mode.

The RTC can be clocked by HSE/32 or LSI. Its 32-bit programmable counter can work with the alarm register to realize long-term measurement and generate alarm events.

3.25 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32M063C MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process of the security mechanism.

3.26 Debug port (DBG)

Based on the ARM SWJ-DP embedded in HK32M063C, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_M - V_{SS}$	External main supply voltage	–0.3	28	V
$\lvert V_{SSX} - V_{SS} \rvert$	Variation between different ground pins	-	50	mV
V_{LDO05}	LDO output voltage	4.5	5.5	V
V_{HO}	High side drive output voltage	V_M – 15	V_M	V
V_{LO}	Low side drive output voltage	–0.3	15	V
P_{DMAX}	Package loss	1.4	-	W
θ_{JA}	Junction-to-ambient thermal resistance	89	-	°C/W
θ_{JC}	Junction-to-case thermal resistance	40	-	°C/W

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VLDO05}	Total current into V_{LDO05} (source)(1)	110	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	110	
I_{IO}	Output current sunk by any I/O and control pin	60	
	Output current sourced by any I/O and control pin	60	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_M) and ground (V_{SS}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_M, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–55	130	°C
T_J	Maximum junction temperature	–55	130	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	48	

Symbol	Description	Min	Max	Unit
f_{PCLK2}	Internal APB2 clock frequency	-	48	
V_M	MCU operating power supply input	7	28	V
V_{REFP}(1)	Analog operating voltage	2.2	5.5	V
T	Operating temperature	–40	105	°C

4.2.2 5 V LDO characteristics

Table 4-5 5 V LDO static electrical characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{M_ON}	V_M UVLO release voltage	-	7.0	7.5	8.0	V
V_{M_UVLO}	V_M UVLO voltage	-	6.6	7.1	7.6	
V_{M_HYS}	V_M UVLO hysteresis voltage	-	0.4			
I_{QVM}	V_M static current	VIN = 0 V	-	360	-	μA
V_{LDO05}	LDO voltage	-	4.5	5	5.5	V
I_{V05LM}	LDO output current limits	-	63	100	140	mA

4.2.3 Internal reference voltage

Table 4-6 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	-	0.8	-	V

4.2.4 HSE clock characteristics

Table 4-7 HSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
R_F(1)	Feedback resistor	-	-	1.1	-	MΩ
$T_{stb\ (HSE)}$(2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	0.7	1.8	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (R_S)		-	12	-	pF
$I_{DD\ (HSE)}$(1)	HSE oscillator power consumption	Normal operation: V_{DD} = 5 V, CL = 12 pF	-	400	-	μA

(1) The value is guaranteed in design;

(2) $T_{stb\ (HSE)}$ refers to the time from HSE startup to the time when it outputs stable frequency signals.

HK32M063C integrates an HSE negative feedback circuit supplied with a crystal resonator. The following oscillator circuit outside the chip is recommended:

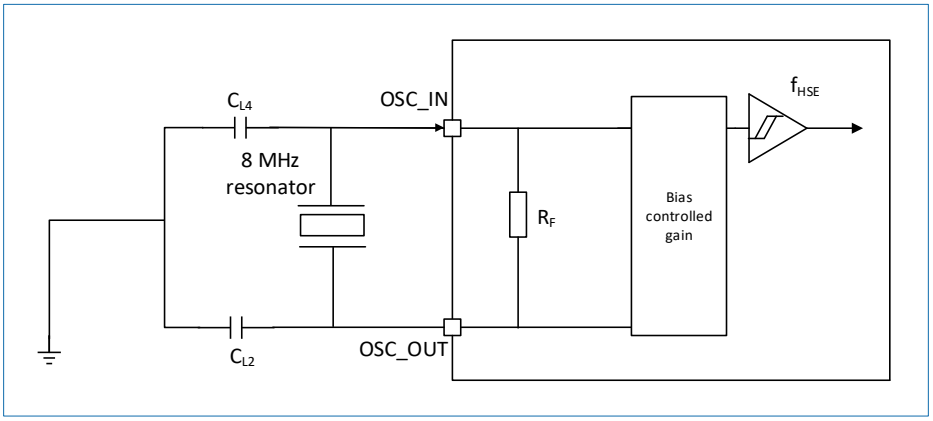

Figure 4-1 HSE negative feedback circuit

Alternatively, HK32M063C can be clocked from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-8 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	4	-	32	MHz
$DuCy_{(HSE)}$(1)	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.5 HSI clock characteristics

Table 4-9 HSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	48	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-	45	50	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	–1	-	1	%
		Factory calibration: T_A = –40°C to +105°C	–1.3	-	1.0	
$T_{stb\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_M$	-	8	11	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	48 MHz, V_{DD} = 5 V	-	115	145	µA

(1). The value is guaranteed in design.

4.2.6 LSI clock characteristics

Table 4-10 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	40	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	50	150	µs
$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	250	-	nA

(1). The value is guaranteed in design.

4.2.7 PLL characteristics

Table 4-11 PLL characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	-	48	MHz
	Input clock duty cycle	45	50	55	%
f_{PLL_OUT}	Output clock frequency	6	-	48	MHz
t_{LOCK}	PLL lock time	-	60	150	µs

(1). The values are guaranteed in design.

4.2.8 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-word programming time	62	62	102	µs
T_{ERASE}	Page erase time	100	100	200	ms
	Mass erase time	100	100	200	ms
I_{DDPROG}	One-word programming current	-	-	8	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	9	mA
I_{DDREAD}	Read current@25 MHz	-		3	mA
N_{END}	Erasure endurance	100	-	-	Thousand cycles
t_{RET}	Data retention	10	-	-	Years

4.2.9 I/O pin input characteristics

Table 4-13 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 5 V	0.65 × V_{DD}	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 5 V	-	-	0.2 × V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD} = 5 V	0.65 × V_{DD}	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 5 V	-	-	0.2 × V_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 5 V	-	-	0.2 × V_{DD}	mV
I_{lkg}	Input leakage current	V_{DD} = 5 V; 0 < V_{IN} < 5 V	-	5	-	nA
		V_{DD} = 5 V; V_{IN} = 5 V	-	5	-	nA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	33	-	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The value is guaranteed in design.

4.2.10 I/O pin output characteristics

Table 4-14 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}	-	-	V
V_{OL}	Output low level voltage	2.4 V ≤ V_{DD} ≤ 5.5 V	-	-	0.2 × V_{DD}	V

4.2.11 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-15 NRST pin input characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{Noise}	Low level ignored duration	-	-	80	ns

4.2.12 TIM timer characteristics

Table 4-16 TIM1 characteristics(1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH3	-	$f_{TIMxCLK}$/2	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 48 MHz.

Table 4-17 TIM2/3 characteristics(1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	-	$f_{TIMxCLK}$/2	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 48 MHz.

4.2.13 EMACC characteristics

Table 4-18 Motor drive carrier frequency characteristics

System Clock	ADC Clock	Min	Typ	Max	Unit
48 MHz	f_{ADC} = f_{PCLK}/2	-	12	16	kHz

Table 4-19 Comparison between the software and the FOC algorithm with EMACC

Test Condition	Electrical Angle	Coordinate System Conversion	SVPWM	Total Time Consumption	Unit
System clock: 48 MHz (software-based motor library)	16.7	14	6.9	41.6	μs
System clock: 48 MHz (EMACC-powered motor library)	16.7	2.4	3.6	26.8	μs

4.2.14 P&N-channel MOSFET gate driver (Predriver) characteristics

Table 4-20 P&N-channel MOSFET gate driver (Predriver) characteristics

Parameter		Description	Condition	Min	Typ	Max	Unit
Static electrical characteristics	V_{OH}	High-level output voltage	H_{IN} = 5 V	V_M – 11	V_M – 9.5	V_M – 8	V
	V_{OL}	Low-level output voltage	L_{IN} = 5 V	8.5	10	11.5	V
	I_{HO+}	Maximum HOx sink current	H_O = V_M	-	60	-	mA
	I_{HO-}	Maximum HOx source current	H_O = V_M – 10 V	-	195	-	mA
	I_{LO+}	Maximum LOx sink current	H_O = 0 V	-	100	-	mA
	I_{LO-}	Maximum LOx source current	H_O = 10 V	-	80	-	mA
	T_{SD}	Over-temperature protection trigger threshold	-	140	160	180	℃
	$T_{RECOVER}$	Over-temperature protection cancel threshold	-	120	140	160	℃
Dynamic electrical characteristics(1) (CL = 1 nF)	t_{on}	Turn-on propagation delay	-	-	120	-	ns
	t_{off}	Turn-off propagation delay	-	-	40	-	
	t_{Hr}	High-side MOSFET output rise time	-	-	60	-	
	t_{Hf}	High-side MOSFET output fall time	-	-	290	-	
	t_{Lr}	Low-side MOSFET output rise time	-	-	240	-	
	t_{Lf}	Low-side MOSFET output fall time	-	-	60	-	
	DT	Dead-time	-	-	100	-	

(1). The dynamic propagation time varies based on the parasitic parameters of peripheral traces. The values provided here are for reference only.

4.2.15 ADC characteristics

Table 4-21 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage when ADC is enabled	-	2.0	5	5.5	V
V_{REFP}	Positive reference voltage	-	2.0	5	5.5	V
V_{REFN}	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	12	24	MHz
f_S (1)	Sampling frequency	f_{ADC} = 12 MHz	-	0.857	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	V_{REFN}	-	V_{REFP}	V
R_{AIN}(1)	External input impedance	For details, see Table 4-22.				kΩ
R_{ADC}(1)	Sampling switch resistance	-	-	-	2	kΩ
C_{ADC}(1)	Sample and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S(1)	Sampling time	f_{ADC} = 12 MHz	1.5	-	239.5	Cycles
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz; 12-bit resolution	14	-	252	Cycles

(1). The value is guaranteed in design.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f}_{ADC} \times \boldsymbol{C}_{ADC} \times \ln(2^{N+2})} - \boldsymbol{R}_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-22 Maximum input impedance values (f_{ADC} = 12 MHz)

Sampling Cycles Ts (Cycles)	Sampling Time tS (μs)	Maximum Input Impedance (kΩ)
1.5	0.125	0.577
7.5	1.6	10.8
13.5	1.125	21.1
28.5	2.375	46.9
41.5	3.458	69.3
55.5	4.625	93.3
71.5	5.958	120.8
239.5	19.958	409.5

Table 4-23 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	V_{DD} = V_{REFP} = 5 V; f_{ADC} = 12 MHz	-	13	LSB
EO	Offset error(2)		-	3	
EG	Gain error(3)		-	5	
ED	Differential linearity error(4)		-	2	
EL	Integral linearity error(5)		-	3	

(1) Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2) Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3) Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4) Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5) Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With restricted V_{DDA}, frequency, and temperature ranges, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

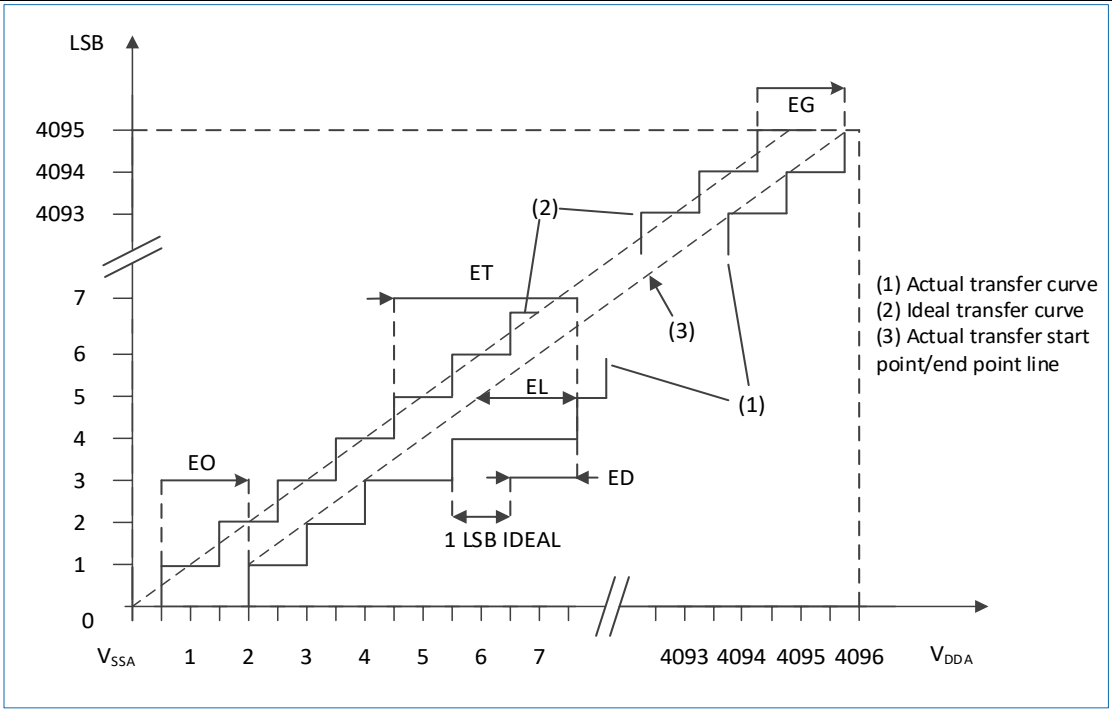

Figure 4-2 ADC accuracy characteristics

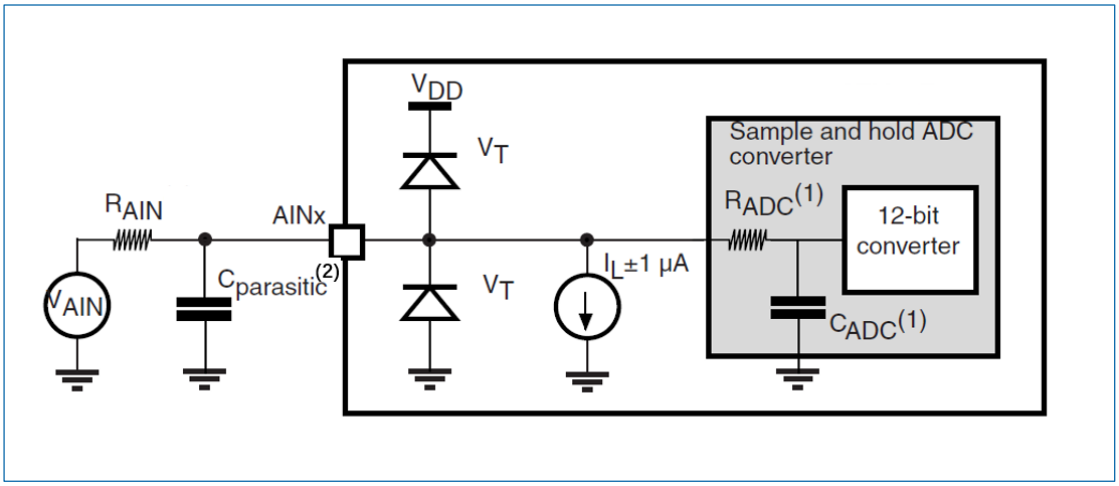

Figure 4-3 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-21.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

4.2.16 DAC voltage divider characteristics

Table 4-24 DAC voltage divider characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage when DAC is enabled	-		5	5.5	V
R_O	Output impedance	DAC buffer enabled	-	7	-	kΩ
I_{OUT}(1)	Output current	DAC buffer enabled	-	-	2	mA

(1). The value is guaranteed in design.

4.2.17 COMP characteristics

Table 4-25 COMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage	-	4.5	5	5.5	V
V_{com}	Input common mode voltage	-	0.2	-	5.3	V
V_{diff}	Input differential mode voltage	Low-power (low-speed) mode	-	-	40	mV
		High-power (high-speed) mode	-	-	10.5	
V_{hy}	Hysteresis voltage	Level 1	-	0	-	mV
		Level 2	-	10	-	
		Level 3	-	20	-	
I_{OP}	Operating current (V_{DD} = 5 V, static power consumption)	Low-power (low-speed) mode	1.405	2.81	3.74	µA
		High-power (high-speed) mode	22.2	38.55	42.42	
T_{dly}(1)	Output delay (no hysteresis)	High-power (high-speed) mode Rising edge	28.67	42.81	79	ns
		Low-power (low-speed) mode Rising edge	142.3	287.4	753.4	
		High-power (high-speed) mode Falling edge	30.62	57.8	72.13	
		Low-power (low-speed) mode Falling edge	206.5	597.2	849.8	

(1) The value is guaranteed in design.

4.2.18 OPAMP characteristics

Table 4-26 OPAMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	4.5	5	5.5	V
V_{OUT}	Output voltage	-	0.2	-	V_{DDA} – 0.2	V
CMIR	Input common mode voltage	-	0	-	5.5	V
I_{bias}(1)	Input bias current	-	0.8	1	1.2	µA
I_{load}	Output current	R_L = 100 Ω, V_{DD} = 5 V	-	6	-	mA
I_q	Operating current	Static mode	-	-	1100	µA
I_l(1)	Leakage current	OPAMP disabled	-	2.00	170.00	nA
V_{OS}	Input bias voltage	Before calibration	-	±15	-	mV
		After calibration	-	±2.5	-	mV
CMRR(1)	Common mode rejection ratio	-	51	-	145	dB
PSRR(1)	Power supply rejection ratio	-	41	70	109.4	dB
UGF	Unity-gain bandwidth	-	-	6	6.4	MHz
SR	Slew rate	(5% – 95%) rising	5.213	6.251	8.061	V/µs
		(5% – 95%) falling	5.278	6.571	8.679	
ϕ	Phase margin	-	47.09	70.93	84.58	Deg
PGA gain	PGA gain	Level 1	-	1	-	times
		Level 2	-	2	-	
		Level 3	-	5	-	
		Level 4	-	8	-	
		Level 5	-	10	-	
		Level 6	-	14	-	
		Level 7	-	16	-	
		Level 8	-	20	-	

(1) The value is guaranteed in design.

5 Typical circuitry

5.1 Power supply scheme

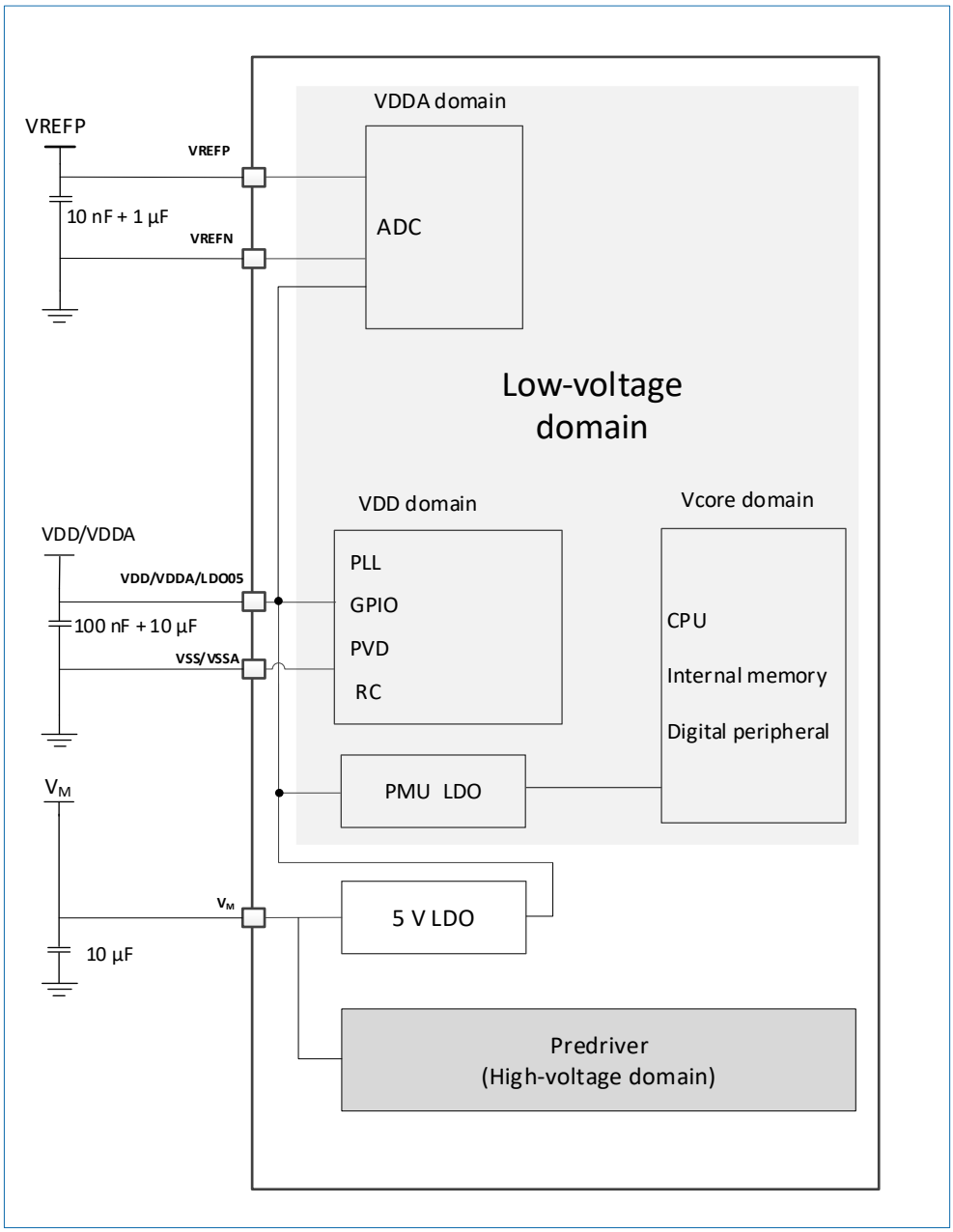

Figure 5-1 Power supply block diagram

5.2 Typical application

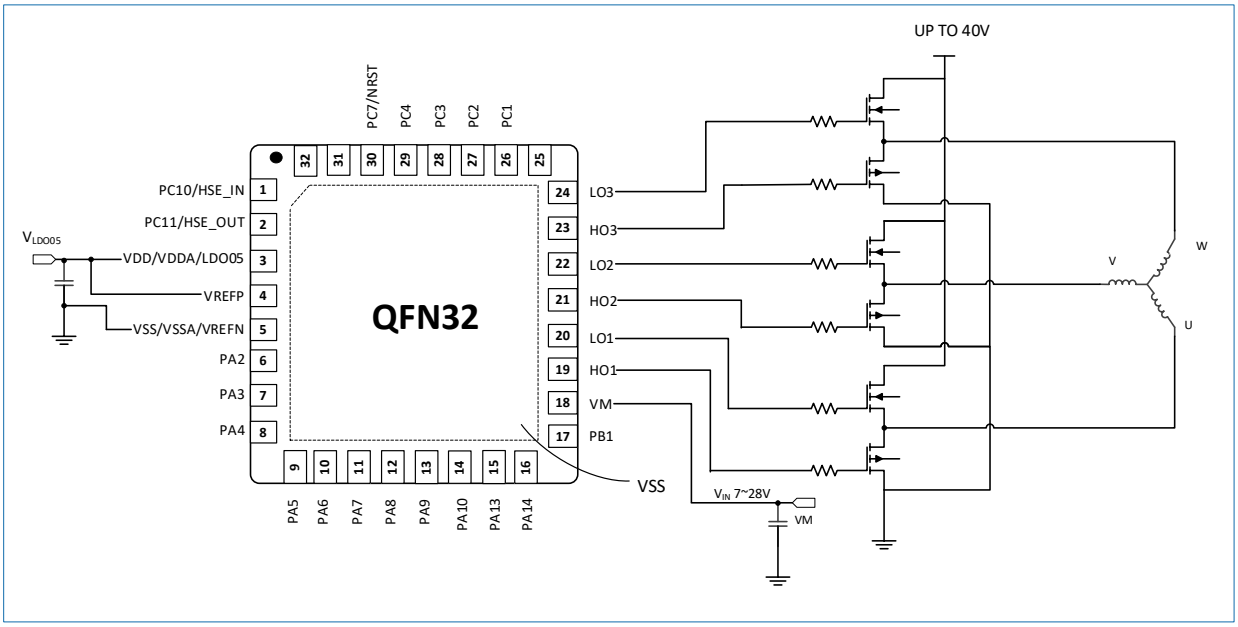

Figure 5-2 Typical application block diagram

6 Pinout and pin description

HK32M063C MCUs are delivered in the QFN32 package.

6.1 QFN32

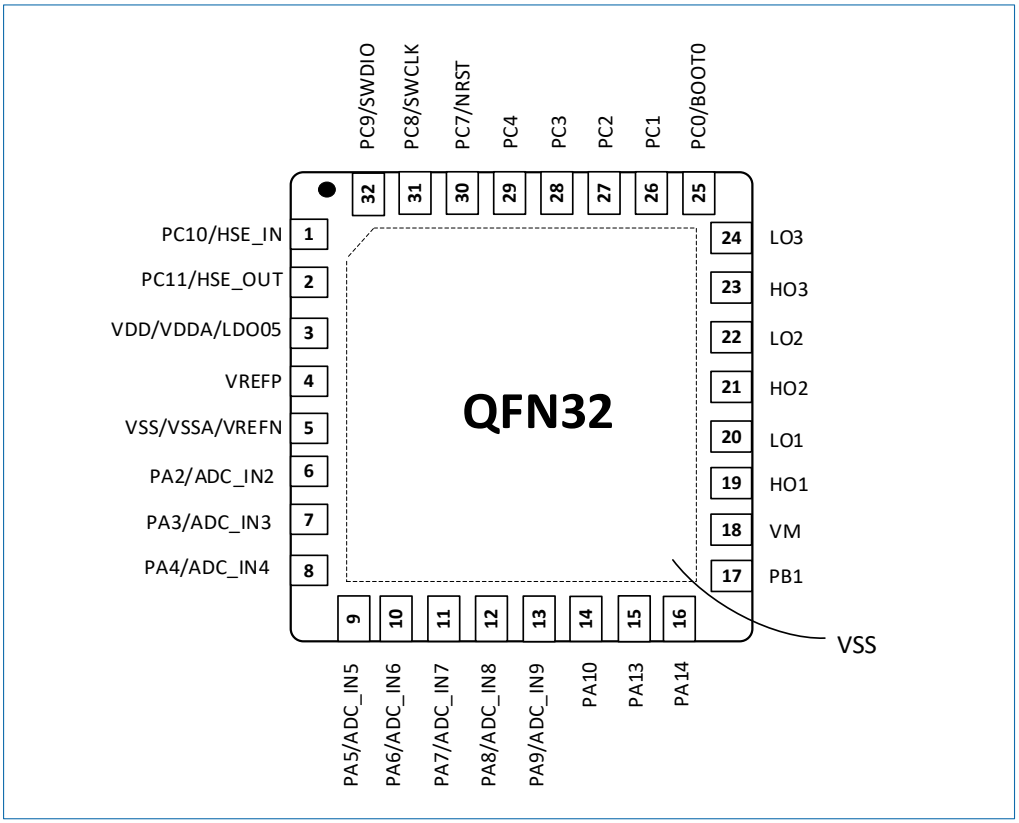

Figure 6-1 QFN32 package pinout

6.2 Pin description

Table 6-1 Pin description

QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
0	VSS	S	-	Digital ground (Pin 0 is the thermal pad on the QFN package bottom.)	
1	PC10/HSE_IN (PC10)	I/O	-	-	HSE_IN COMP3_INN1 OPA3_INN1 EXTIN10
2	PC11/HSE_OUT (PC11)	I/O	-	-	HSE_OUT COMP4_INN1 OPA3_OUT2 EXTIN11
3	VDD/VDDA/LDO05	S	-	Digital/Analog power supply/5 V LDO output	
4	VREFP	S	-	Reference power supply	
5	VSS/VSSA/VREFN	S	-	Reference power supply ground/Digital/Analog ground	
6	PA2	I/O	FT(2)	TIM3_CH1 COMP4_OUT	ADC_IN2 OPA2_OUT1 EXTIN2
7	PA3	I/O	FT	COMP3_OUT	ADC_IN3 OPA2_INN1

QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
					EXTIN3
8	PA4	I/O	FT	COMP1_OUT	CKI_1 ADC_IN4 EXTIN4
9	PA5	I/O	FT	COMP2_OUT TRACE_TX	ADC_IN5 DAC1_OUT EXTIN5
10	PA6	I/O	FT	RCC_MCO	ADC_IN6 COMP1_INP1 EXTIN6
11	PA7	I/O	FT	-	ADC_IN7 OPA1_OUT1 COMP2_INP1 EXTIN7
12	PA8	I/O	FT	RCC_MCO	ADC_IN8 OPA1_INN1 COMP3_INP1 EXTIN8
13	PA9	I/O	FT	-	ADC_IN9 COMP4_INP1 OPA1_INP2 OPA2_INP2 EXTIN9
14	PA10	I/O	FT	-	COMP1_INN0 COMP2_INN0 COMP3_INN0 COMP4_INN0 OPA3_INP1 EXTIN10
15	PA13	I/O	FT	-	OPA1_INP1 OPA2_INP1 EXTIN13
16	PA14	I/O	FT	-	OPA1_PGA_N OPA2_PGA_N COMP1_INP0 COMP2_INP0 COMP3_INP0 COMP4_INP0 OPA3_INP0 EXTIN14
17	PB1	I/O	FT	-	OPA1_INP0 OPA2_INP0 EXTIN1
18	VM	S	-	MCU operating power supply input	
19	HO1	O	-	1 channel high side output	
20	LO1	O	-	1 channel low side output	
21	HO2	O	-	2 channel high side output	
22	LO2	O	-	2 channel low side output	
23	HO3	O	-	3 channel high side output	
24	LO3	O	-	3 channel low side output	
25	PC0/BOOT0(PC0)	I/O	FT	TIM1_ETR ADC_EXT_TRIG TIM2_CH4	EXTIN0
26	PC1	I/O	FT	TIM2_CH3 SPI_CLK	EXTIN1
27	PC2	I/O	FT	TIM2_CH2 TIM3_CH3	EXTIN2

QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
				SPI_CS	
28	PC3	I/O	FT	TIM2_CH1 TIM3_CH2 SPI_MISO	EXTIN3
29	PC4	I/O	FT	TIM3_CH1 SPI_MOSI TRACE_TX	CKI_3 OPA3_INP2 EXTIN4
30	PC7/NRST(PC7)	I/O	FT	TIM3_CH4	NRST EXTIN7
31	PC8/SWCLK(SWCLK)	I/O	FT	CM0_SWCLK UART1_TX/UART1_RX ADC_EXT_TRIG	COMP1_INN1 EXTIN8
32	PC9/SWDIO(SWDIO)	I/O	FT	CM0_SWDIO UART1_RX/UART1_TX ADC_EXT_TRIG	COMP2_INN1 EXTIN9

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). FT = 5 V tolerant.

Note:

- Unless otherwise specified, all I/Os are configured in analog input mode during and after resets.
- For details about alternate functions, see section "6.3 Alternate function table".

6.3 Alternate function table

Table 6-2 Alternate function table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC8	SWCLK	ADC_EXT_TRIG	-	-	-	-	UART1_TX	-
PC9	SWDIO	ADC_EXT_TRIG	-	-	-	-	UART1_RX	-
PC10	-	-	-	-	-	-	-	-
PC11	-	-	-	-	-	-	-	-
PA2-AIN2	COMP4_OUT	-	-	-	-	TIM3_CH1	-	-
PA3-AIN3	COMP3_OUT	-	-	-	-	-	-	-
PA4-AIN4	COMP1_OUT	-	-	-	-	-	-	-
PA5-AIN5	COMP2_OUT	-	-	-	-	-	TRACE_TX	-
PA6-AIN6	RCC_MCO	-	-	-	-	-	-	-
PA7-AIN7	-	-	-	-	-	-	-	-
PA8-AIN8	RCC_MCO	-	-	-	-	-	-	-
PA9-AIN9	-	-	-	-	-	-	-	-
PA10	-	-	-	-	-	-	-	-
PA13	-	-	-	-	-	-	-	-
PA14	-	-	-	-	-	-	-	-
PC0	-	ADC_EXT_TRIG	TIM1_ETR	-	TIM2_CH4	-	-	-
PC1	-	-	-	-	TIM2_CH3	-	-	SPI_CLK
PC2	-	-	-	-	TIM2_CH2	TIM3_CH3	-	SPI_CS
PC3	-	-	-	-	TIM2_CH1	TIM3_CH2	-	SPI_MISO
PC4	-	-	-	-	-	TIM3_CH1	TRACE_TX	SPI_MOSI
PC7-NRST	-	-	-	-	-	TIM3_CH4	-	-

7 Package

7.1 Package outline

7.1.1 QFN32

QFN32 is a 5 mm × 5 mm, 0.5 mm pitch package.

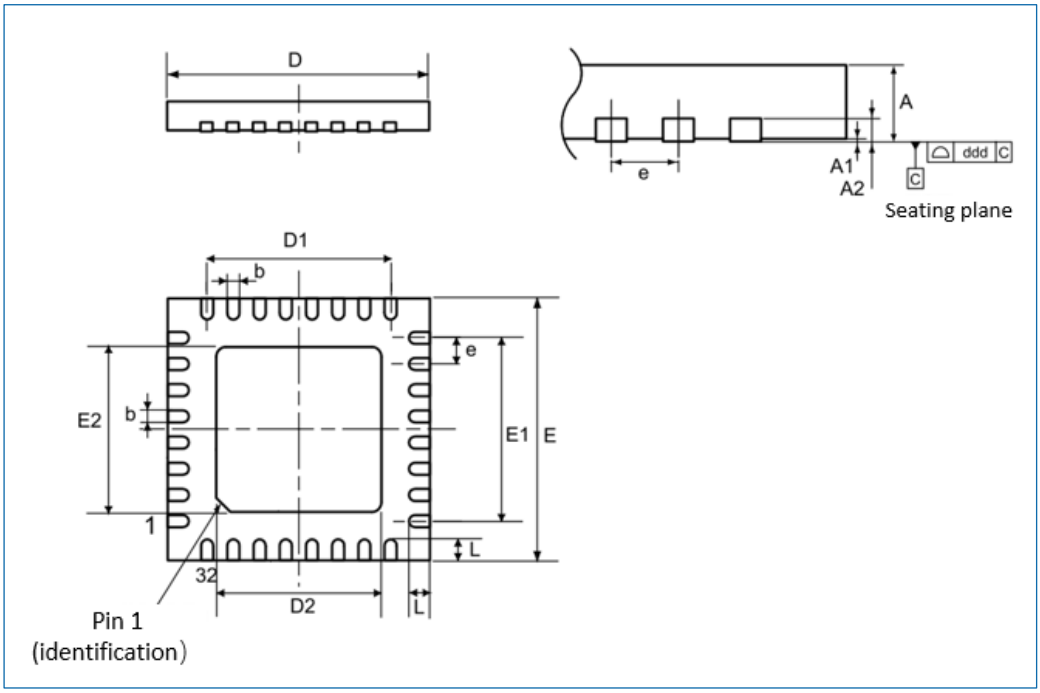

Figure 7-1 QFN32 package outline

Table 7-1 QFN32 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches) (1)	Max (inches) (1)
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.500	0.550	0.600	0.0197	0.0217	0.0236
A2	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-2 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 QFN32 marking

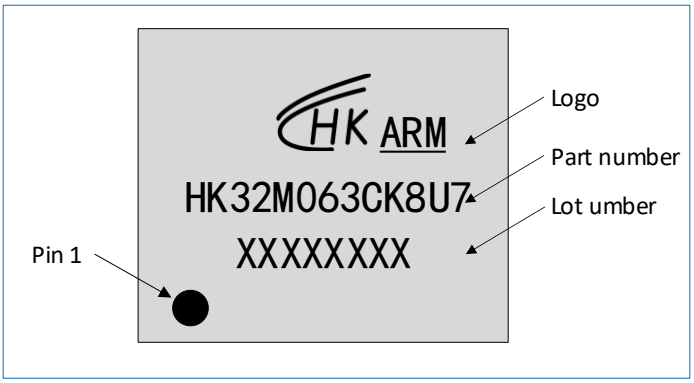

Figure 7-2 QFN32 HK32M063CK8U7 marking example

8 Ordering information

8.1 Device numbering conventions

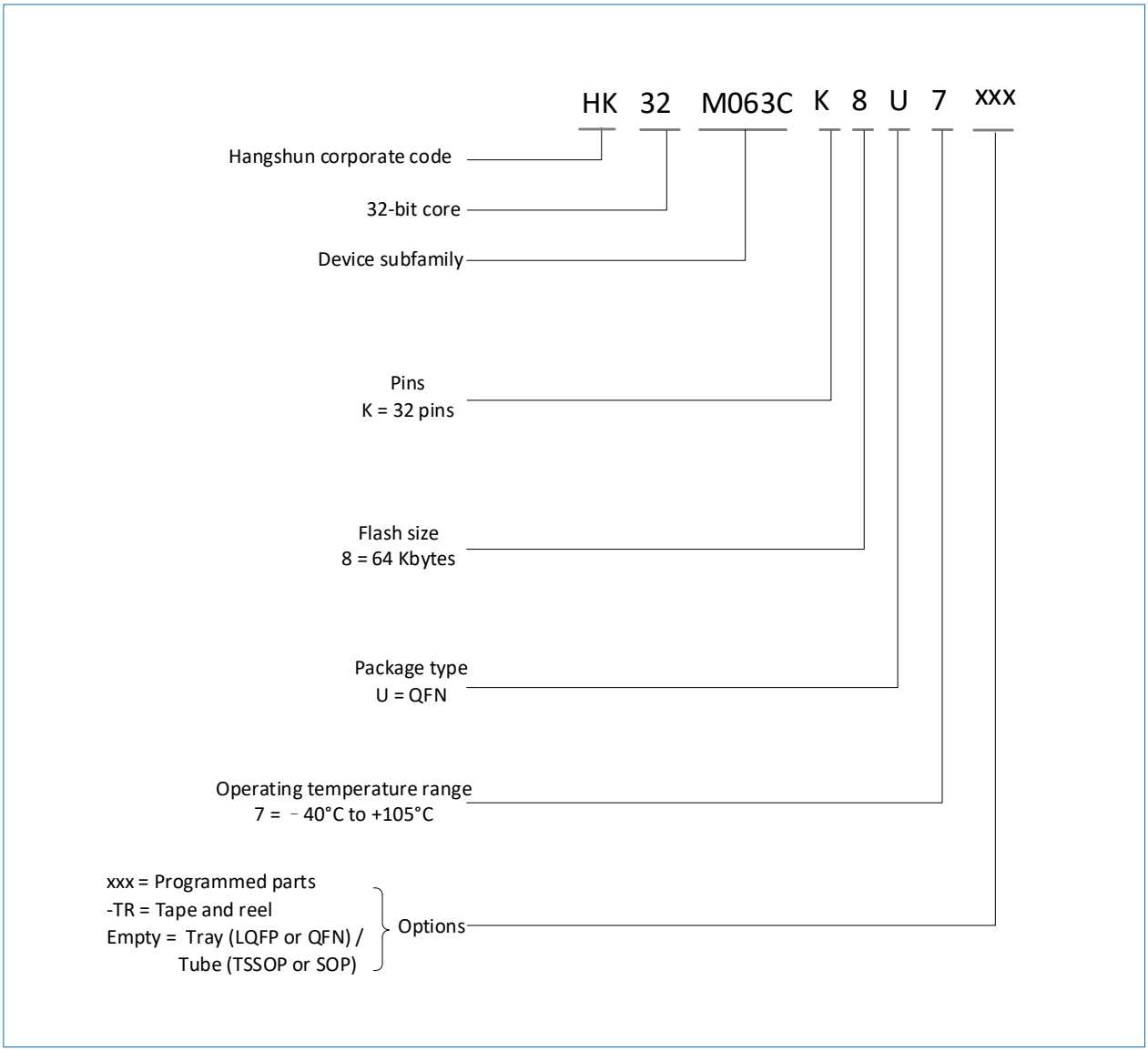

Figure 8-1 Device numbering conventions

8.2 Packing information

Table 8-1 HK32M063C ordering information

Package	Part Number	Shipping Option	Remarks
QFN32	HK32M063CK8U7	Tray	
QFN32	HK32M063CK8U7-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PGA	Programmable Gain Amplifier
PLL	Phase-locked Loop
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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