HK32F39AxCxDxE Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F39A series microcontrollers (MCUs) to help you quickly understand their features and functions.

Audience

This document is intended for:

- HK32F39A developers
- HK32F39A testers
- HK32F39A users

Release Notes

This document is applicable to HK32F39A series MCUs.

Revision History

Version	Date	Description
1.0	2023/05/29	The initial release.
1.1	2023/09/15	1. Updated the block diagram. 2. Corrected the ADC sampling rate. 3. Updated the USART communication speeds. 4. Updated the relationships between ADC channels and pins. 5. Updated the operating current characteristics. 6. Added section "7.2 Device marking" and section "8.1 Device numbering conventions". 7. Added section "4.2.17 QSPI characteristics". 8. Updated Figure 3-4 Reset circuit.
1.2	2023/11/03	1. Updated the maximum prescaler value of FLITFCLK in section "3.10.2 Clock tree". 2. Updated sections "4.2.6 HSE clock characteristics" and "4.2.7 LSE clock characteristics". 3. Updated alternate functions in section "6.3 LQFP64/LQFP100 pin description". 4. Changed the abbreviation of voltage comparator from VC to COMP.

Contents

1 Introduction

This document is the datasheet for HK32F39A series MCUs. HK32F39A is a family of high-performance MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes the HK32F39AxC, HK32F39AxD, and HK32F39AxE sub-series. Their part numbers include:

- HK32F39ARxT6 (LQFP64 package):
  - HK32F39ARCT6
  - HK32F39ARDT6
  - HK32F39ARET6
- HK32F39AVxT6 (LQFP100 package):
  - HK32F39AVCT6
  - HK32F39AVDT6
  - HK32F39AVET6

For more details of HK32F39A, see *HK32F39A User Manual*.

2 Product overview

HK32F39A adopts the ARM® Cortex®-M3 core. HK32F39A series MCUs can operate at a maximum frequency of 120 MHz and provide 1-Kbyte L1 cache for instructions. Hangshun's patented coprocessing arithmetic logic unit (COALU) embedded in HK32F39A can realize the effect of most arithmetic instructions supported by ARM® Cortex®-M4, including the calculation of 32-bit single-precision floating-point numbers. Additionally, COALU supports a variety of 32-bit and 64-bit customized arithmetic operations.

HK32F39A embeds large-capacity memories, including up to 527 Kbytes of Flash, 64 Kbytes of SRAM, 32 Kbytes of CCM SRAM, and 1 Kbyte of cache. It can connect to up to 1 Gbyte of external static memory via the flexible static memory controller (FSMC) module. 256 Mbytes of the external static memory are used to store instructions and can be used by the internal 1-Kbyte cache for instructions. Additionally, it can connect to 256 Mbytes of NOR Flash memory via the quad serial peripheral interface (QSPI) module. The NOR Flash memory is used to store instructions and can be used by the internal 1-Kbyte cache for instructions.

HK32F39A incorporates the advanced encryption standard (AES) module, HASH module, and true random number generator (TRNG), which are used for data encryption, data decryption, and digital signatures. The built-in cyclic redundancy check (CRC) module is used to check data integrity.

With its embedded digital camera memory interface (DCMI), four thin film transistor (TFT) interfaces, and two direct memory access (DMA) modules (12 DMA channels in total), HK32F39A MCUs provide a solution that captures, processes, and displays digital images and videos.

The serial audio interface (SAI) embedded in HK32F39A ensures its compliance with most audio interface protocols.

HK32F39A embeds two advanced 16-bit pulse width modulation (PWM) timers (eight PWM output channels in total, six of which have complementary PWM outputs with programmable inserted dead-times), four general-purpose 16-bit PWM timers (16 PWM output channels in total), and two basic 16-bit timers. The two advanced timers are connected to the embedded four voltage comparators (COMPs) on the chip. In motor solutions, customers do not need additional voltage comparators or related circuitry on the circuit board.

HK32F39A provides an independent V_{BAT} power domain. When the main V_{DD} supply is powered off, the real-time clock (RTC) can be powered by V_{BAT}.

HK32F39A integrates various analog circuits: three 12-bit ADCs (sharing up to 25 analog signal input channels: two channels for weak drive signal input and one channel for 5 V high-voltage signal inputs), two 12-bit DACs, a temperature sensor, a 0.8 V internal reference voltage, a programmable voltage detector (PVD), a power-on reset (POR)/power-down reset (PDR) circuitry, and a V_{BAT} resistor voltage divider (the output of the divider is connected to the ADC on the chip).

HK32F39A supports multiple power consumption modes. In the lowest-power consumption mode, the typical leakage current is less than 100 nA. HK32F39A operates in the –40°C to +105°C temperature range, from a 2.0 V to 3.6 V power supply. It meets the environmental requirements of most applications.

HK32F39AxC, HK32F39AxD, and HK32F39AxE MCUs are offered in 64-pin and 100-pin packages. The peripherals vary based on the package type.

With its wide range of peripherals, HK32F39A is suitable for various applications:

- Industry applications, such as programmable controllers, printers, and scanners
- Human-machine audio-video multimedia interaction
- Graph-displaying devices
- Speech recognition devices
- Monitoring devices
- Motor-driven devices and speed control

- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- ARM® Cortex®-M3 core
  - Maximum frequency: 120 MHz
  - 24-bit SysTick timer
- Operating voltage range
  - Main power supply (V_{DD}): 2.0 V to 3.6 V; backup power supply (V_{BAT}): 1.8 V to 3.6 V
  - When the main V_{DD} supply is powered off, the RTC is powered by $V_{BAT.}$
  - When the main V_{DD} supply is powered off, the 86-byte backup register is powered by V_{BAT}.
- Typical operating current (V_{DD})
  - Dynamic power consumption in Run mode: 19.3 mA@120 MHz@3.3 V
  - Static power consumption in Sleep mode: 5.6 mA@120 MHz@3.3 V (Wakeup time: one clock period)
  - Static power consumption in Stop mode:
    - LDO operating at full speed: 303 µA@3.3 V
    - LDO in low-power mode: 89.4 µA@3.3 V (Wakeup time: 10 µs)
  - Static power consumption in Standby mode: 3.3 µA@3.3 V (Wakeup time: 150 µs)
  - Static power consumption in Shutdown mode: 0.09 µA@3.3 V (Wakeup time: 200 µs)
- Typical operating current (V_{BAT})
  - V_{BAT} power consumption: 2.6 µA@3.3 V (RTC enabled)
  - V_{BAT} power consumption: 2.1 µA@3.3 V (RTC disabled, backup registers retained)
- Coprocessing arithmetic logic unit (COALU)
  - Realizes the same effect as most of the arithmetic instructions supported by ARM® Cortex®-M4
  - Calculation of 32-bit single-precision floating-point numbers
  - A variety of 32-bit and 64-bit customized arithmetic operations
- DMA controller
  - Two independent DMA controllers: DMA1 and DMA2
  - DMA1 provides seven channels
  - DMA2 provides five channels
  - Can be triggered by the timer, ADC, SPI, I2C, or USART
- Memory
  - 527-Kbyte Flash memory, including the 512-Kbyte main Flash and 15-Kbyte information block. When the CPU frequency is 24 MHz or lower, there is no wait state for bus access. The Flash data security protection function provides separate read and write protection.
  - 1-Kbyte cache for storing CPU instructions
  - Up to 97-Kbyte on-chip SRAM
  - 1 Gbyte of external memory (NOR/PSRAM/NAND/PC Card) via the FSMC module. 256-Mbyte external

memory is used to store instructions and can be used by the internal cache.
    - 256 Mbytes of external NOR Flash memory via the QSPI module. The NOR Flash memory is used to store instructions and can be used by the internal cache.
    - Embedded encryption and decryption functions for instructions. Instructions are stored as ciphertext on internal and external memories.
- Clock
    - External high-speed clock (HSE): 4 MHz to 32 MHz
    - External low-speed clock (LSE): 32.768 kHz
    - Internal high-speed clock (HSI): 56 MHz/28 MHz/8 MHz
    - Internal low-speed clock (LSI): 40 kHz
    - PLL output clock: 120 MHz (maximum value)
- Reset
    - External pin reset
    - Power reset
    - Software reset
    - IWDG and WWDG reset
    - Low-power management reset
- Encryption
    - TRNG
    - 128/192/256-bit AES
    - Hash (SHA-256)
    - CRC32
- Data communication interfaces
    - 6 × USARTs
    - 3 × SPIs (support the I2S protocol)
    - 2 × I2Cs
    - 1 × SDIO
    - 2 × CAN 2.0A/2.0B
    - 1 × full-speed (FS) USB
- Audio and video interfaces
    - 1 × DCMI
    - 4-channel interface
    - 1 × SAI, including two independent audio protocol processing modules
- Timer and PWM generator
    - Advanced PWM timers: TIM1/TIM8 (six complementary PWM output channels with programmable inserted dead-times)
    - General-purpose PWM timers: TIM2/TIM3/TIM4/TIM5 (16-bit timers)
    - Basic timers: TIM6/TIM7 (supports CPU interrupts, DMA requests, and DAC conversion trigger)
- Programmable voltage detector (PVD)
    - Adjustable eight-level thresholds for detecting voltage
    - Rising edge or falling edge detection configurable
- On-chip analog peripherals

- 3 × 12-bit ADCs, each up to 1 MSPS (25 analog input channels in total: two channels for weak drive signal input, one channel for 5 V high-voltage signal input); dual-ADC mode, sampling rate up to 2 MSPS
- 2 × 12-bit DACs
- 1 × temperature sensor
- 1 × 0.8 V internal reference voltage
- 1 × V_{BAT} resistor voltage divider (the output of the divider is connected to the ADC on the chip for monitoring V_{BAT} voltage)
- 4 × voltage comparators (connected to two on-chip advanced PWM timers. In motor solutions, customers do not need additional voltage comparators or related circuitry on the circuit board.)

- UID
  - Each HK32F39A MCU provides a 96-bit UID.
- Debug and trace port
  - SW-DP dual-wire debug port
  - JTAG five-wire debug port
  - ARM® CoreSight™ debug component (DWT, FPB, ITM, TPIU)
  - Single-wire asynchronous trace data output interface (TRACESWO)
  - Four-wire synchronous trace data output interface (TRACEDO[3:0], TRACECKO)
  - Customized DBGMCU debug controller (the low-power mode simulation control, debug peripheral clock control, and allocation of debug and trace interfaces)
- General-purpose input/output (GPIO)
  - Up to 51 GPIOs in the 64-pin package/80 GPIOs in the 100-pin package
  - Each GPIO can be used as an external interrupt input
  - Built-in switchable pull-up/pull-down resistors
  - Supports open-drain output
  - Supports Schmitt hysteresis input
  - Configurable output drive capacity: ultra-high/high/medium/low level
  - Provides up to 40 mA drive current
- Clock-calendar function provided by RTC counter in cooperation with software
- Reliability
  - Passed HBM3000V/CDM500V/MM200V/LU200mA level tests.
- Operating temperature range: –40°C to 105°C

2.2 Device overview

Table 2-1 HK32F39A series features

Feature		HK32F39A RCT6	HK32F39A RDT6	HK32F39A RET6	HK32F39A VCT6	HK32F39A VDT6	HK32F39A VET6
CPU	Core	Cortex®- M3					
	Frequency (MHz)	120					
Memory	Flash (Kbyte)	256	384	527	256	384	527
	Cache (Kbyte)	1					

Feature		HK32F39A RCT6	HK32F39A RDT6	HK32F39A RET6	HK32F39A VCT6	HK32F39A VDT6	HK32F39A VET6
	SRAM (Kbyte)	64					
	CCM SRAM (Kbyte)	32					
DMA (Channels)		DMA1 (7 channels) + DMA2 (5 channels)					
Timer	Advanced timer (16-bit)	2					
	General-purpose timer (16-bit)	4					
	Basic timer (16-bit)	2					
	SysTick timer	1					
	RTC	1					
	IWDG	1					
	WWDG	1					
Peripheral comm. interface	USART	6					
	I2C	2					
	SPI/I2S	3/3					
	QSPI	1					
	CAN	2					
	USB	1					
	FSMC	-	-	-	1	1	1
	SDIO	1					
	TFT (Channels)	-	-	-	1 (4)	1 (4)	1 (4)
Audio & video interface	DCMI	1					
	SAI	1					
Coprocessing arithmetic logic unit (COALU)		1					
CRC		1					
Encryption	TRNG	1					
	AES	1					
	Hash	1					
ADC	ADC (Channels)	ADC1 (17) + ADC2 (16) + ADC3 (13)			ADC1 (19) + ADC2 (18) + ADC3 (15)		

Feature		HK32F39A RCT6	HK32F39A RDT6	HK32F39A RET6	HK32F39A VCT6	HK32F39A VDT6	HK32F39A VET6
	Maximum sampling rate	1 MSPS					
	Accuracy	12-bit					
Temperature sensor		1					
DAC		2					
Voltage comparator (COMP)		4					
Programmable voltage detector (PVD)		1					
96-bit UID		1					
GPIO		51	51	51	80	80	80
Package		LQFP64	LQFP64	LQFP64	LQFP100	LQFP100	LQFP100
Operating voltage		2.0 V – 3.6 V					
Backup power supply		1.8 V – 3.6 V					
Operating temperature		–40°C – 105°C					

(1). Note: The hyphen (-) in the table indicates that the feature is not supported.

3 Function description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor which provides an MCU platform featuring low cost and high performance. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M3 core, the HK32F39A family is compatible with ARM tools and software.

The following figure shows the block diagram of HK32F39A:

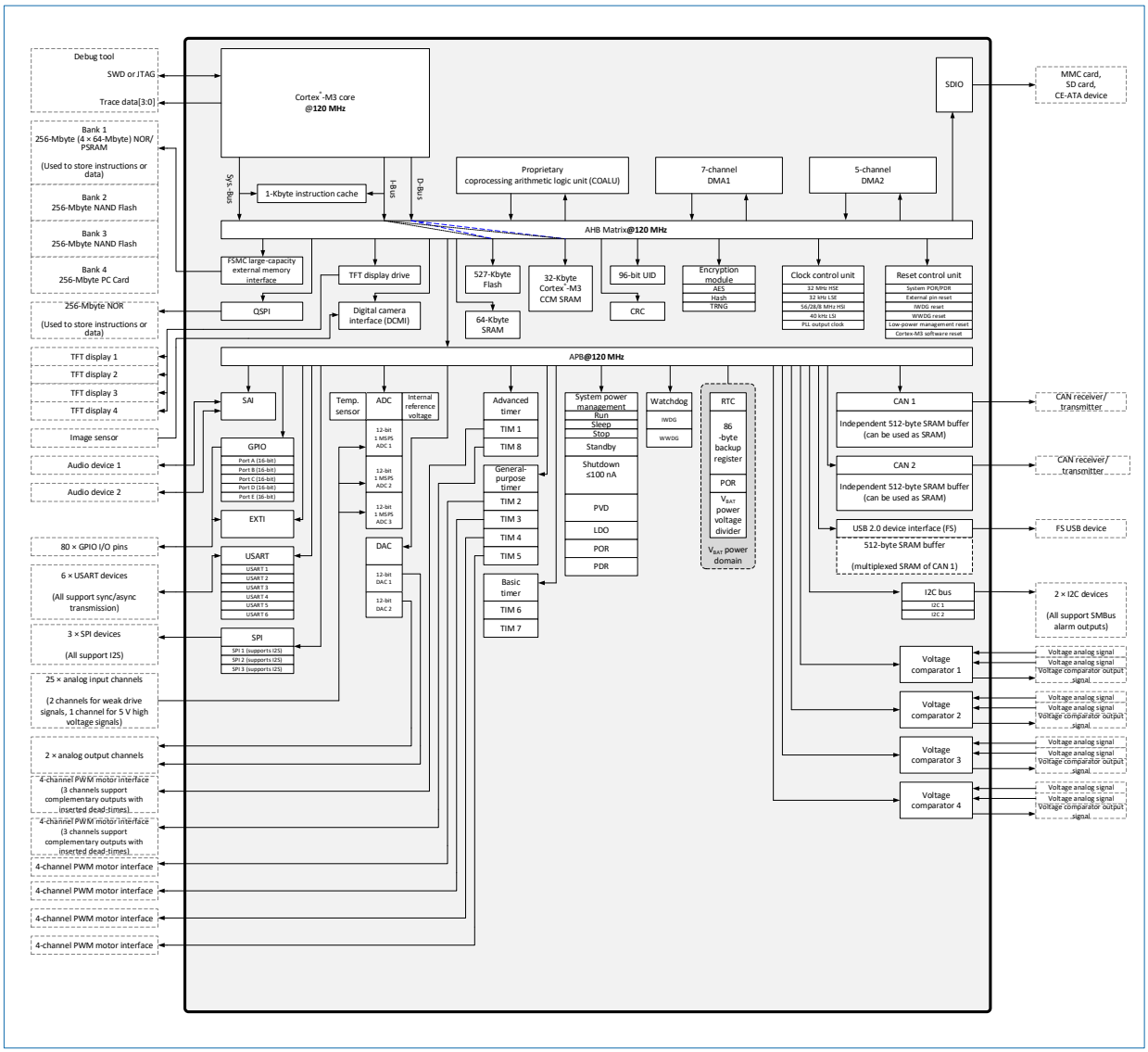


Figure 3-1 HK32F39A block diagram

3.2 Memory mapping

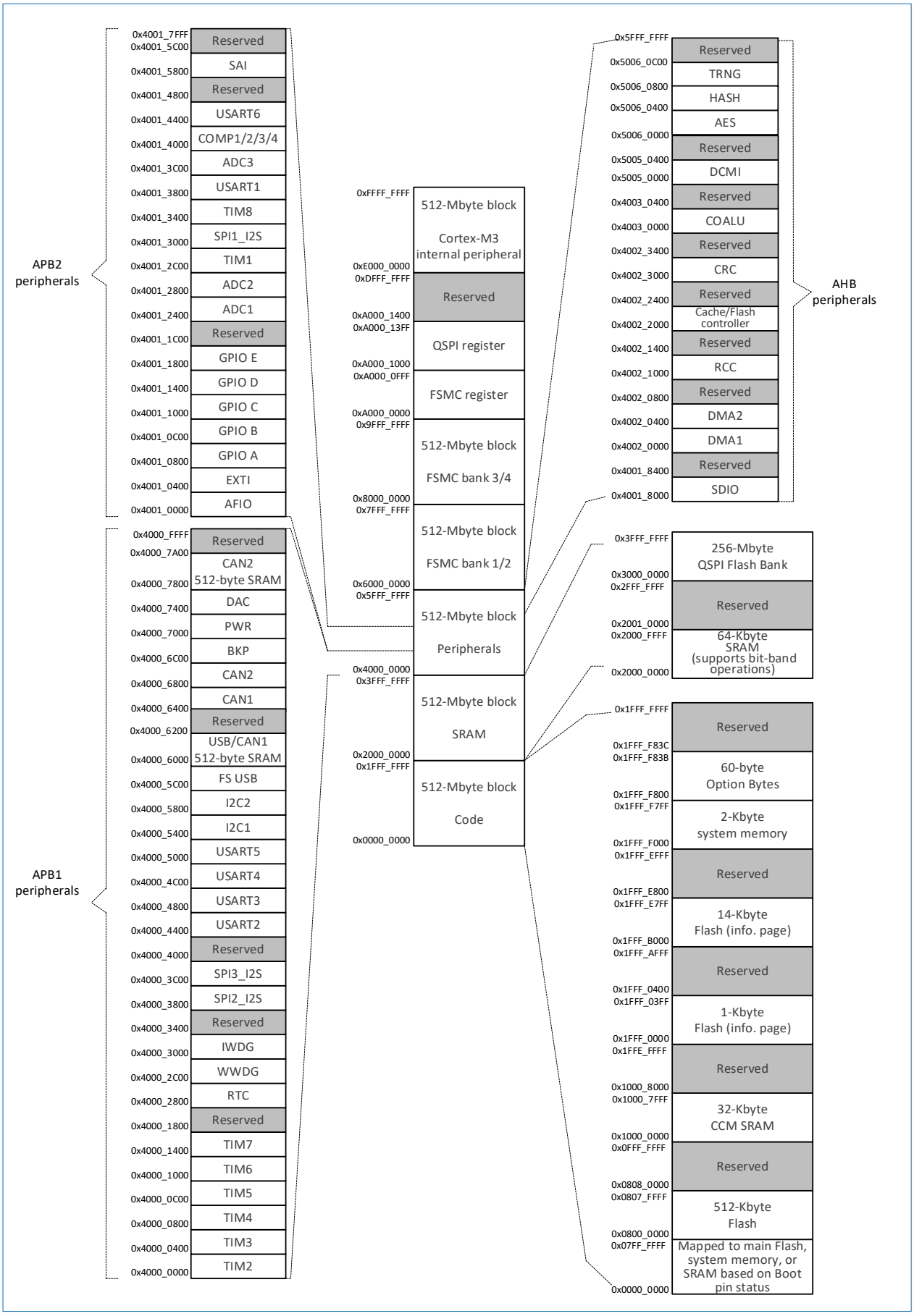


Figure 3-2 Memory mapping

3.2.1 Flash

HK32F39A integrates a Flash memory of up to 527 Kbytes to store programs and data. The Flash consists of a 512-Kbyte main Flash block and a 15-Kbyte information block.

- Flash data width: 128 bits, 2 Kbytes per page
- Flash access: write in half words (16 bits), words (32 bits), two words (64 bits), or four words (128 bits); read in 128 bits
- Supports Flash read/write protection.
- Integrates the instruction prefetch buffer and data buffer.
- Integrates a module for automatically encrypting and decrypting Flash instructions to protect the intellectual property (IP) of on-chip software.

3.2.2 SRAM

HK32F39A integrates a 64-Kbyte SRAM. The SRAM can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait state, meeting the requirements of most applications.

3.2.3 CCM SRAM

HK32F39A embeds 32 Kbytes of core-coupled memory (CCM) SRAM whose memory logic address is from 0x1000 0000 to 0x1000 7FFF. CCM SRAM can be accessed in words, half words, or bytes and is accessible from I-BUS, D-BUS, DMA1, and DMA2.

3.3 COALU

Hangshun's patented coprocessing arithmetic logic unit (COALU) can realize the effect of most arithmetic instructions supported by ARM® Cortex®-M4, including the calculation of 32-bit single-precision floating-point numbers. Additionally, COALU supports a variety of 32-bit and 64-bit customized arithmetic operations, which makes HK32F39A an MCU with improved calculation capability suitable for different types of calculation.

- Fixed-point calculation
  - 64-bit/32-bit root calculation
  - 64-bit/32-bit division
  - Saturation
    - Saturated multiply accumulate
    - 32-bit saturated addition/subtraction
    - Single instruction multiple data (SIMD) saturated addition/subtraction
    - Data saturation
  - SIMD addition/subtraction
  - Half addition/subtraction result
  - Extended addition/subtraction
  - Multiply accumulate and SIMD multiply accumulate
- Floating-point calculation
  - Floating-point addition
  - Floating-point subtraction
  - Floating-point multiplication
  - Floating-point division
  - Floating-point root calculation
  - Floating-point multiply accumulate

- Conversion between floating-point numbers and fixed-point numbers (including the conversion between 32-bit floating-point numbers and fixed-point numbers, and between 64-bit floating-point numbers and fixed-point numbers)

3.4 Cache

The device integrates 1 Kbyte of high-speed cache for storing instructions.

- 8-way set associative
- The least recently used (LRU) strategy is adopted.
- The embedded counter counts the hit rate of instructions stored in the cache.
- The cache control register can be configured to cache specific instructions. The data of one of the following instruction fetch operations can be cached at a time:
  - I-Bus instruction fetch from internal Flash
  - SYS-Bus instruction fetch from external Flash via QSPI
  - SYS-Bus instruction fetch from external Flash via FSMC

3.5 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32F39A integrates a CRC hardware calculation unit. It is used to get a CRC code from an 8-, 16- or 32-bit data word by using a generator polynomial.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with a reference signature generated at link time and stored at a specified memory location.

3.6 FSMC

- The flexible static memory controller (FSMC) can interface with 1 Gbyte of external static memories, including:
  - Static random access memory (SRAM)
  - Read-only memory (ROM)
  - NOR Flash
  - PSRAM (four memory banks)
- Two NAND Flash memory banks with error correction code (ECC) hardware that checks up to 8 Kbytes of data
- Compatible with 16-bit PC Cards
- Supports burst mode access to synchronous devices, such as NOR Flash and PSRAM
- 8-bit or 16-bit data bus
- Independent chip select (CS) for each memory bank
- Independent configuration for each memory bank
- Supports write enable and byte lane select outputs when PSRAM and SRAM devices are used
- Translates 32-bit wide AHB transactions into consecutive 16-bit or 8-bit access to external 16-bit or 8-bit devices
- The 2-word long write FIFO (each word is 32-bit wide) of FSMC makes it possible to release the AHB for other operations when writing to slow memories. Before a new FSMC operation is started, the FIFO is drained. The FSMC inserts wait states until the current memory access is complete.
- Asynchronous wait control for external memories
- Write encryption and read decryption for 16-bit external memories
- Supports Intel 8080 mode and Motorola 6800 mode, and can flexibly connect to various LCD controllers.

3.6.1 TFT LCD interface

Some of the FSMC interfaces are thin film transistor (TFT) liquid crystal display (LCD) interfaces, which can directly drive LCDs. You can use either the TFT LCD interfaces or other FSMC interfaces (excluding TFT LCD interfaces) at a time. Four TFT LCD panels (RGB: 5 bits for red, 6 bits for green, and 5 bits for blue), including four horizontal synchronization signals, four vertical synchronization signals, and four data enable signals of the four TFT LCD panels, can be driven by using the FSMC interface.

3.7 NVIC

HK32F39A embeds a nested vectored interrupt controller (NVIC) to manage interrupts flexibly with the lowest interrupt latency.

- The closely coupled NVIC ensures low-latency interrupt processing.
- The interrupt vector entry address is directly passed to the core.
- Allows the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

The HK32F39A MCU has 71 external interrupts numbered from 0 to 70.

3.8 EXTI

The extended interrupt/event controller (EXTI) is comprised of 26 edge detectors that are used to generate interrupt/event requests. The EXTI lines from EXTI0 to EXTI15 are connected to I/O pins.

The connections of the other 10 EXTI lines are as follows:

- EXTI 16 connected to the PVD output
- EXTI 17 connected to the RTC alarm event
- EXTI 18 connected to the USB wakeup event
- EXTI 20 connected to the COMP1 output
- EXTI 21 connected to the COMP2 output
- EXTI 22 connected to the COMP3 output
- EXTI 23 connected to the COMP4 output
- EXTI 24 connected to the ADC1 AWD event
- EXTI 25 connected to the ADC2 AWD event
- EXTI 26 connected to the ADC3 AWD event

EXTI lines from EXTI 24 to EXTI 26 are connected to internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). EXTI lines from EXTI 24 to EXTI 26 detect the rising edge of events in only Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system.

3.9 Resets

HK32F39A supports the system reset, power reset, and backup domain reset.

3.9.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain. You can identify a reset source by checking reset status flags in the RCC_CSR

register. For details, see Table 3-1.

When any of the following events occurs, a system reset signal is generated:

- Low level on NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW reset)
- Low-power management reset

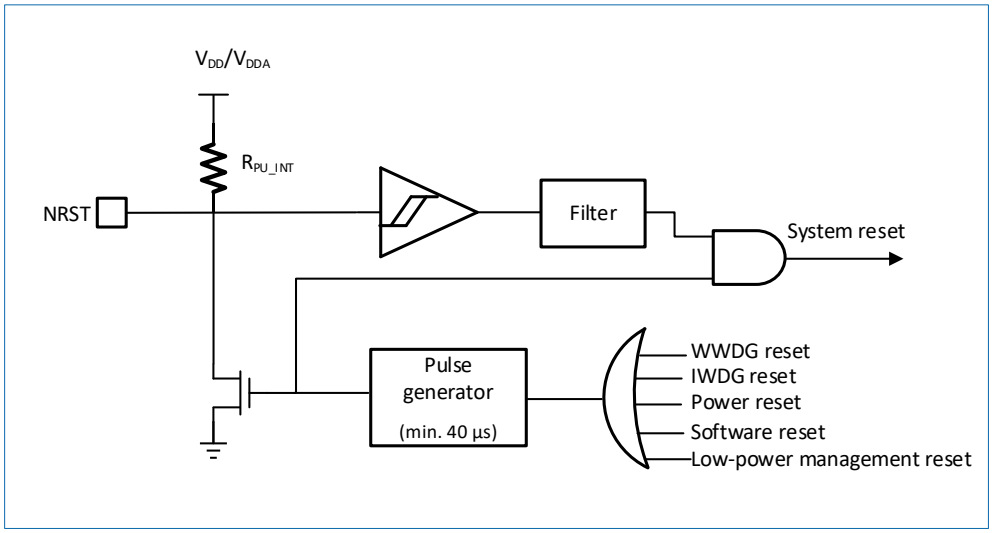


Figure 3-3 Reset circuitry

The reset sources act on the NRST pin and the NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004.

The internal reset signal is output on the NRST pin. The pulse generator guarantees a pulse duration of at least 40 µs for each internal or external reset source. When the NRST pin is pulled low and an external reset is generated, a reset pulse is generated.

Table 3-1 Software reset and low-power management reset

Reset Type	Configuration
Software reset	The SYSRESETREQ bit in Cortex®-M3 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
Low-power management reset	To generate a low-power management reset when entering the Standby mode: Set the nRST_STDBY bit in option bytes to 0 to generate the low-power management reset. Then, even if the system is in the process of entering the Standby mode, it will be reset instead of entering the Standby mode.
	To generate a low-power management reset when entering the Stop mode: Set the nRST_STOP bit in Option bytes to 0 to generate the low-power management reset. Then, even if the system is in the process of entering the Stop mode, it will be reset instead of entering the Stop mode.

3.9.2 Power reset

A power reset is generated when one of the following events occurs:

- POR/PDR reset
- Exit from Standby mode

The power reset resets all registers, except for the registers in the backup domain.

HK32F39A embeds POR/PDR circuits. The circuits keep operating to ensure that the system runs properly when the power supply is over the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the MCU remains in the reset state and no external reset circuit is required.

3.9.3 Backup domain reset

The backup domain has two dedicated resets, which only affect the backup domain. A backup domain reset is generated when one of the following events occurs:

- Software reset: Set the BDRST bit in the RCC_BDCR register.
- After both V_{DD} and V_{BAT} are powered off, power on V_{DD} and/or V_{BAT}.

3.10 Clocks

HK32F39A selects a system clock when it starts. When it resets, the 8 MHz HSI RC oscillator is selected as the default CPU clock, and then a 4 to 32 MHz external clock can be selected. If the external clock fails, it will be isolated and a corresponding interrupt will be generated.

HK32F39A also provides the LSI, LSE, and GPIO input as clock sources and uses the PLL to generate required clocks.

HK32F39A integrates a clock security system (CSS) circuit. The threshold for the detection of HSE frequency is adjustable.

3.10.1 Clock sources

Table 3-2 Clock sources

Clock	Description
HSI clock	Output frequency: 56 MHz, which can be divided into 28 MHz or 8 MHz (default value)
HSE clock	Frequency: 4 MHz to 32 MHz Clock can be input from OSC_IN
PLL clock	Input frequency: 2 MHz to 80 MHz Output frequency: 16 MHz to 120 MHz
LSI clock	Frequency: 30 kHz to 60 kHz (typical value: 40 kHz)
LSE clock	Frequency: 32.768 kHz Clock can be input from OSC32_IN
GPIO input clock	PA1, PB1, PC7, PB7: up to 64 MHz

3.10.2 Clock tree

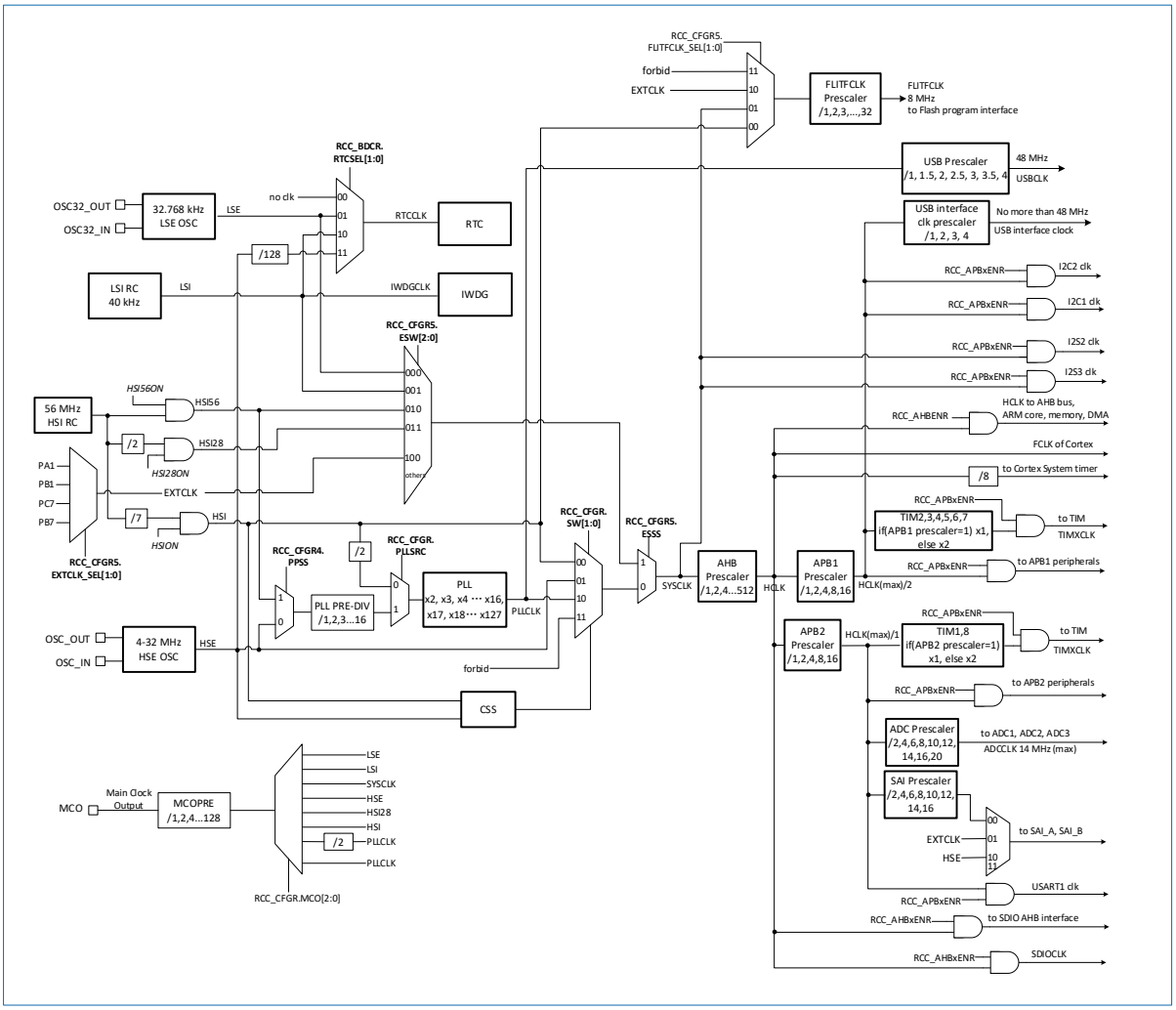


Figure 3-4 Clock tree

Note:

- PLL: chosen from HSI8/2, HSI56/PREDIV, or HSE/PREDIV.
- SYSCLK: chosen from HSI8, HSI28, HSI56, HSE, PLL, LSI, LSE, or GPIO input clock. HSI (8 MHz) is the default clock.
- FLITFCLK: chosen from HSI8, GPIO input clock, or SYSCLK clock.

3.11 Boot modes

When the system starts, the boot pins are used to select one of the following boot modes:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the USART1 interface.

3.12 Power supply schemes

- V_{DD} = 2.0 V to 3.6 V: The V_{DD} pin supplies power to I/O pins and internal low dropout regulators (LDOs).
- V_{DDA} = 2.0 V to 3.6 V: The V_{DDA} pin supplies power to the analog circuitry, such as the ADC and temperature sensor.
- V_{BAT} = 1.8 V to 3.6 V: When V_{DD} is powered off, V_{BAT} supplies power to the RTC, external 32.768 kHz oscillator,

and backup registers.

3.13 Power supply supervisor

HK32F39A embeds power-on reset (POR)/power-down reset (PDR) circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the POR/PDR threshold (see Table 4-6). When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuit is required.

HK32F39A integrates a programmable voltage detector (PVD). The PVD monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated, and the interrupt program may send a warning message or set the MCU in the safe state. The PVD is enabled by using software.

3.14 Low-power modes

HK32F39A supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the phase-locked loop (PLL), the HSE oscillator, and the HSI oscillator are disabled. The MCU can be woken up from Stop mode by any extended interrupt/event controller (EXTI) line. The EXTI line source can be any one of the 16 external I/O pins, a PVD output, an RTC alarm, or a USB wakeup signal.

- Standby mode

  In Standby mode, the MCU achieves extremely low power consumption. The internal LDO is off, so the entire 1.2 V domain is powered off. The PLL, HSI oscillator, and HSE oscillator are disabled. SRAM and register contents are lost, except for registers in the backup domain. The Standby circuitry works as normal. MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

- Shutdown mode

  In Shutdown mode, the MCU achieves extremely low power consumption. All internal LDOs and all clock sources are off. By default, the backup domain power supply is off (which can be configured to on). The shutdown wakeup circuitry keeps operating. MCUs exit from Shutdown mode when an external reset on the NRST pin, an IWDG reset, or a rising edge on the WKUP pin occurs. The backup domain power supply is configurable, but is it off by default, so MCUs cannot be woken up by an RTC alarm when the backup domain power supply in in the default off state.

Table 3-3 Entry into and exit from Cortex®-M3 low-power modes

Operating Mode	Entry	Exit	CPU Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
Sleep mode	1. Set PWR_CR:LPDS = 0 and PWR_CR:PDDS = 0. 2. The software executes WFI/WFE instructions.	Any IRQ interrupt/event, including SysTick.	The CPU clock is off. No impact on other clocks or the ADC clock.	On	On
Stop mode	1. Set PWR_CR:PDDS = 0. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes	Any EXTI line. The MCU can be pre-woken by periodic ADC sampling. The real	All clocks stop.	HSI and HSE oscillators are off.	On or in low power mode (configured

Operating Mode	Entry	Exit	CPU Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
	WFI/WFE instructions.	wakeup occurs when the conditions are met.			in PWR_CR)
Standby mode	1. Set PWR_CR:LPDS = 0 and PWR_CR:PDDS = 1. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions. 4. Clear the WUF bit in the Power control/status register (PWR_CSR).	Three polarity-configurable external pins (WKUPx), the RTC alarm, and the IWDG reset.	All clocks stop.	HSI and HSE oscillators are off.	Off
Shutdown mode	1. Set PWR_CR:LPDS = 0, PWR_CR:PDDS = 1, and PWR_CSR2:SHDS = 1. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions.	Three polarity-configurable external pins (WKUPx), and the RTC alarm (when the backup domain power supply is configured to on).	All clocks stop.	All clocks stop.	Off

3.15 DMA

The flexible general-purpose DMAs (seven channels for DMA1 and five channels for DMA2) manage the data transfer from memories to memories, from devices to memories, and from memories to devices. The two DMAs support circular buffer management, preventing the interrupt that occurs when the DMA controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by software. The length, source, and destination of data to be transferred can be independently set by using software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, SDIO, and ADC.

3.16 RTC and BKP

The power supply of RTC and the backup registers is controlled by a switch. When V_{DD} is present, the switch selects V_{DD} to supply power. Otherwise, the switch takes power from the V_{BAT} pin.

3.16.1 RTC

The real-time clock has a set of continuously running counters and can provide the clock calendar function via software. In addition, the real-time clock provides alarm interrupt and periodic interrupt functions.

The RTC can be driven by a 32.768 kHz external oscillator or an internal low-power RC oscillator whose typical frequency is 40 kHz. To compensate for the natural quartz deviation, an external 512 Hz signal is output to calibrate the RTC. The RTC has a 32-bit programmable counter for long-term measurement in conjunction with the compare register. A 20-bit prescaler is used for the time base clock. By default, the prescaler is configured to generate a time base of 1 second from a clock at 32.768 kHz.

The HK32F39A MCU has a wakeup timer for periodic wakeup.

3.16.2 BKP

Backup registers are used to store user application data. The system reset and power reset do not reset backup registers. When woken up from Standby mode, backup registers are not reset. HK32F39A provides 43 backup domain data registers (BKP_DR0 to BKP_DR42).

3.17 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs or work as a free running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use the window mode of the IWDG. The original reset value of the IWDG timer is set through option bytes.

3.18 WWDG

The window watchdog (WWDG) is based on a 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.19 SysTick timer

The SysTick timer is a dedicated standard downcounter for the operating system. Its features include:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.20 Basic timer

HK32F39A integrates basic timers TIM6 and TIM7. A basic timer can be used as a 16-bit generic time base or used to generate a DAC trigger signal.

3.21 General-purpose timer

Every general-purpose timer (TIM2/TIM3/TIM4/TIM5) provides a 16-bit auto-reload up/down counter, a 16-bit prescaler, and four independent channels. Every channel can be used for input capture, output compare, PWM output, and one-pulse mode output. General-purpose timers can work with advanced timers through the Timer Link feature for synchronization and event chaining. In debug mode, the counter can be frozen.

The general-purpose timers (except for TIM3) can be used to trigger DAC.

Every general-purpose timer can generate PWM outputs and has its own DMA request mechanism.

The four input channels of TIM2/TIM3/TIM4/TIM5 support triggering on the rising edge, falling edge, or both.

3.22 Advanced timer

HK32F39A integrates the advanced timers TIM1 and TIM8. Each timer can be deemed as a three-phase PWM generator with six channels. It has complementary PWM outputs with programmable inserted dead-times and can be used as a complete general-purpose timer. The four independent channels of each timer can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). In debug mode, the counter can be frozen. Many functions of advanced timers are the same as those of general-purpose timers, and the two types of timers have the same structure. Therefore, the advanced timers can work

together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

TIM8 can be used to trigger DAC.

TIM1 and TIM8 have the following functions:

- CCER[15]: CC4NP bit in the TIM_CCER register for inputting triggers on the rising and falling edges
- CR1[15]: ETR_CLR_SEL bit in the TIM_CR1 register for selecting an external pin or the voltage comparator COMP4 to clear PWM outputs.
- CR1[14]: BRK_SEL bit in the TIM_CR1 register for selecting an external pin or the voltage comparator COMP1/COMP2/COMP3 to output PWM breaks.
- The four input channels of TIM1/TIM8 support triggering on the rising edge, falling edge, or both.

3.23 I2C bus

HK32F39A has two I2C bus interfaces. The I2C bus interface can work as a master or slave and supports the standard and fast modes. The I2C interfaces support the 7-bit and 10-bit addressing modes and 7-bit dual addressing mode when the I2C interface works as the slave. The I2C interfaces embed hardware CRC generation/verification. They can be served by the DMA controller and support SMBus V2.0/PMBus.

3.24 USART

HK32F39A embeds six universal synchronous/asynchronous receivers/transmitters (USART1/USART2/USART3/USART4/USART5/USART6). These interfaces provide asynchronous communications, IrDA SIR ENDEC support, multi-processor communications, single-wire half-duplex communications, and LIN Master/Slave capability.

USART1 and USART6 interfaces can communicate at a speed of up to 7.5 Mbit/s. USART2/USART3/USART4/USART5 interfaces communicate at a speed of up to 3.75 Mbit/s. All the USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (compliant with ISO 7816), and SPI-like communication mode. All USART interfaces can be served by the DMA controller.

3.25 SPI

HK32F39A has three serial peripheral interfaces (SPIs). In master or slave mode, the full-duplex and half-duplex communication speed is up to 18 Mbit/s. The 3-bit prescaler provides eight master mode frequencies. Each frame can be configured to 8-bit or 16-bit. The hardware CRC generation/verification supports the basic SD card and MMC mode.

All SPI interfaces can be served by the DMA controller.

The three SPI interfaces can operate in I2S mode. The three standard I2S interfaces can run in master or slave mode and can be configured to operate with 16-bit, 24-bit, or 32-bit resolution. These interfaces can also be configured as input or output channels. The supported audio sampling frequency ranges from 8 kHz to 192 kHz. If an I2S interface is configured as a master, the master clock can be output to an external DAC or CODEC at 256 times the sampling frequency.

3.26 SDIO

An SD/secure digital input-output (SDIO)/MultiMediaCard (MMC) host interface supports three different data bus modes in MMC System Specification Version 4.2.

- 1-bit (default)
- 4-bit
- 8-bit: In this mode, the interface allows data transfer at up to 48 MHz, and the interface is compliant with SD Memory Card Specification Version 2.0.

SD Memory Card Specification Version 2.0 supports two data bus modes: 1-bit (default) and 4-bit.

The MCU of the current version supports only one SD/SDIO/MMC 4.2 card each time but multiple cards of MMC 4.1 or earlier versions each time. In addition to SD/SDIO/MMC, the interface is compatible with the CE-ATA digital protocol version 1.1.

3.27 CAN

HK32F39A has two independent controller area network (CAN) interfaces. The CAN interfaces are compliant with Specification 2.0A and 2.0B (active). Their highest bit rate is 1 Mbit/s. The CAN interfaces can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN interface has three transmit mailboxes and two 3-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.28 USB

HK32F39A embeds a USB controller that complies with the full-speed USB device standard. The USB interface has software-configurable endpoint settings and suspend/resume support. The dedicated 48 MHz clock for USB is generated by the internal main PLL.

3.29 GPIO

Each GPIO pin can be configured by software as an output pin (push-pull or open-drain), input pin (floating, pull-up, or pull-down), or peripheral alternate function pin. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.30 ADC

HK32F39A embeds three 12-bit ADCs. Every ADC can use up to 16 external channels and can perform the conversion in single or scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow for:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be served by the DMA controller. The analog watchdog function can realize precise monitoring of one, some, or all selected channels. When the monitored signal exceeds the preset threshold, an interrupt is generated. The events generated by general-purpose timers (TIMx) and advanced timers (TIM1/TIM8) can be internally connected to the ADC start trigger events and injection trigger events respectively. The application program then synchronizes the A/D conversion and timers.

The following table lists the relationships between ADC channels and pins:

3.31 DAC

HK32F39A embeds two 12-bit DACs with a buffer. They are used to convert 2-channel digital signals to 2-channel analog voltage signals and output the signals.

The main features of DAC include:

- Two DACs: each corresponds to an output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Update synchronization
- Noise-wave generation
- Triangular-wave generation

- Independent or simultaneous conversions of the two DAC channels
- DMA capability for each channel
- External triggering for conversion
- Input voltage reference V_{REF+}
- HK32F39A has eight DAC trigger inputs. The update outputs of timers can trigger the DAC channel and are connected to different DMA channels.

3.32 Voltage comparator

HK32F39A has four voltage comparators (COMPs):

- Four pairs of voltages are input to four independent voltage comparators via eight I/Os.
- The outputs of the four voltage comparators can be inputs to I/Os or event inputs to timers.
  - The output of one voltage comparator can be the OCREF_CLR event of TIM1 and TIM8.
  - The outputs of the three voltage comparators can be the Break event of TIM1 and TIM8.
- The outputs of the voltage comparators can be event inputs to EXTI for system wakeup and interrupt generation.
- Programmable hysteresis voltage of each voltage comparator: 0 mV or 30 mV
- Voltage comparators have programmable speeds and power modes.
  - Low-speed ultra-low-power mode: the power consumption can be as low as 3 µA.
  - Low-speed low-power mode: the typical power consumption is 5 µA.
  - Medium-speed medium-power mode: the typical power consumption is 40 µA.
  - High-speed high-power mode: the typical power consumption is 100 µA.
- The output polarity of voltage comparators is configurable: high level or low level.

3.33 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.34 DCMI

The digital camera memory interface (DCMI) is a synchronous parallel digital interface that can receive high-speed image and video data from an external CMOS camera module. DCMI has the following features:

- Supports various data formats: YCbCr4:2:2/RGB565 video and JPEG compressed data.
- 8-bit, 10-bit, 12-bit, or 14-bit parallel interface
- Configurable polarity for the pixel clock and synchronization signals
- Supports the sampling of continuous frames or a single frame
- Provides the automatic crop feature
- Supports frame skipping, line skipping, and pixel skipping sampling
- 8-word FIFO

3.35 SAI

The serial audio interface (SAI) complies with most audio interface protocols, such as:

- I2S
- LSB- or MSB-justified
- PCM/DSP

- TDM
- AC'97
- SPDIF
- PDM

The SAI includes two independent audio protocol processing modules. Each module has its independent clock unit and protocol processing unit. You can configure the SAI to work synchronously or independently, work as a master or slave, and work as a transmitter or receiver.

The SAI supports dual-channel/single-channel, μ_law/a_law compression/decompression.

3.36 QSPI interface

The quad serial peripheral interface (QSPI) is a communication interface for single, dual, or quad SPI Flash memories. The QSPI Flash interface can operate in:

- Indirect mode (directly accesses the QSPI registers)
- Status polling mode (periodically reads the external Flash memory status register)
- Memory mapping mode (the external Flash memory is mapped to the MCU address space)

Up to 256 Mbytes of external Flash can be mapped to the MCU address space. Access in 8-bit, 16-bit, and 32-bit is supported. The execution of code is supported. The opcode and frame format are fully programmable. Single data rate (SDR) and double data rate (DDR) are supported.

3.37 TRNG

The true random number generator (TRNG) is a random number generator that provides a 32-bit random number based on continuous analog noise.

TRNG uses an 8 MHz HSI clock. After TRNG is enabled, the TRNG_DR register can be read after about 1,500 clock periods.

- Provides 32-bit random numbers generated by the analog quantity generator.
- The interval at which two random numbers are generated is 40 × TRNG_CLK clock periods.
- The entropy of TRNG is monitored for the identification of exceptional behaviors (generation of stable values or stable value sequences).
- TRNG can be disabled to reduce power consumption.

3.38 AES

HK32F39A integrates an advanced encryption and decryption unit fully compliant with Federal Information Processing Standards 197 (FIPS 197).

- Supported modes: electronic code book (ECB)/cipher block chaining (CBC)/counter mode (CTR).
- Supports the 128-bit, 192-bit, and 256-bit keys for encryption.
- Encryption and decryption computation time:
  - 128-bit key: 57 clock periods
  - 192-bit key: 67 clock periods
  - 256-bit key: 77 clock periods
- Decryption key preparation time:
  - 128-bit key: 57 clock periods
  - 192-bit key: 67 clock periods
  - 256-bit key: 77 clock periods
- Supports the randomization of the AES clock by using TRNG.

- More convenient protection of the register content and easier resumption of the context when interrupts occur.

3.39 Hash

The hash module is applicable to data authentication applications. The hash module is compliant with the following protocols:

- Federal Information Processing Standards Publications 180-2 (FIPS PUB 180-2)
- Secure Hash Algorithm 256 (SHA-256)

When the SHA-256 fast computation processing system is the slave, the input data can be in words, half words, bytes, and bits (little-endian representation).

To adapt to the SHA-256 standard that adopts the big-endian mode, the last input data of little-endian mode is automatically padded to fit the digest minimum block size of 512 bits (16 × 32 bits).

3.40 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32F39A MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, used as a USB string serial number or used by other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot processes that have the security mechanism.

3.41 Debug and trace port

HK32F39A embeds the Arm SWJ-DP which is a combined JTAG-DP and SW-DP. It can realize the connection of a serial wire debug or JTAG probe to a target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively. A specific signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short time.

Note:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- The stress above the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for a long time, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}–V_{SS}	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	3.63	V
V_{IN}	Input voltage on pins	V_{SS} – 0.3	V_{DD}	
$\|\Delta V_{DDx}\|$	Variation between different power pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Variation between different ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	

(1). All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ\,(PIN)}$ is the sum of the absolute instantaneous values of the positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to +150	°C
T_J	Maximum junction temperature	125	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	60	
f_{PCLK2}	Internal APB2 clock frequency	0	120	
V_{DD}	Standard operating voltage	2	3.6	V
V_{DDA}(1)	Analog operating voltage	2	3.6	V
V_{BAT}	Backup operating voltage	1.8	3.6	V
T	Operating temperature	–40	105	℃

(1). It is recommended that you use the same power supply for V_{DD} and V_{DDA}.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0] = 000	2.183	2.188	2.196	V
		PLS[2:0] = 001	2.286	2.289	2.298	
		PLS[2:0] = 010	2.393	2.399	2.407	
		PLS[2:0] = 011	2.502	2.508	2.518	
		PLS[2:0] = 100	2.621	2.629	2.639	
		PLS[2:0] = 101	2.726	2.733	2.745	
		PLS[2:0] = 110	2.839	2.846	2.855	
		PLS[2:0] = 111	2.958	2.969	2.979	
	Programmable voltage detector level selection (falling edge)	PLS[2:0] = 000	2.116	2.119	2.125	
		PLS[2:0] = 001	2.208	2.211	2.220	
		PLS[2:0] = 010	2.305	2.310	2.320	
		PLS[2:0] = 011	2.399	2.406	2.416	
		PLS[2:0] = 100	2.506	2.512	2.521	
		PLS[2:0] = 101	2.596	2.602	2.613	
		PLS[2:0] = 110	2.693	2.701	2.710	
		PLS[2:0] = 111	2.798	2.805	2.817	

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge(2)	1.8	1.88	1.96(3)	V
		Rising edge	1.84 (3)	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset duration	-	1.50	2.50	4.50	ms

(1). PDR is based on the monitoring of V_{DD} and V_{DDA}. POR is based on the monitoring of only V_{DD}.

(2). The actual performance value is guaranteed to be smaller than the minimum $V_{POR/PDR}$ value.

(3). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	0.74	0.8	0.811	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition		V_{DD} = 3.3 V				Unit
			–40°C	25°C	85°C	105°C	
Run mode	CPU operating at 120 MHz; APB clock enabled; Four wait states to access Flash.	Cache enabled	12.18	20.95	22.31	23.44	mA
		Cache disabled	11.2	19.34	20.71	21.82	
	CPU operating at 120 MHz; APB clock disabled; Four wait states to access Flash.	Cache enabled	6.71	11.50	12.74	13.81	mA
		Cache disabled	6.1	10.44	11.66	12.75	
	CPU operating at 8 MHz (HSE); APB clock enabled; Zero wait states to access Flash.	Cache enabled	1.83	1.98	3.08	4.1	mA
		Cache disabled	3.65	3.91	5.06	6.12	
	CPU operating at 8 MHz (HSE); APB clock disabled; Zero wait states to access Flash.	Cache enabled	1.19	1.36	2.39	3.41	mA
		Cache disabled	1.15	1.25	2.32	3.36	
	CPU operating at 40 kHz; APB clock enabled, using the 40 kHz LSI.		0.23	0.31	1.34	2.33	mA
	CPU operating at 32.768 kHz; APB clock enabled, using the 32.768 kHz LSE.		0.23	0.3	1.35	2.32	mA
Sleep mode	CPU paused; APB clock enabled, using the 120 MHz clock.		8.52	14.63	15.92	17.01	mA
	CPU paused; APB clock disabled, using the 120 MHz clock.		3.3	5.65	6.82	7.85	mA
	CPU paused; APB clock enabled, using the 8 MHz HSI.		1.56	1.69	2.95	3.72	mA
	CPU paused; APB clock disabled, using the 8 MHz HSI.		0.88	1.01	2.85	3.04	mA
Stop mode	CPU paused; LDO operating at full speed; HSE/HSI/LSE disabled; IWDG disabled.		202.67	303	1322	2179	µA
	CPU paused; LDO in the low-power state; HSE/HSI/LSE disabled, IWDG disabled.		18.38	89.47	729	1374	µA
Standby mode	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; The Standby circuitry works as normal; LSI oscillator enabled; IWDG enabled.		2.98	3.87	16.74	30.29	µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; The Standby circuitry works as normal; LSI oscillator disabled; IWDG disabled.		2.96	3.87	16.68	30.22	µA
	CPU powered off, internal LDO disabled, core domain		2.35	3.36	16.16	29.72	µA

Mode	Condition	V_{DD} = 3.3 V				Unit
		–40°C	25°C	85°C	105°C	
	(including CPU, SRAM, Flash, registers) powered off; The Standby circuitry works as normal; HSE, HSI, LSE, and LSI disabled.					
Shutdown mode	CPU paused, LSE enabled, RTC running (BKPPDS = 0)	1.7	2.67	11.98	21.87	µA
	CPU paused, LSE disabled, RTC disabled (BKPPDS = 1)	0.04	0.09	0.62	1.60	µA
	CPU paused, LSE disabled, RTC stopped (BKPPDS = 0)	1.31	2.19	11.41	21.27	µA
V_{BAT}	CPU paused, LSE/LSI enabled, RTC running	1.7	2.67	11.98	25.86	µA
	CPU paused, LSE/LSI enabled, RTC stopped	1.31	2.19	11.41	21.27	µA

4.2.6 HSE clock characteristics

Table 4-9 HSE oscillator circuit characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{crystal}$(1)	Crystal oscillator frequency range supported by the oscillator circuit	-	4	-	32	MHz

(1). The value is guaranteed in design.

HK32F39A integrates an HSE crystal oscillator circuit with negative feedback. The following oscillator circuit outside the chip is recommended:

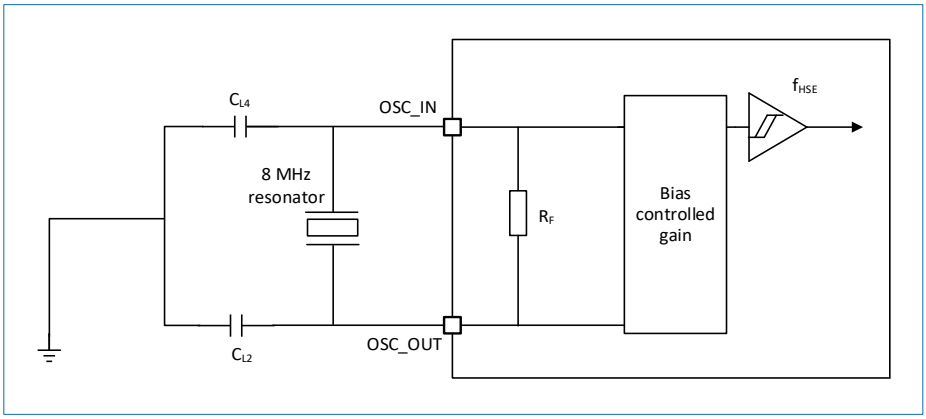


Figure 4-1 Recommended oscillator circuit outside the chip

When HSE is configured to bypass mode, the HSE oscillator circuit is disabled. The OSC_IN pin can work as a clock input pin from which an external clock signal is input. The following table describes the requirements for this clock signal.

Table 4-10 Characteristics of the clock signal input from OSC_IN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}(1)	Frequency	-	-	-	64	MHz
V_{HSEH}	High level voltage on the OSN_IN input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the OSN_IN input pin		V_{SS}	-	0.3 × V_{DD}	
$Tw_{(HSE)}$	Effective high/low level duration		5	-	-	ns
$Tr_{(HSE)}$/$Tf_{(HSE)}$	Rise/Fall time		-	-	20	
$Cin_{(HSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.7 LSE clock characteristics

Table 4-11 LSE oscillator circuit characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{crystal}$(1)	Crystal oscillator frequency range supported by the oscillator circuit	-	-	32.768	-	kHz
R_F(1)	Feedback resistor	-	-	2		MΩ
T_{stb}	Oscillator startup time(2)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	2000	ms
C(1)	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12.5	-	pF
g_m	Oscillator transconductance	Started	-	-	-	
I_2(1)	LSE driving current	-	-	400	-	nA

(1). The value is guaranteed in design.

(2). T_{stb} refers to the time from LSE startup to the time when it outputs stable frequency signals.

HK32F39A integrates an LSE crystal oscillator circuit with negative feedback. The following oscillator circuit outside the chip is recommended:

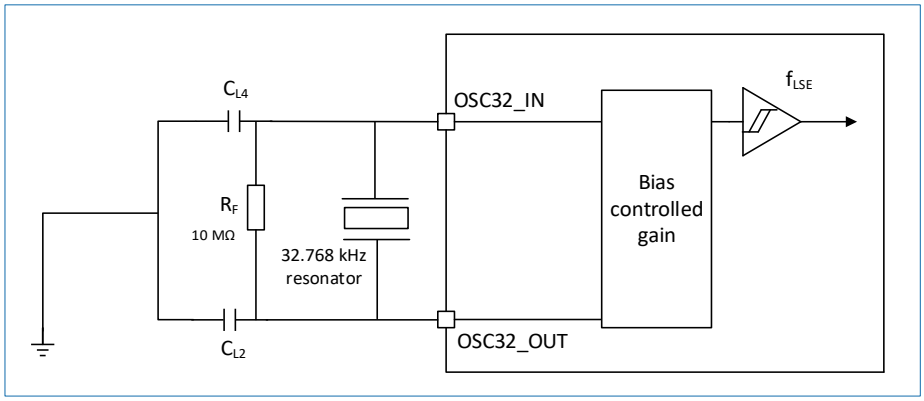


Figure 4-2 Recommended oscillator circuit outside the chip

When LSE is configured to bypass mode, the LSE oscillator circuit is disabled. The OSC32_IN pin can work as a clock input pin from which an external clock signal is input. The following table describes the requirements for this clock signal.

Table 4-12 Characteristics of the clock signal input from OSC32_IN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{LSE_ext}	Frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the OSN32_IN input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	Low level voltage on the OSN32_IN input pin		V_{SS}	-	0.3 × V_{DD}	
$Tw_{(LSE)}$	Effective high/low level duration		450	-	-	ns
$Tr_{(LSE)}/Tf_{(LSE)}$	Rise/Fall time		-	-	50	
$Cin_{(LSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.8 HSI clock characteristics

Table 4-13 Characteristics of the HSI clock

Symbol	Parameter	Condition		Min	Typ	Max	Unit
F_{HSI} RC 56	RC oscillator	-		-	56	-	MHz
f_{HSI}	Frequency	-		-	8	-	
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	HSI oscillator accuracy	Factory trimmed accuracy (ambient temperature)		–1	-	1	
		Factory calibrated	TA= –40°C to 105°C	-	-	2.5	%
			TA= –40°C to 85°C	-	-	2.2	%
			TA = 0°C to 70°C	-	-	2	%
$Tsu_{(HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$I_{DD(HSI)}$	Oscillator power consumption	-		-	80	100	µA

4.2.9 LSI clock characteristics

Table 4-14 Characteristics of the LSI clock

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$tsu_{(LSI)}$	Oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$	Oscillator power consumption	-	0.65	1.2	µA

4.2.10 PLL characteristics

Table 4-15 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	8	80	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	120	MHz
t_{LOCK}	PLL lock time	-	80	120	µs
Jitter	Cycle-to-cycle jitter	-	5	13	ps

4.2.11 GPIO input clock

HK32F39A is clocked from PA1, PB1, PC7, PB7 input clock.

Table 4-16 GPIO input clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{ext}	Input clock frequency	1	8	64	MHz
	Input clock duty cycle	40	-	60	%

4.2.12 Flash memory characteristics

Table 4-17 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-byte programming time	6	-	7.5	µs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
IDD_{PROG}	One-byte programming current	-	-	5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Supply current@24 MHz (read mode)	-	2	3	mA
	Supply current@1 MHz (read mode)	-	0.25	0.4	mA
N_{END}	Erasure endurance	100,000			Cycles

Symbol	Parameter	Min	Typ	Max	Unit
t_{RET}	Data retention	20			Years

4.2.13 I/O pin input characteristics

Table 4-18 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	1.6	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.5	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	1.56	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.26	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	300	-	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V 0 < V_{IN} < 3.3 V	-	0.01	1	μA
		V_{DD} = 3.3 V V_{IN} = 5 V	-	0.02	1	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	35	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	35	-	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.14 I/O pin output characteristics

Table 4-19 I/O pin output direct current characteristics

Mode[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	V
	V_{OH}	Output high level voltage		-	125	V
01	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	V
	V_{OH}	Output high level voltage		-	125	V
11	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	V
	V_{OH}	Output high level voltage		-	125	V

Table 4-20 I/O pin output alternating current characteristics

Mode[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	5	ns
	$tr_{(IO)out}$	Output low to high level rise time		-	5	ns

4.2.15 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC

circuit or no circuit.

Table 4-21 NRST pin input characteristics

Symbol	Parameter	Min	Max	Unit
T_{Noise}	Low level ignored duration	-	265	ns

4.2.16 TIM timer characteristics

Table 4-22 TIM characteristics

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2^{(1)}$	MHz

(3). $F_{TIMxCLK}$ = 120 or 60 MHz

4.2.17 QSPI characteristics

Table 4-23 QSPI characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ck}	QSPI clock frequency	2.7 V < V_{DD} < 3.6 V C_{load} = 30 pF	-	30	-	MHz
$t_{w(CKH)}$	QSPI clock high time	f_{AHBCLK} = 120 MHz, presc = 0	$t_{(ck)}/2 - 2$	-	$t_{(ck)}/2$	ns
$t_{w(CKL)}$	QSPI clock low time		$t_{(ck)}/2$	-	$t_{(ck)}/2 + 2$	ns
$t_{s(IN)}$	Data in set up time	-	8	-	-	ns
$t_{h(IN)}$	Data in hold time	-	5	-	-	ns
$t_{v(OUT)}$	Data output valid time	--	-		5.5	ns
$t_{h(OUT)}$	Data out hold time	-	0	-	-	ns

4.2.18 ADC characteristics

Table 4-24 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Reference input current	-	-	150	480	µA
INL	Integral non linearity (maximum difference between the actual conversion point and the end point correlation line)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1.5	±4	LSB
DNL	Differential non linearity (maximum difference between actual steps and the ideal one)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1	±3	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} grounded)	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}	Sampling and hold capacitor	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs

Item	Description	Condition	Min	Typ	Max	Unit
		-	83			$1/f_{ADC}$
t_{lat}	Input trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	μs
		-	-	-	3	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	μs
		-	-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	μs
		-	1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	μs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	μs
		-	14 to 252 (sampling time t_S + 12.5 for successive approximation)			$1/f_{ADC}$

4.2.19 DAC characteristics

Table 4-25 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	2.0	3.3	3.6	V
V_{REF+}	Reference supply voltage	2.0	3.3	3.6	V
V_{SSA}	Ground	0	0	0	V
R_{LOAD}	Resistive load with buffer enabled	5	-	-	kΩ
R_O	Impedance output with buffer disabled	-	15	-	kΩ
C_{LOAD}	Capacitive load	-	-	-	pF
DAC_OUT min	Lower DAC_OUT voltage with buffer enabled	0.1	-	-	V
DAC_OUT max	Higher DAC_OUT voltage with buffer enabled	-	-	V_{DD} – 0.1	V
DAC_OUT min	Lower DAC_OUT voltage with buffer disabled	0	-	-	mV
DAC_OUT max	Higher DAC_OUT voltage with buffer disabled	-	-	V_{REF}	V
$I_{DDVREF+}$	DAC direct current consumption in quiescent mode (standby mode)	108	135	162	μA
I_{DDA}	DAC direct current consumption in quiescent mode	-	-	429	μA
DNL	Differential non linearity (difference between two consecutive code – 1 LSB)	-	-	±1	LSB
INL	Integral non linearity (difference between measured value at code i and the value at code i on a line drawn between code 0 and last code 1023)	-	-	±4	LSB
		-	-	±4	LSB
Offset	Offset error (difference between the measured value at code 0x800 and the ideal value $V_{REF+}/2$)	-	-	±10	mV
		-	-	±12	LSB
Gain error	Gain error	-	-	±0.5	%
$t_{SETTLING}$	Settling time (full scale: when DAC_OUT reaches the final value ±1LSB, the transition for a 10-bit input code from the minimum to the maximum)	-	3	4	μs
Update rate	Maximum frequency of obtaining a correct DAC_OUT change when the input code changes slightly (from code i to i + 1LSB)	-	-	1	MS/s
t_{WAKEUP}	Wakeup time from the off state (setting the ENx bit in the DAC control register)	-	6.5	10	μs

Symbol	Parameter	Min	Typ	Max	Unit
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB

4.2.20 Temperature sensor characteristics

Table 4-26 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L	Temperature linearity	-		±1	±2	℃
V_{25}	Output voltage	25℃	0.76	0.909	0.94	V
Avg_Slope	Average slope	-	2.9	3	3.1	mV/℃

5 Typical circuitry

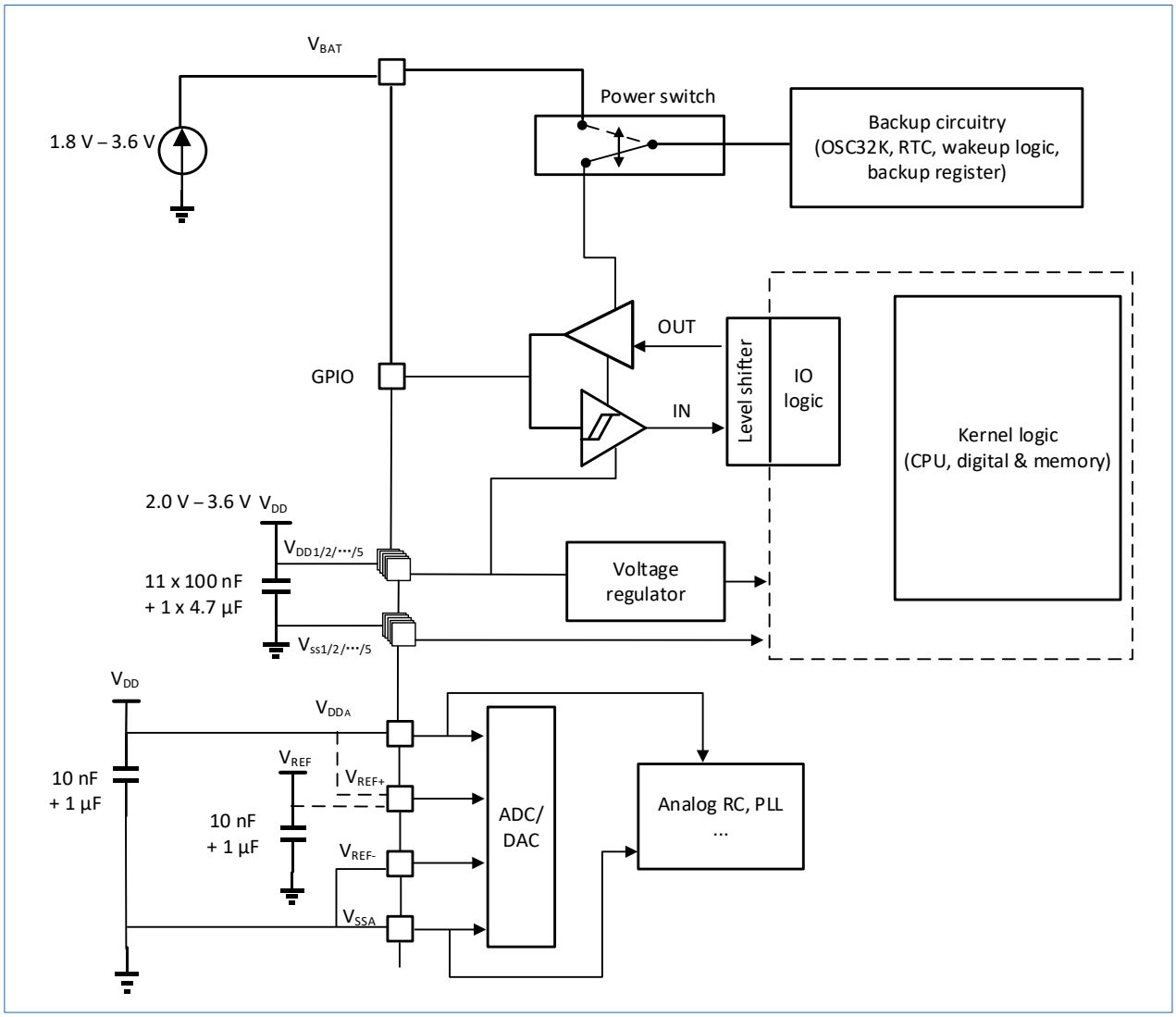


Figure 5-1 Power supply scheme

6 Pinouts and pin descriptions

HK32F39A MCUs are delivered in two packages: LQFP64 and LQFP100.

6.1 LQFP64

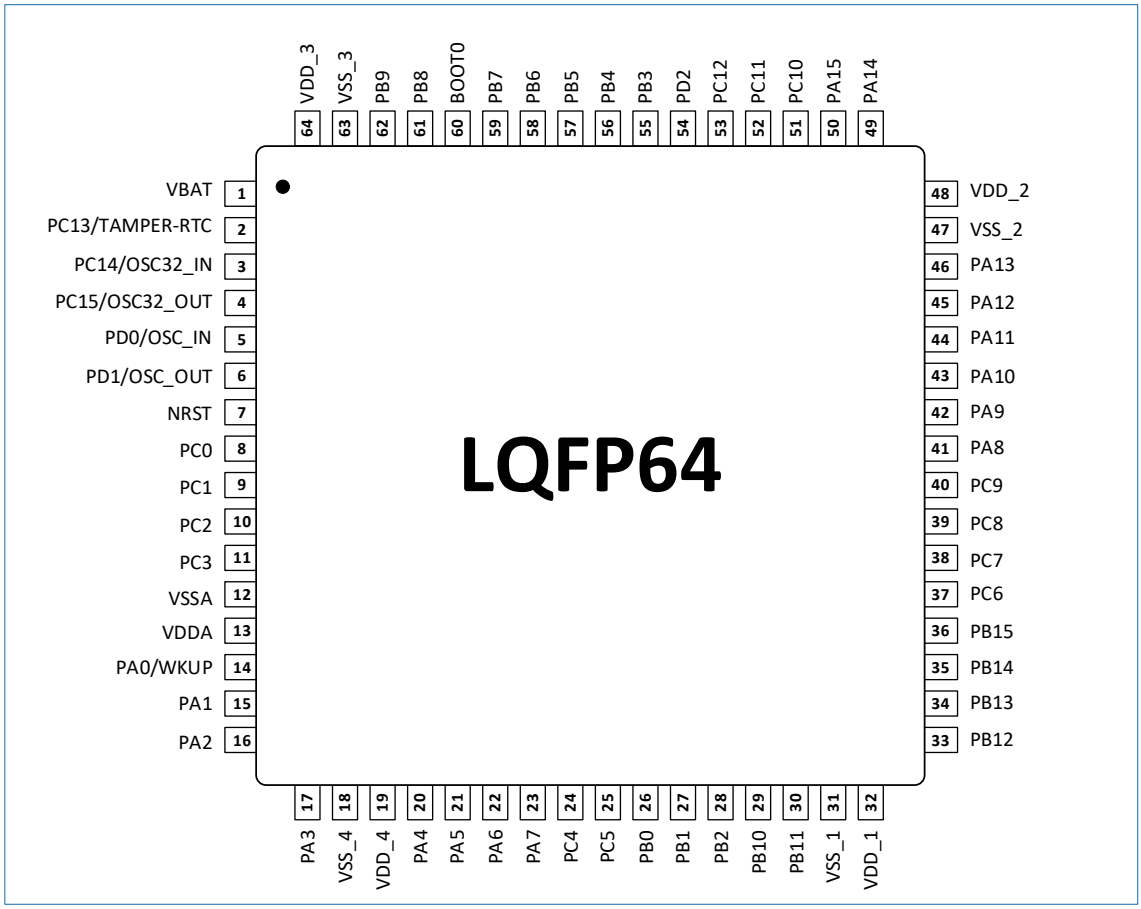


Figure 6-1 LQFP64 package pinout

6.2 LQFP100

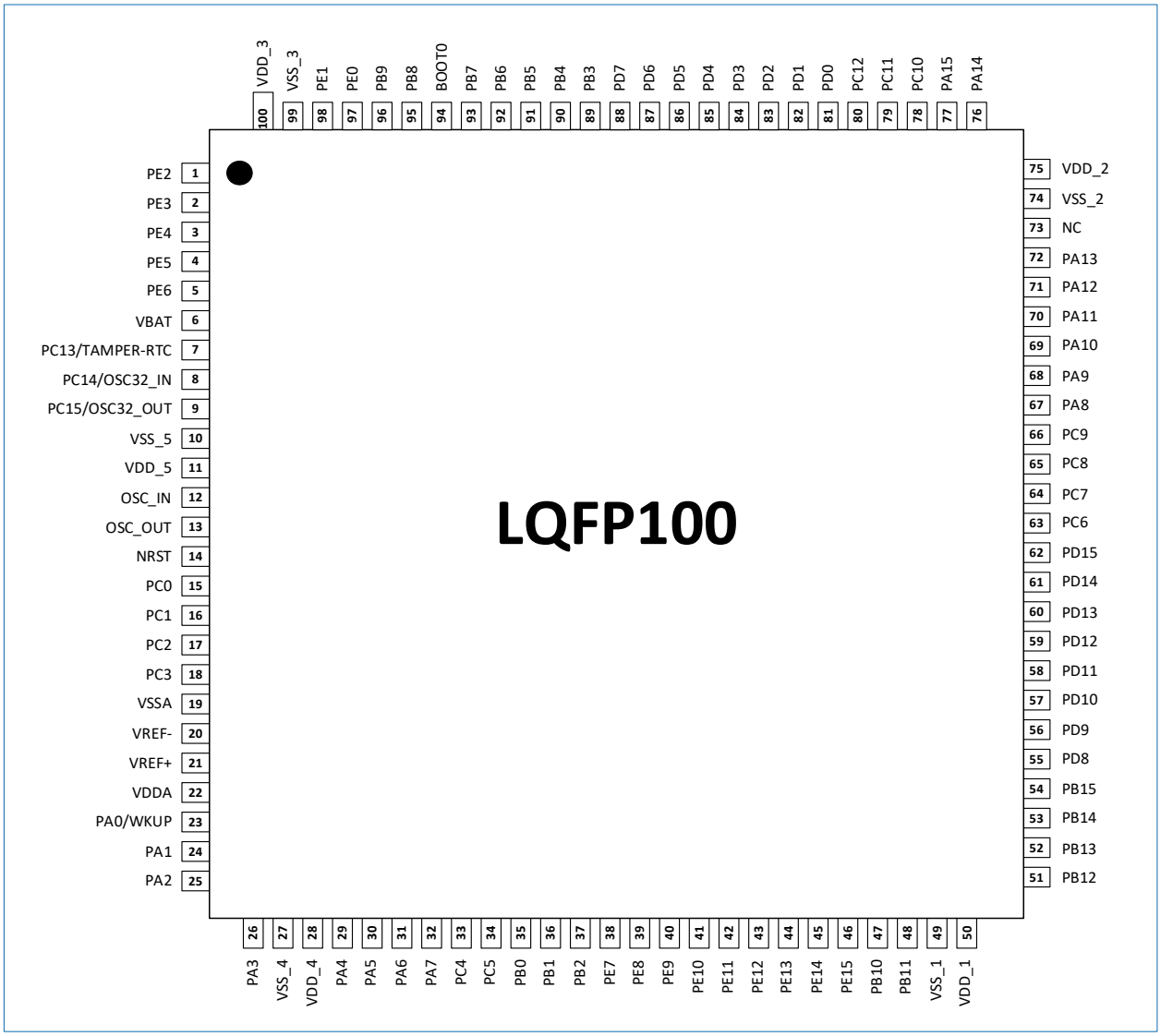


Figure 6-2 LQFP100 package pinout

6.3 LQFP64/LQFP100 pin description

The following table shows pin descriptions of LQFP64 and LQFP100 packages.

Table 6-1 LQFP64/LQFP100 pin description

LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
-	1	PE2	I/O	-	TRACECKO/FSMC_A23/ADC2_IN17	TXEV/EXTIN2/SAI_MCLK_A
-	2	PE3	I/O	-	TRACEDO0/FSMC_A19/ADC2_IN18	TXEV/EXTIN3
-	3	PE4	I/O	-	TRACEDO1/FSMC_A20/ADC3_IN17	TXEV/EXTIN4/SAI_FS_A
-	4	PE5	I/O	-	TRACEDO2/FSMC_A21/ADC3_IN18	TXEV/EXTIN5/SAI_SCK_A
-	5	PE6	I/O	FT	TRACEDO3/FSMC_A22	TXEV/EXTIN6/SAI_SD_A
1	6	VBAT	S	-	-	-
2	7	PC13/TAMPER-RTC	I/O(3)	-	TAMPER-RTC/WKUP1/RTCO/ QSPI_BK1_NCS	TXEV/EXTIN13
3	8	PC14/OSC32_IN (PC14)	I/O(3)	-	OSC32_IN/LSE_CKI	TXEV/EXTIN14
4	9	PC15/OSC32_O	I/O(3)	-	OSC32_OUT	TXEV/EXTIN15

LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
		UT (PC15)				
-	10	VSS_5	S	-	-	-
-	11	VDD_5	S	-	-	-
5	-	PD0/OSC_IN (OSC_IN)	I/O	-	OSC_IN/HSE_CKI	TXEV/PD0/EXTIN0/CAN1_RX
6	-	PD1/OSC_OUT (OSC_OUT)	I/O	-	OSC_OUT	TXEV/PD1/EXTIN1/CAN1_TX
-	12	OSC_IN	I	-	OSC_IN/HSE_CKI	-
-	13	OSC_OUT	O	-	OSC_OUT	-
7	14	NRST	I/O	-	-	-
8	15	PC0	I/O	-	ADC123_IN10/DCMI_PIXCLK	TXEV/EXTIN0/FSMC_A13
9	16	PC1	I/O	-	ADC123_IN11/DCMI_PIXDI13/ TFT_DEN1	TXEV/EXTIN1
10	17	PC2	I/O	-	ADC123_IN12/DCMI_PIXDI12/ TFT_VSYNC1	TXEV/EXTIN2
11	18	PC3	I/O	-	ADC123_IN13/DCMI_PIXDI11/ TFT_HSYNC1	TXEV/EXTIN3
12	19	VSSA	S	-	-	-
	20	VREF-	S	-	-	-
	21	VREF+	S	-	-	-
13	22	VDDA	S	-	-	-
14	23	PA0/WKUP (PA0)	I/O (3)	-	WKUP0/USART2_CTS/ADC123_IN0/ TIM2_CH1_ETR/TIM5_CH1/ TIM8_ETR/EXTIN0/DCMI_PIXDI10	TXEV/FSMC_NE4
15	24	PA1	I/O	-	USART2_RTS/ADC123_IN1/ TIM5_CH2/TIM2_CH2/EXTIN1/ RCC_CKI0/DCMI_PIXDI9	TXEV/FSMC_A14
16	25	PA2	I/O	-	USART2_TX/TIM5_CH3/ADC123_IN 2/TIM2_CH3/EXTIN2/TFT_DCLK	TXEV
17	26	PA3	I/O	-	USART2_RX/TIM5_CH4/ ADC123_IN3/TIM2_CH4/EXTIN3/ DCMI_PIXDI8/SAI_MCLK_A	TXEV/FSMC_A15
18	27	VSS_4	S	-	-	-
19	28	VDD_4	S	-	-	-
20	29	PA4	I/O	-	SPI1_NSS/USART2_CK/DAC1_OUT/ ADC12_IN4/EXTIN4/TFT_DEN2/ I2S1_WS/TIM5_ETR/SAI_FS_B	TXEV
21	30	PA5	I/O	-	SPI1_SCK/DAC2_OUT/ADC12_IN5/ EXTIN5/TFT_VSYNC2/I2S1_CK/ SAI_MCLK_B	TXEV
22	31	PA6	I/O	-	SPI1_MISO/TIM8_BKIN/ADC12_IN6 / TIM3_CH1/EXTIN6/TFT_HSYNC2/ SAI_SCK_B	TXEV/TIM1_BKIN
23	32	PA7	I/O	-	SPI1_MOSI/TIM8_CH1N/ADC12_IN 7/TIM3_CH2/EXTIN7/DCMI_PIXDI7 /	TXEV/TIM1_CH1N/FSMC_A0

LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
					I2S1_SD/SAI_SD_B	
24	33	PC4	I/O	-	ADC12_IN14/DCMI_PIXDI6/ I2S1_MCK	TXEV/EXTIN4/FSMC_A1
25	34	PC5	I/O	-	ADC12_IN15/DCMI_PIXDI5	TXEV/EXTIN5/FSMC_A2
26	35	PB0	I/O (3)	-	ADC12_IN8/TIM3_CH3/TIM8_CH2 N/WKUP2/DCMI_PIXDI4	TXEV/TIM1_CH2N/EXTIN0/ FSMC_A3/CAN2_RX
27	36	PB1	I/O	-	ADC12_IN9/TIM3_CH4/TIM8_CH3 N/RCC_CKI1/DCMI_PIXDI3	TXEV/TIM1_CH3N/EXTIN1/ FSMC_A4/CAN2_TX
28	37	PB2	I/O	FT	BOOT1(4)/QSPI_BK1_IO0/USART6_C K	TXEV/EXTIN2/FSMC_A5/ SAI_SD_A
-	38	PE7	I/O	FT	FSMC_D4	TXEV/TIM1_ETR/EXTIN7/ SAI_SD_B
-	39	PE8	I/O	FT	FSMC_D5	TXEV/TIM1_CH1N/EXTIN8/ SAI_SCK_B
-	40	PE9	I/O	FT	FSMC_D6	TXEV/TIM1_CH1/EXTIN9/ SAI_FS_B
-	41	PE10	I/O	FT	FSMC_D7	TXEV/TIM1_CH2N/EXTIN10/ SAI_MCLK_B
-	42	PE11	I/O	FT	FSMC_D8	TXEV/TIM1_CH2/EXTIN11
-	43	PE12	I/O	FT	FSMC_D9	TXEV/TIM1_CH3N/EXTIN12
-	44	PE13	I/O	FT	FSMC_D10	TXEV/TIM1_CH3/EXTIN13
-	45	PE14	I/O	FT	FSMC_D11	TXEV/TIM1_CH4/EXTIN14
-	46	PE15	I/O	FT	FSMC_D12	TXEV/TIM1_BKIN/EXTIN15
29	47	PB10	I/O	-	I2C2_SCL/USART3_TX/COMP1_O	TXEV/TIM2_CH3/EXTIN10/ FSMC_INT2/SAI_SCK_A
30	48	PB11	I/O	-	I2C2_SDA/USART3_RX/COMP2_O	TXEV/TIM2_CH4/EXTIN11/ FSMC_INT3
31	49	VSS_1	S	-	-	-
32	50	VDD_1	S	-	-	-
33	51	PB12	I/O	FT	SPI2_NSS/I2S2_WS/I2C2_SMBA/ USART3_CK/TIM1_BKIN/ DCMI_PIXDI2/TFT_DEN3/ADC3_IN1 6/CAN2_RX	TXEV/EXTIN12
34	52	PB13	I/O	FT	SPI2_SCK/I2S2_CK/USART3_CTS/ TIM1_CH1N/DCMI_PIXDI1/ TFT_VSYNC3/CAN2_TX/USART6_TX	TXEV/EXTIN13
35	53	PB14	I/O	FT	SPI2_MISO/TIM1_CH2N/ USART3_RTS/DCMI_PIXDI0/ TFT_HSYNC3/USART6_RX	TXEV/EXTIN14
36	54	PB15	I/O	FT	SPI2_MOSI/I2S2_SD/TIM1_CH3N/ USART4_CK	TXEV/EXTIN15/FSMC_INTR
-	55	PD8	I/O	FT	FSMC_D13	TXEV/USART3_TX/EXTIN8
-	56	PD9	I/O	FT	FSMC_D14	TXEV/USART3_RX/EXTIN9
-	57	PD10	I/O	FT	FSMC_D15	TXEV/USART3_CK/EXTIN10
-	58	PD11	I/O	FT	FSMC_A16_CLE	TXEV/USART3_CTS/EXTIN11
-	59	PD12	I/O	FT	FSMC_A17_ALE	TXEV/TIM4_CH1/USART3_RTS/ EXTIN12
-	60	PD13	I/O	FT	FSMC_A18	TXEV/TIM4_CH2/EXTIN13

LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
-	61	PD14	I/O	FT	FSMC_D0	TXEV/TIM4_CH3/EXTIN14
-	62	PD15	I/O	FT	FSMC_D1	TXEV/TIM4_CH4/EXTIN15
37	63	PC6	I/O	FT	I2S2_MCK/TIM8_CH1/SDIO_D6/ USART4_CTS	TXEV/TIM3_CH1/EXTIN6/ FSMC_A6
38	64	PC7	I/O	FT	I2S3_MCK/TIM8_CH2/SDIO_D7/ RCC_CKI2/USART4_RTS	TXEV/TIM3_CH2/EXTIN7/ FSMC_A7
39	65	PC8	I/O	FT	TIM8_CH3/SDIO_D0	TXEV/TIM3_CH3/EXTIN8/ FSMC_A8/USART1_CTS/ USART5_TX
40	66	PC9	I/O	FT	TIM8_CH4/SDIO_D1	TXEV/TIM3_CH4/EXTIN9/ FSMC_A9/USART1_RTS/ USART5_RX
41	67	PA8	I/O	FT	USART1_CK/TIM1_CH1/RCC_MCO/ EXTIN8/QSPI_BK1_IO1/SAI_SCK_A	TXEV/FSMC_A10
42	68	PA9	I/O	FT	USART1_TX/TIM1_CH2/EXTIN9/ QSPI_BK1_IO2/SAI_FS_A	TXEV/FSMC_A11
43	69	PA10	I/O	FT	USART1_RX/TIM1_CH3/EXTIN10/ QSPI_BK1_IO3/SAI_SD_A	TXEV/FSMC_A12
44	70	PA11	I/O	FT	USART1_CTS/USB_DM/CAN1_RX/ TIM1_CH4/EXTIN11/DCMI_VYSNC	TXEV
45	71	PA12	I/O	FT	USART1_RTS/USB_DP/CAN1_TX/ TIM1_ETR/EXTIN12/DCMI_HYSNC	TXEV
46	72	PA13/JTMS-SWDIO (JTMS-SWDIO)	I/O	FT	USART6_CTS	TXEV/PA13/DCMI_VYSNC/ FSMC_NIORD
-	73	NC	-	-	-	-
47	74	VSS_2	S	-	-	-
48	75	VDD_2	S	-	-	-
49	76	PA14/JTCK-SWCLK (JTCK-SWCLK)	I/O	FT	EXTIN14/USART5_CK	TXEV/PA14/FSMC_NIOWR/ USART2_CTS/I2C1_SMBA/ DCMI_HYSNC
50	77	PA15/JTDI (JTDI)	I/O	FT	SPI3_NSS/I2S3_WS/EXTIN15/ QSPI_CKO/USART6_RTS	TXEV/PA15/TIM2_CH1_ETR/ SPI1_NSS/I2S1_WS/ FSMC_NREG/USART2_RTS
51	78	PC10	I/O	-	USART4_TX/SDIO_D2/COMP1_N	TXEV/USART3_TX/EXTIN10/ FSMC_A24/USART2_TX
52	79	PC11	I/O	-	USART4_RX/SDIO_D3/COMP1_P	TXEV/USART3_RX/EXTIN11/ FSMC_A25/USART2_RX
53	80	PC12	I/O	-	USART5_TX/SDIO_CK/COMP2_N	TXEV/USART3_CK/EXTIN12/ FSMC_NE2_NCE3/USART2_CK
-	81	PD0	I/O	FT	FSMC_D2	TXEV/CAN1_RX/EXTIN0
-	82	PD1	I/O	FT	FSMC_D3	TXEV/CAN1_TX/EXTIN1
54	83	PD2	I/O	-	TIM3_ETR/USART5_RX/SDIO_CMD/ COMP2_P	TXEV/EXTIN2/ FSMC_NE3_NCE4_1
-	84	PD3	I/O	FT	FSMC_CLK/USART5_CTS	TXEV/USART2_CTS/EXTIN3/ SPI3_NSS/I2S3_WS
-	85	PD4	I/O	FT	FSMC_NOE/USART5_RTS	TXEV/USART2_RTS/EXTIN4/ SPI3_SCK/I2S3_CK

LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
-	86	PD5	I/O	FT	FSMC_NWE	TXEV/USART2_TX/EXTIN5/ SPI3_MISO
-	87	PD6	I/O	FT	FSMC_NWAIT	TXEV/USART2_RX/EXTIN6/ SPI3_MOSI/I2S3_SD
-	88	PD7	I/O	FT	FSMC_NE1/FSMC_NCE2	TXEV/USART2_CK/EXTIN7
55	89	PB3/JTDO (JTDO)	I/O	-	TRACESWO/SPI3_SCK/I2S3_CK/ TFT_DEN4/QSPI_BK2_NCS/ADC3_IN5/COMP3_N	TXEV/PB3/TIM2_CH2/SPI1_SCK /I2S1_CK/EXTIN3/DCMI_PIXDI13/SAI_SCK_B
56	90	PB4/NJRST (NJRST)	I/O	-	SPI3_MISO/TFT_VSYNC4/ QSPI_BK2_IO0/ADC3_IN6/COMP3_P	TXEV/PB4/TIM3_CH1/ SPI1_MISO/EXTIN4/ DCMI_PIXDI12/SAI_MCLK_B
57	91	PB5	I/O	-	I2C1_SMBA/SPI3_MOSI/I2S3_SD/ TFT_VSYNC4/QSPI_BK2_IO1/ ADC3_IN7/COMP4_N	TXEV/TIM3_CH2/SPI1_MOSI/ I2S1_SD/EXTIN5/ DCMI_PIXDI11/CAN2_RX/ SAI_SD_B
58	92	PB6	I/O	-	I2C1_SCL/TIM4_CH1/QSPI_BK2_IO2/ADC3_IN8/COMP4_P	TXEV/USART1_TX/EXTIN6/ DCMI_PIXDI10/FSMC_NCE4_2/ CAN2_TX/I2S1_MCK/SAI_FS_B
59	93	PB7	I/O	FT	I2C1_SDA/FSMC_NADV/TIM4_CH2/ RCC_CKI3/QSPI_BK2_IO3	TXEV/USART1_RX/EXTIN7
60	94	BOOT0(4)	I	-	-	-
61	95	PB8	I/O	-	TIM4_CH3/SDIO_D4/COMP3_O	TXEV/I2C1_SCL/CAN1_RX/ EXTIN8/FSMC_CD/USART4_TX/ SAI_MCLK_A
62	96	PB9	I/O	-	TIM4_CH4/SDIO_D5/COMP4_O	TXEV/I2C1_SDA/USART4_RX/ CAN1_TX/EXTIN9/SAI_FS_A
-	97	PE0	I/O	FT	TIM4_ETR/FSMC_NBL0	TXEV/EXTIN0
-	98	PE1	I/O	FT	FSMC_NBL1	TXEV/EXTIN1
63	99	VSS_3	S	-	-	-
64	100	VDD_3	S	-	-	-

(1). I = input, O = output, I/O = input/output, S = supply.

(2). FT: 5 V tolerant.

(3). Except for these pins, the other I/O pins have the Schmitt function and can be configured via registers.

(4). BOOT0/BOOT1 pin is connected to an internal weak pull-down resistor.

7 Package characteristics

7.1 Package outlines

7.1.1 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch, 64-pin low-profile quad flat package.

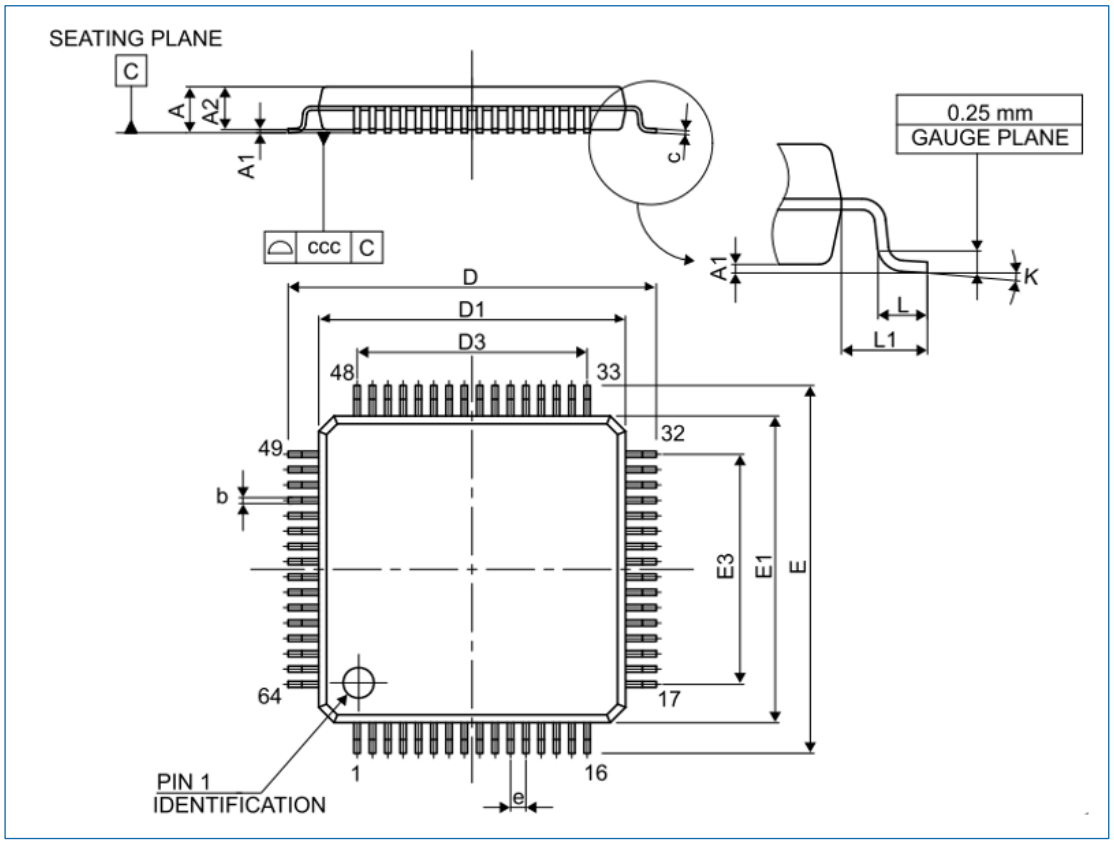


Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches) (1)	Max (inches) (1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP100

LQFP100 is a 14 mm × 14 mm, 0.5 mm pitch, 100-pin low-profile quad flat package.

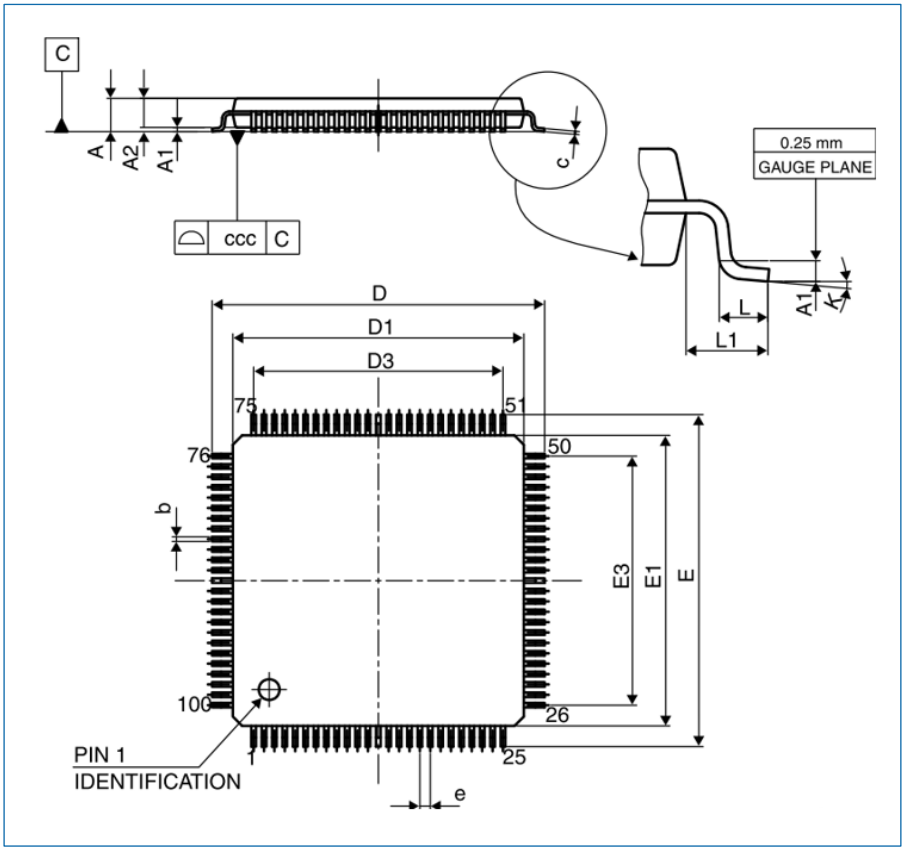


Figure 7-2 LQFP100 package outline

Table 7-2 LQFP100 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches) (1)	Max (inches) (1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-3 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP64 marking

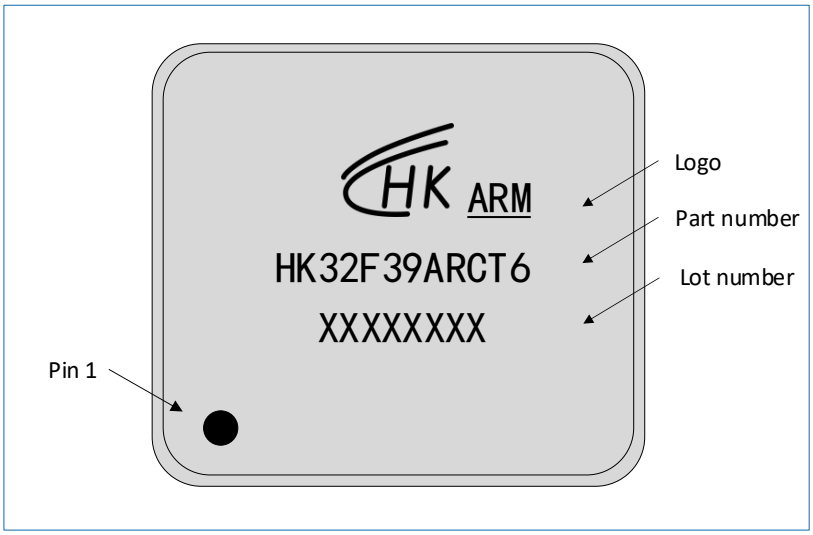


Figure 7-3 LQFP64 HK32F39ARCT6 marking example

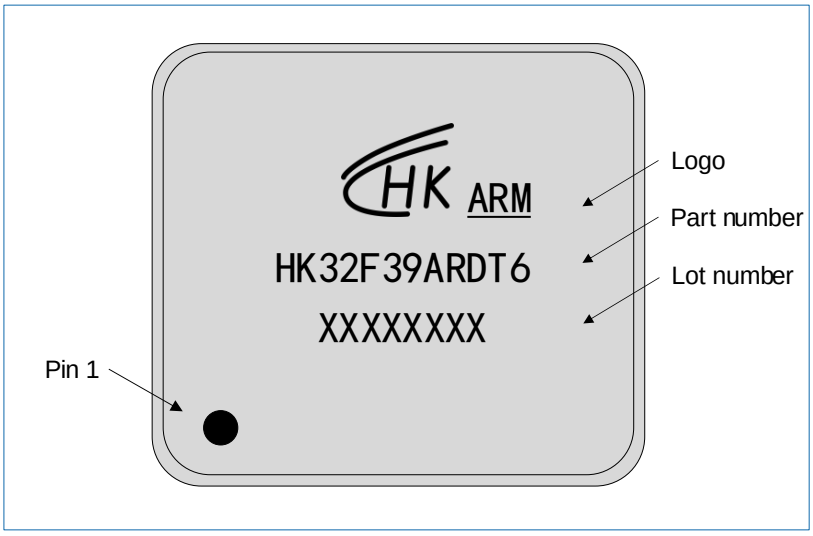


Figure 7-4 LQFP64 HK32F39ARDT6 marking example

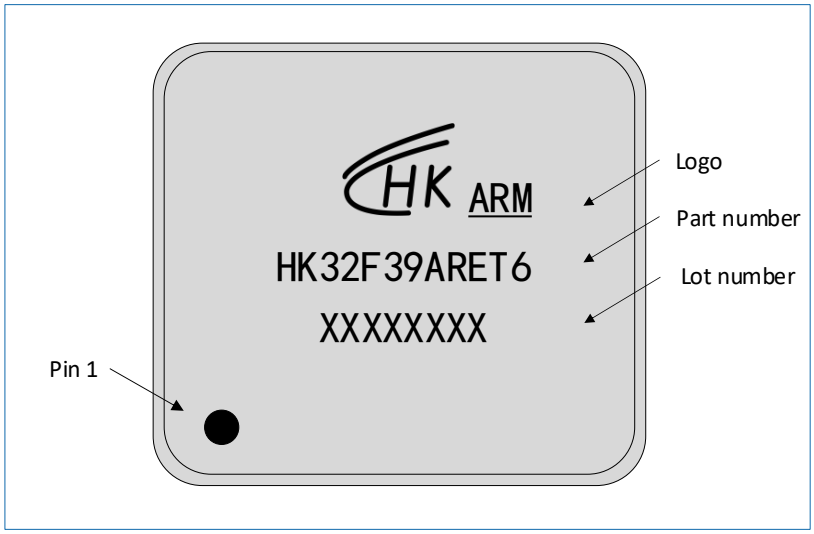


Figure 7-5 LQFP64 HK32F39ARET6 marking example

7.2.2 LQFP100 marking

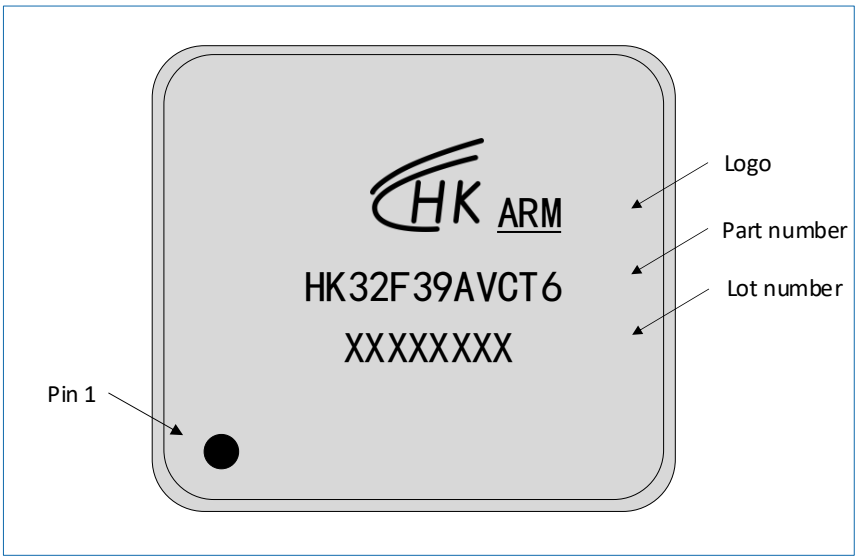


Figure 7-6 LQFP100 HK32F39AVCT6 marking example

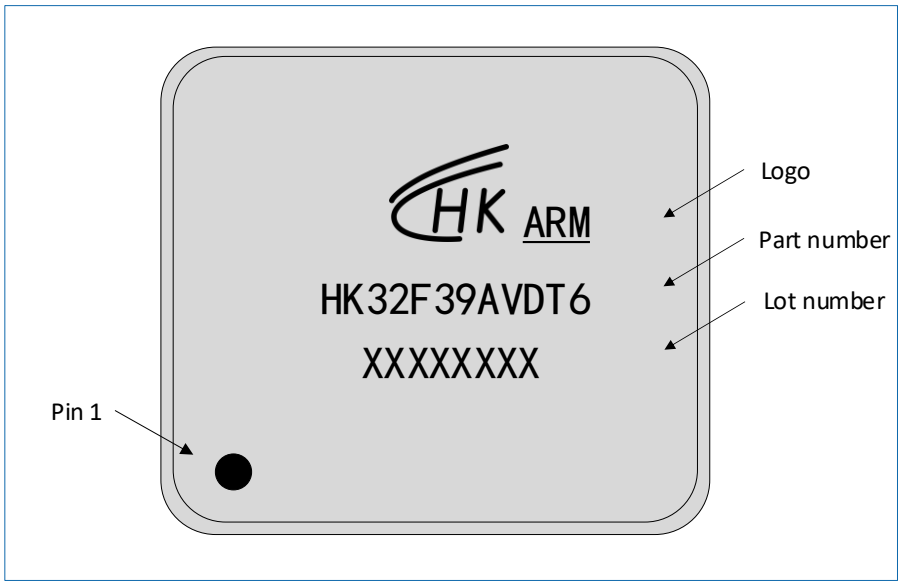


Figure 7-7 LQFP100 HK32F39AVDT6 marking example

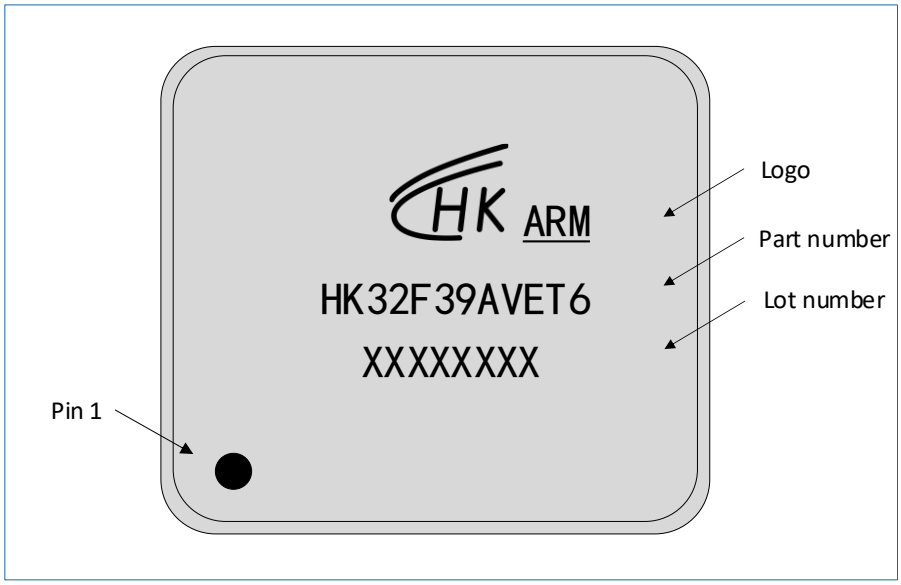
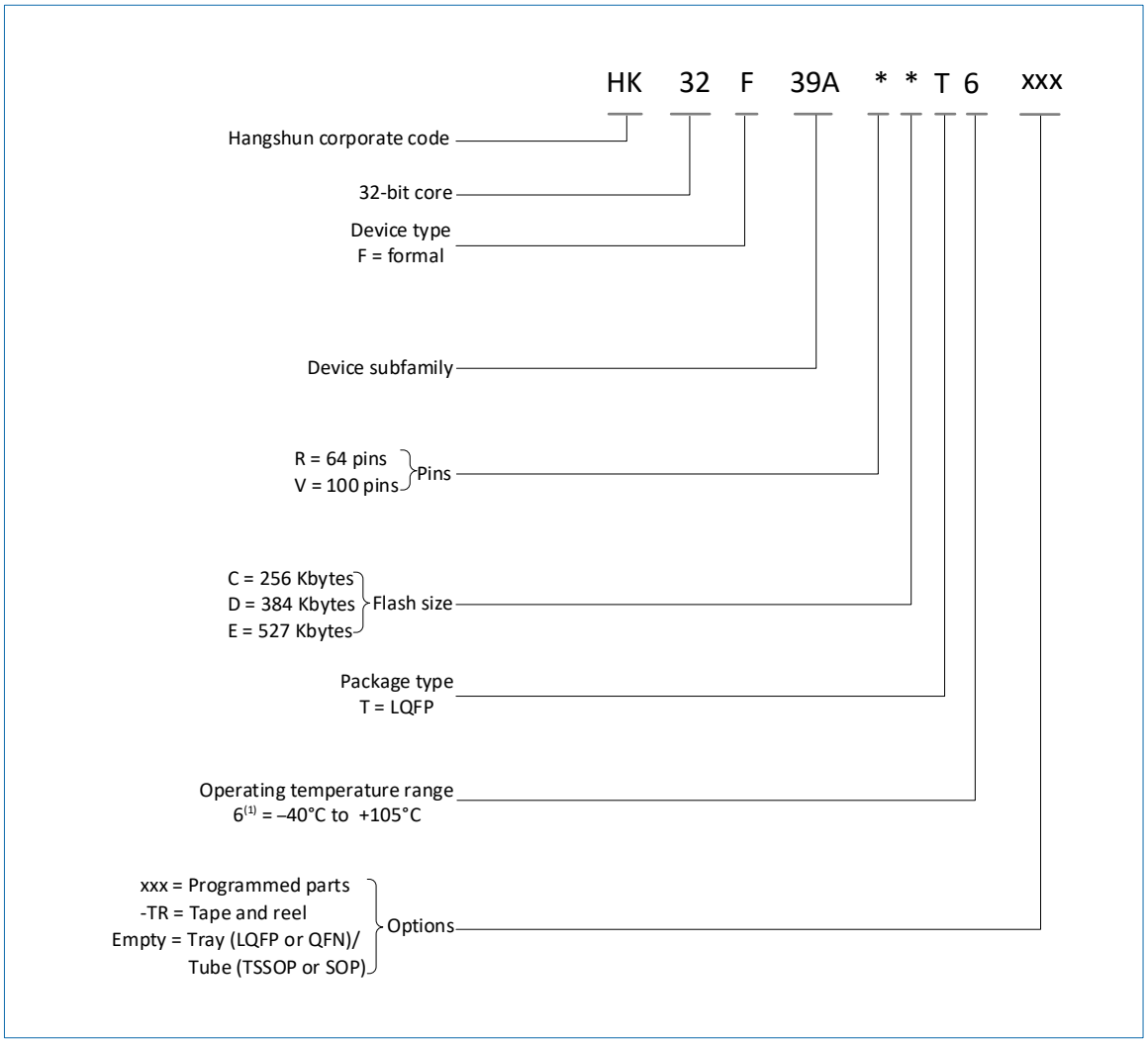


Figure 7-8 LQFP100 HK32F39AVET6 marking example

8 Ordering information

8.1 Device numbering conventions



(1). Note: The HK32F39A series was first released in earlier times, so its device numbering is based on *Hangshun Product Naming Conventions V0.9*, which is slightly different from the latest naming conventions.

8.2 Packaging information

Figure 8-1 HK32F39A packaging information

Package	Part Number	Package	Remarks
LQFP64	HK32F39ARCT6	Tray	
LQFP64	HK32F39ARCT6-TR	Tape and reel	
LQFP64	HK32F39ARDT6	Tray	
LQFP64	HK32F39ARDT6-TR	Tape and reel	
LQFP64	HK32F39ARET6	Tray	
LQFP64	HK32F39ARET6-TR	Tape and reel	
LQFP100	HK32F39AVCT6	Tray	
LQFP100	HK32F39AVCT6-TR	Tape and reel	
LQFP100	HK32F39AVDT6	Tray	
LQFP100	HK32F39AVDT6-TR	Tape and reel	
LQFP100	HK32F39AVET6	Tray	
LQFP100	HK32F39AVET6-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DCMI	Digital Camera Memory Interface
DMA	Direct Memory Access
EXTI	Extended Interrupts and Events Controller
FM	Fast Mode
GPIO	General-purpose Input/Output
HSE	High Speed External (Clock Signal)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSB	Least Significant Bit
LSE	Low-Speed External (Clock Signal)
LSI	Low Speed Internal (clock signal)
LVD	Low Voltage Detect
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PVD	Programmable Voltage Detector
PWM	Pulse Width Modulation
QSPI	Queued Serial Peripheral Interface
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
RTC	Real-time Clock
SAI	Serial Audio Interface
SDIO	Secure Digital Input and Output
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TRNG	True Random Number Generator
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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