HK32F103xCxDxE Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F103xCxDxE series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32F103xCxDxE.

Audience

This document is intended for:

- HK32F103xCxDxE developers
- HK32F103xCxDxE testers
- HK32F103xCxDxE users

Release Notes

This document is applicable to HK32F103xCxDxE series MCUs.

Revision History

Version	Date	Description
1.0.0	2019/07/23	The initial release.
1.0.1	2020/03/04	Update section "3.13 Low-power modes".
1.0.2	2020/03/09	Update section "4.2.5 Operating current".
1.0.3	2020/06/19	Update section "3.9.2 Clock tree".
1.0.4	2020/07/03	Update section "4.2.12 Flash memory characteristics".
1.0.5	2020/10/12	Update section "3.29 ADC".
1.1.0	2021/03/18	Update section "4.2.17 ADC characteristics."
1.1.4	2021/06/01	Update section "4.2.17 ADC characteristics".
1.1.5	2021/06/23	Update section "4.2.5 Operating current".
1.1.6	2021/07/15	Update section "4.2.17 DAC characteristics".
1.2	2022/10/09	1. Updated sections "2.1 Features", "2.2 Device overview", "3.1 Block diagram", and "4.2.13 Output voltage characteristics". 2. Deleted section "3.2.1.1 Flash option word". 3. Added section "3.3 Cache".
1.2.1	2022/11/02	Corrected the grammar error in the whole document
1.3	2023/10/30	1. Updated the ADC description and reliability test data in section "2.1 Features". 2. Updated the reliability test data in section "2.2 Device overview". 3. Updated Table 3-3 Software reset and low-power management reset settings. 4. Updated the I2S description in section "3.26 SPI". 5. Added sections "4.2.3 POR/PDR characteristics", "7.2 Device marking", and "8.1 Device numbering conventions". 6. Updated sections "3.5 Cache", "3.28 CAN", "4.2.14 I/O pin output characteristics", "6 Pinouts and pin descriptions", and "8.2 Packaging information".

Contents

1 Introduction

This document is the datasheet for HK32F103xCxDxE series MCUs. HK32F103xCxDxE is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun) for a wide range of purposes. This MCU family includes the HK32F103xC, HK32F103xD, and HK32F103xE sub-series. Their part numbers include:

- HK32F103xC:
  - HK32F103RCT6 (LQFP64)
  - HK32F103VCT6 (LQFP100)
- HK32F103xD:
  - HK32F103RDT6 (LQFP64)
  - HK32F103VDT6 (LQFP100)
- HK32F103xE:
  - HK32F103RET6 (LQFP64)
  - HK32F103VET6 (LQFP100)

For more details of HK32F103xCxDxE, see *HK32F103xCxDxE User Manual*.

2 Product overview

HK32F103xCxDxE adopts the ARM® Cortex®-M3 core operating at a maximum frequency of 120 MHz.

HK32F103xCxDxE embeds up to 512 Kbytes of Flash and a 64-Kbyte SRAM. Up to 1 Gbyte of external memory (NOR/PSRAM/NAND/PC Card) can be connected to HK32F103xCxDxE via the flexible static memory controller (FSMC) module. 256 Mbytes of the external memory are used to store instructions and can be used by the internal 1-Kbyte cache for instructions.

HK32F103xCxDxE embeds a cyclic redundancy check (CRC) module for data integrity verification.

HK32F103xCxDxE integrates a wide selection of communication interfaces that can meet the requirements of different application scenarios: five USARTs/UARTs, three SPIs (SPI2 and SPI3 support the I2S protocol), one SDIO, two I2Cs, one CAN 2.0A/2.0B, and one full-speed (FS) USB.

HK32F103xCxDxE has two 16-bit advanced pulse width modulation (PWM) timers (eight PWM output channels in total, six of which have complementary PWM outputs with programmable inserted dead-times), four 16-bit general-purpose PWM timers (16 PWM output channels in total), and two 16-bit basic timers.

HK32F103xCxDxE provides an independent V_{BAT} power domain. When the main V_{DD} supply is powered off, the real-time clock (RTC) can be powered by V_{BAT}. Additionally, 84 bytes of backup registers are available under V_{BAT}.

HK32F103xCxDxE integrates various analog peripherals: three 12-bit ADCs (sharing up to 16 external analog input channels: two channels for weak drive signal inputs and one channel for 5 V high-voltage signal inputs), two 12-bit DACs, a temperature sensor, a 0.8 V internal reference voltage, a programmable voltage detector (PVD), a power-on reset (POR)/power-down reset (PDR) circuitry, and a V_{BAT} resistor voltage divider (the output of the divider is connected to the ADC on chip).

HK32F103xCxDxE supports multiple power consumption modes. In the lowest-power consumption mode, the typical leakage current is less than 100 nA. HK32F103xCxDxE operates in the –40°C to +105°C temperature range, from a 2.0 V to 3.6 V power supply. It meets the environmental requirements of most applications.

The HK32F103xC, HK32F103xD, and HK32F103xE series products are delivered in 64-pin and 100-pin packages. The peripherals vary based on the package type.

With its diversified peripheral interfaces, HK32F103xCxDxE is suitable for a wide range of applications:

- Industry applications, such as programmable controllers, printers, and scanners
- Human-machine audio-video multimedia interaction
- Graph-displaying devices
- Speech recognition devices
- Monitoring devices
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- ARM® Cortex®-M3 core
    - Maximum frequency: 120 MHz

- 24-bit SysTick timer
- The CPU event signal can be input to the MCU pin to realize board-level communication with the CPU of other chips.

- Operating voltage range
  - Dual power domains:
    - Main power supply V_{DD}: 2.0 V to 3.6 V
    - Backup power supply V_{BAT}: 1.8 V to 3.6 V
  - When the main power supply V_{DD} is powered off, the RTC can be powered by $V_{BAT.}$
  - 84 bytes of backup registers are available under V_{BAT}.
- Operating temperature range: –40°C to +105°C
- V_{DD} typical operating current
  - Run mode: 19.3 mA@120 MHz@3.3 V
  - Sleep mode: 5.6 mA@120 MHz@3.3 V (Wakeup time: one clock period)
  - Stop mode
    - LDO in the low-power state: 89.4 µA@3.3 V (Wakeup time: 10 µs)
    - LDO operating at full speed: 303 µA@3.3 V
  - Standby mode: 3.3 µA@3.3 V (Wakeup time: 150 µs)
- V_{BAT} typical operating current (V_{DD} powered off)
  - V_{BAT} RTC enabled: 2.6 µA@3.3 V
  - V_{BAT} RTC disabled: 2.1 µA@3.3 V
- Memory
  - Up to 512 Kbytes of Flash
    - No wait states to access Flash when the CPU frequency is 24 MHz or lower
    - Separate read and write protection for Flash code
  - 64-Kbyte internal SRAM
  - Up to 1 Gbyte of external memory (NOR/PSRAM/NAND/PC Card) can be connected to HK32F103xCxDxE. (256 Mbytes of the external memory are used to store instructions and can be used by the internal cache for instructions.)
- Data security
  - CRC32 hardware unit
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz, typical value: 8 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): configurable to 8 MHz/28 MHz/56 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL output clock: 120 MHz (maximum value)
  - GPIO external input clock: 1 MHz to 64 MHz
- Reset
  - External pin reset
  - Power-on reset (POR)/Power-down reset (PDR)
  - Software reset

- IWDG reset and WWDG reset
- Low-power management reset

- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detecting voltage
  - Rising edge and falling edge detection configurable
- General-purpose input/output (GPIO)
  - 51 GPIO pins in the 64-pin package/80 GPIO pins in the 100-pin package
  - Each GPIO can be used as an external interrupt input
  - Built-in switchable pull-up/pull-down resistors
  - Support open-drain output
  - Support Schmitt hysteresis input
  - Configurable output drive capacity: ultra-high/high/medium/low
- Data communication interface
  - 5 × USARTs/UARTs (USART1/2/3, UART4/5)
  - 3 × SPIs (SPI2 and SPI3 support the I2S protocol)
  - 2 × I2C
  - 1 × SDIO
  - 1 × CAN 2.0A/2.0B
  - 1 x FS USB2.0
- Timer and PWM generator
  - Advanced timers: TIM1/TIM8 (six complementary PWM output channels with programmable inserted dead-times)
  - General-purpose timers: TIM2/TIM3/TIM4/TIM5
  - Basic timers: TIM6/TIM7 (support CPU interrupts, DMA requests, and DAC conversion trigger)
- On-chip analog circuitry
  - 3 × 12-bit ADCs, each up to 1 MSPS (sharing up to 16 analog input channels: two channels for weak drive signal inputs, one channel for 5 V high-voltage signal input); dual-ADC mode, sampling rate up to 2 MSPS
  - 2 × 12-bit DACs
  - 1 × temperature sensor
  - 1 × 0.8 V internal reference voltage
  - 1 × V_{BAT} resistor voltage divider (the output of the divider is connected to the ADC on chip for the monitoring of V_{BAT})
- DMA controller
  - Two independent DMA controllers: DMA1 and DMA2
  - DMA1 provides seven channels
  - DMA2 provides five channels
  - Can be triggered by the timer, ADC, SPI, I2C, USART, and UART
- CPU debug and trace port
  - Dual-wire SW-DP
  - Five-wire JTAG
  - ARM® CoreSight™ debug components (DWT, FPB, ITM, TPIU)

- Single-wire asynchronous trace data output interface (TRACESWO)
- Four-wire synchronous trace data output interface (TRACEDO[3:0], TRACECKO)
- Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)

- Clock-calendar function provided by RTC counter in cooperation with software
- UID
  - Each HK32F103xCxDxE MCU provides a 96-bit unique ID (UID).
- Reliability
  - Passed HBM2000V/CDM500V/MM200V/LU200mA level tests.

2.2 Device overview

Table 2-1 HK32F103xCxDxE series features

Feature	HK32F103RCT6	HK32F103RDT6	HK32F103RET6	HK32F103VCT6	HK32F103VDT6	HK32F103VET6
Package	LQFP64			LQFP100		
GPIO	51			80		
CPU frequency	120 MHz					
Flash (Kbyte)	256	384	512	256	384	512
Cache (Kbyte)	1					
SRAM (Kbyte)	64					
DMA	2 (DMA1: 7 channels, DMA2: 5 channels)					
CRC32	1					
FSMC	- (1)	-	-	1	1	1
SDIO	1					
I2C	2					
USB (full-speed)	1					
CAN	1					
USART/UART	5 (USART1 – USART3, UART4, UART5)					
SPI/I2S	3/2 (SPI1, SPI2/I2S2, SPI3/I2S3)					
Advanced timer	2					
General-purpose timer	4					
Basic timer	2					
IWDG	1					
WWDG	1					
96-bit UID	Supported					
Programmable voltage detector (PVD)	Supported					
ADC (External channels)	ADC1 (16) + ADC2 (16) + ADC3 (8)					
DAC	2					
Temperature sensor	1					
Operating voltage	V_{DD}: 2.0 V to 3.6 V V_{BAT}: 1.8 V to 3.6 V					
Operating temperature	–40°C to +105°C					

(1). The hyphen (-) in the table indicates that the feature is not supported.

3 Function description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor that provides an MCU platform featuring low power consumption and high performance. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M3 core, the HK32F103xCxDxE family is compatible with ARM tools and software.

The block diagram of HK32F103VET6 is as follows:

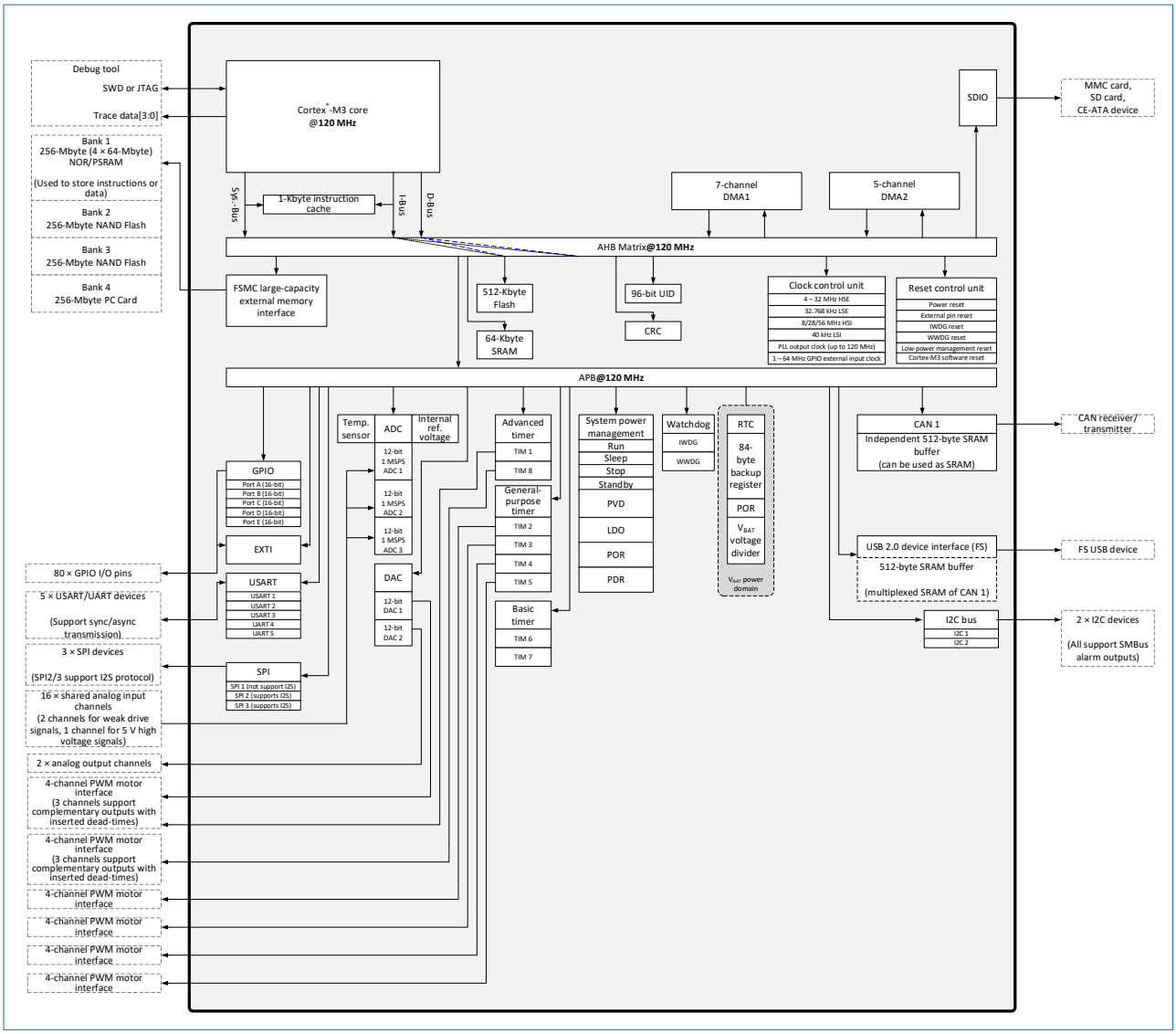

Figure 3-1 HK32F103VET6 block diagram

3.2 Memory mapping

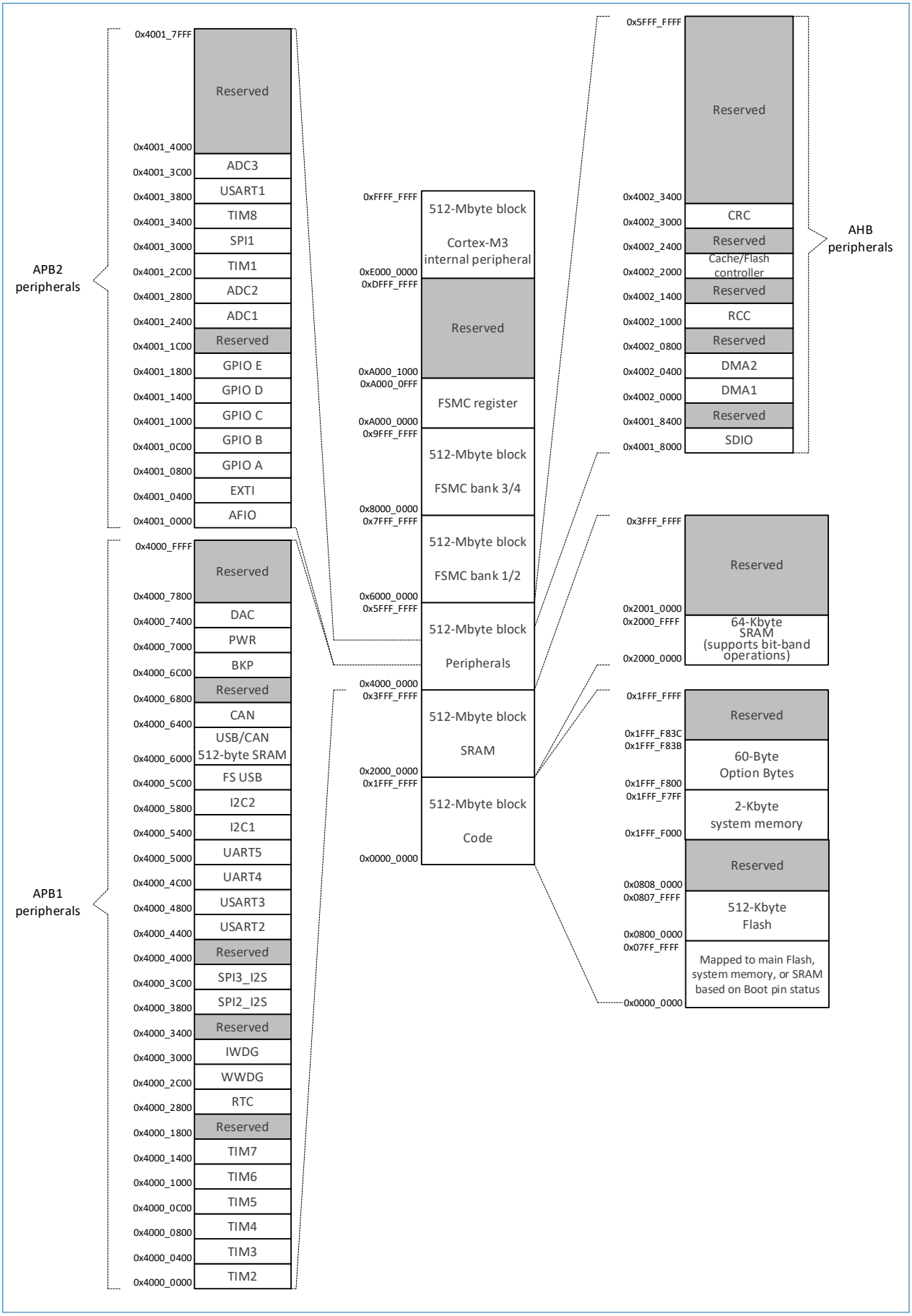

Figure 3-2 HK32F103xCxDxE memory mapping

3.3 Flash

HK32F103xCxDxE integrates a Flash memory of up to 512 Kbytes to store programs and data.

- Flash data width: 128 bits, 2 Kbytes per page
- Flash access: write in half words (16 bits), words (32 bits), two words (64 bits), or four words (128 bits); read in 128 bits
- Supports Flash read/write protection.
- Supports pre-fetch instruction buffer and data buffer.
- Integrates a module for automatically encrypting and decrypting Flash instructions to protect the intellectual property (IP) of on-chip software.

3.4 SRAM

HK32F103xCxDxE integrates a 64-Kbyte SRAM. The SRAM can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.5 Cache

The device integrates 1 Kbyte of high-speed cache for storing instructions.

- 8-way set associative
- The least recently used (LRU) strategy is adopted.
- The embedded counter counts the hit rate of instructions stored in the cache.
- The cache control register can be configured to cache instructions of specific types. The data of one of the following instruction fetch operations can be cached at a time:
  - I-Bus instruction fetch from internal Flash
  - SYS-Bus instruction fetch from external Flash via FSMC

3.6 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32F103xCxDxE integrates a CRC calculation unit to reduce the application processing burden and accelerate processing.

3.7 FSMC

- External SRAM, NOR Flash memory, PSRAM, and PC Card can be connected to HK32F103xCxDxE via the flexible static memory controller (FSMC)
- Provides two NAND Flash interfaces and hardware ECC for up to 8 Kbytes of data.
- Provides a 16-bit PC Card interface.
- Supports burst access to synchronous devices (NOR Flash and PSRAM).
- 8-bit or 16-bit data bus.
- Independent chip select (CS) and configuration register for each external memory
- Consecutive 8-bit or 16-bit accesses (converted from 32-bit wide AHB transactions) to 8-bit or 16-bit external devices
- Provides a FIFO of two words so that the AHB can be released for other operations when FSMC performs writes to external slow memories.
- Wait control for asynchronous external memories
- Write encryption and read decryption for 16-bit external memories

- Supports Intel 8080 mode and Motorola 6800 mode, and can flexibly connect to various LCD controllers.
- Programmable timing control for different devices, including:
  - Programmable wait states (up to 15)
  - Programmable bus processing cycles (up to 15)
  - Programmable read/write enable delays (up to 15)
  - Separate timings and protocols for read and write operations to support as many types of memories and timings as possible

3.8 NVIC

HK32F103xCxDxE embeds a nested vectored interrupt controller (NVIC) to manage interrupts flexibly with the lowest interrupt latency.

- The NVIC closely coupled with the core interface ensures low latencies in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

An HK32F103xCxDxE MCU has 60 external interrupts.

3.9 EXTI

HK32F103xCxDxE embeds 22 extended interrupt/event controller (EXTI) lines. EXTI0 to EXTI15 are connected to I/Os. The trigger event of each EXTI line can be configured independently. The trigger event can be a rising edge, a falling edge, or both.

3.10 Resets

HK32F103xCxDxE supports the system reset, power reset, and backup domain reset.

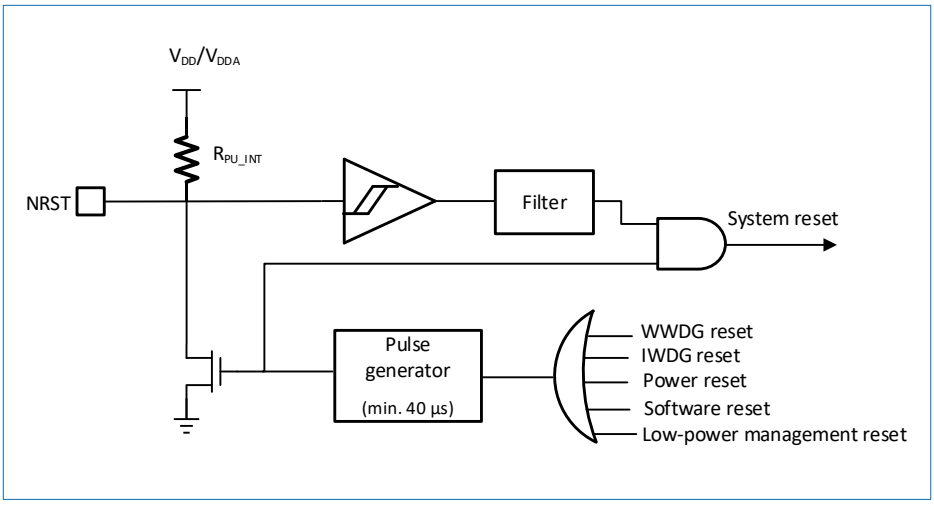

Figure 3-3 Reset circuitry

3.10.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain. You can identify a reset source by checking reset status flags in the RCC_CSR register.

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW Reset)
- Low-power management reset

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004.

The internal reset signal is output on the NRST pin. The pulse generator guarantees a pulse duration of at least 40 µs for each internal or external reset source. When the NRST pin is pulled low and an external reset is generated, a reset pulse is generated.

Table 3-1 Software reset and low-power management reset

Reset Type	Configuration
Software reset	The SYSRESETREQ bit in Cortex®-M3 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
Low-power management reset	Generating a low-power management reset when entering the Standby mode: Set the nRST_STDBY bit in the option byte to 0 to generate the low-power management reset. This way, even if the system is in the process of entering the Standby mode, it will be reset instead of entering the Standby mode.
	Generating a low-power management reset when entering the Stop mode: Set the nRST_STOP bit in the option byte to 0 to generate the low-power management reset. This way, even if the system is in the process of entering the Stop mode, it will be reset instead of entering the Stop mode.

3.10.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Exit from Standby mode

The power reset resets all registers, except for the registers in the backup domain.

HK32F103xCxDxE embeds the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply is over the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the MCU remains in the reset state and no external reset circuits are required.

3.10.3 Backup domain reset

The backup domain has two dedicated resets that only affect the backup domain. A backup domain reset is generated when any of the following events occurs:

- Software reset: Set the BDRST bit in the backup domain control register RCC_BDCR.
- V_{DD} and (or) V_{BAT} are powered on again after being powered off.

3.11 Clocks

A system clock is selected when the MCU starts. The 8 MHz HSI is selected as the system clock by default after a reset. Later, a 4 MHz – 32 MHz HSE can be selected. If the HSE fails, it will be isolated and a corresponding interrupt will be generated. More clock frequencies can be produced by using PLL.

HK32F103xCxDxE also provides LSI, LSE, and GPIO input as clock sources for the low-power and low-cost design scheme.

HK32F103xCxDxE integrates a clock security system (CSS) circuit. The threshold for the detection of HSE frequency is adjustable.

3.11.1 Clock sources

Table 3-2 Clock sources

Clock	Description
HSI	Output frequency: 56 MHz. Accuracy: full temperature range ± 2%
HSE	Frequency: 4 MHz to 32 MHz Supports the input of an external clock (up to 64 MHz) from the OSC_IN pin
PLL clock	Input frequency: 1 MHz to 80 MHz Output frequency: 16 MHz to 120 MHz
LSI	Frequency: 30 kHz to 60 kHz (typical value: 40 kHz)
LSE	Frequency: 32.768 kHz Supports the input of a 32.768 kHz external clock from the OSC32_IN pin
GPIO input clock	Up to 64 MHz, input from PA1, PB1, PC7, PB7

3.11.2 Clock tree

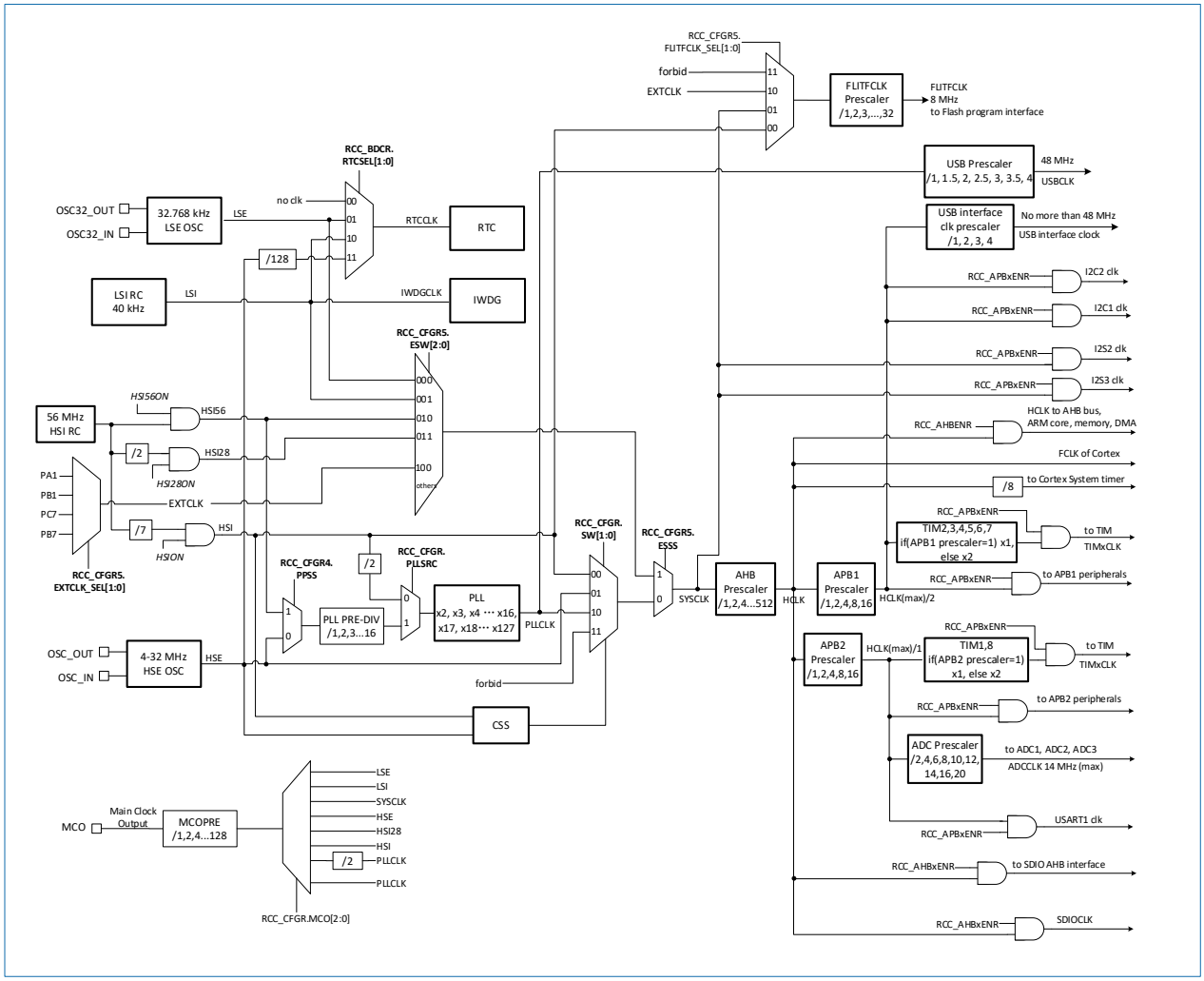

Figure 3-4 Clock tree

Note:

- PLL input clock: chosen from HSI8/2, HSI56/PREDIV, and HSE/PREDIV.
- SYSCLK: chosen from HSI8, HSI28, HSI56, HSE, PLL, LSI, LSE, and GPIO input clock. HSI8 is the default clock.
- FLITFCLK: chosen from HSI8, GPIO input clock, and SYSCLK.

3.12 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from main Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the USART1 interface.

3.13 Power supply scheme

- V_{DD} = 2.0 V to 3.6 V. V_{DD} supplies power to I/O pins and internal low dropout regulators (LDOs).
- V_{DDA} = 2.0 V to 3.6 V. V_{DDA} supplies power to the analog circuitry, including the ADC and temperature sensor.
- V_{BAT} = 1.8 V to 3.6 V. When V_{DD} is powered off, V_{BAT} supplies power to the RTC, external 32.768 kHz oscillator, and backup registers.

3.14 PVD

HK32F103xCxDxE integrates a programmable voltage detector (PVD). The PVD monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated. The interrupt program may send a warning message or set the MCU to the safe state. The PVD is enabled by setting the register.

3.15 Low-power modes

HK32F103xCxDxE supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the phase-locked loop (PLL), HSE oscillator, and HSI oscillator are disabled. MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any of the 16 external I/O pins, a PVD output, or an RTC alarm.

- Standby mode

  In Standby mode, MCUs achieve the lowest power consumption. The internal LDOs are off, so the entire 1.2 V domain is powered off. The PLL, HSI oscillator, and HSE oscillator are disabled. The SRAM content and register content are lost, except for registers in the backup domain. The Standby circuitry works as normal. MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: For more information about the power consumption of different modes, see Table 4-8.

The following table describes the conditions of entering and exiting low-power modes:

Table 3-3 Entry into and exit from low-power modes

Operating Mode	Entry	Exit	Core Domain Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
Sleep	1. Set PWR_CR:LPDS = 0 and PWR_CR:PDDS = 0. 2. The software executes WFI/WFE instructions.	Any interrupt request (IRQ), including SysTick.	The CPU clock is off. No impact on other clocks or the ADC clock.	On	On

Operating Mode	Entry	Exit	Core Domain Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
Stop	1. Set PWR_CR:PDDS = 0. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions.	Any EXTI line. The MCU can be pre-woken up by periodic ADC sampling. The real wakeup occurs when the conditions are met.	All clocks stop.	HSI and HSE oscillators are off.	On or in low-power mode (configured in PWR_CR)
Standby	1. Set PWR_CR:LPDS = 0 and PWR_CR:PDDS = 1. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions. 4. Clear the WUF bit in the Power control/status register PWR_CSR.	Three polarity-configurable external pins (WKUPx), the RTC alarm, and the IWDG reset.	All clocks stop.	HSI and HSE oscillators are off.	Off

3.16 DMA

The flexible general-purpose direct memory access (DMA1 with seven channels and DMA2 with five channels) controllers manage the data transfer from memories to memories, from peripherals to memories, and from memories to peripherals. The two DMAs support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by software. The length, source, and destination of data to be transferred can be independently set by using software. The DMAs can be used with the main peripherals, such as SPI, I2C, USART, TIMx, SDIO, and ADC.

3.17 RTC and BKP

The power supply to RTC and backup registers is controlled by a switch. When V_{DD} is enabled, V_{DD} supplies power to RTC and backup registers. Otherwise, V_{BAT} supplies power to RTC and backup registers.

3.17.1 RTC

The real-time clock (RTC) has a set of continuously running counters and can provide the clock calendar function via software. In addition, the RTC provides alarm interrupt and periodic interrupt functions.

The 32.768 kHz external oscillator or an internal low-power RC oscillator can drive RTC. The typical frequency of the internal low-power RC oscillator is 40 kHz. An external 512 Hz signal is used for the compensation of natural quartz deviation. The RTC has a 32-bit programmable counter for long-term measurement in conjunction with the compare register. The RTC has a 20-bit prescaler which is used to generate the time base clock. When the RTC is clocked by the 32.768 kHz crystal oscillator (LSE), a one-second time base is generated.

3.17.2 BKP

Backup registers (BKP) are used to store user application data. The system reset and power reset do not reset backup registers. Backup registers are not reset upon wakeup from Standby mode. HK32F103xCxDxE has 42 backup registers (BKP_DR1 to BKP_DR42, 84 bytes in total) in the backup domain.

3.18 IWDG

The independent watchdog (IWDG) is based on a 12-bit down counter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. IWDG can be configured as a software

or hardware watchdog through the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use the window watchdog mode of IWDG. The reset initial value of the IWDG can be set through option bytes.

3.19 WWDG

The window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used to reset the system when a problem occurs. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.20 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard down counter with the following features:

- 24-bit down counter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.21 Basic timer

HK32F103xCxDxE integrates basic timers TIM6 and TIM7. A basic timer can be used as a 16-bit generic time base timer or used to generate a DAC trigger signal.

3.22 General-purpose timer

Every general-purpose timer (TIM2/TIM3/TIM4/TIM5) provides a 16-bit auto-reload up/down counter, a 16-bit prescaler, and four independent channels. Every channel can be used for input capture, output compare, PWM output, and one-pulse mode output. In the LQFP100 package, up to 16 channels are available for input capture, output compare, and PWM output. The general-purpose timers can work with the advanced timer through the Timer Link feature for synchronization and event chaining. In debug mode, the counter can be frozen.

The general-purpose timer can be used to trigger DAC.

Every general-purpose timer can generate PWM outputs and has an independent DMA request mechanism.

The four input channels of TIM2/TIM3/TIM4/TIM5 support triggering on the rising edge, falling edge, or both.

3.23 Advanced timer

HK32F103xCxDxE integrates the advanced timers TIM1 and TIM8. Each timer can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1/TIM8 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). In debug mode, the counter can be frozen. Many functions of the advanced timers are the same as those of general-purpose timers, and the two types of timers have the same structure. Therefore, the advanced timers can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

The advanced timers provide the DAC trigger.

TIM1 and TIM8 have the following functions:

- CCER[15]: CC4NP bit in the TIM_CCER register for inputting triggers on both rising and falling edges
- CR1[15]: ETR_CLR_SEL bit in the TIM_CR1 register for selecting an external pin to clear PWM outputs.
- CR1[14]: BRK_SEL bit in the TIM_CR1 register for selecting an external pin to output PWM breaks.
- The four input channels of TIM1/TIM8 support triggering on the rising edge, falling edge, or both.

3.24 I2C bus

HK32F103xCxDxE embeds two I2C bus interfaces. The I2C bus interfaces can work as a master or slave and support the standard and fast modes. They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interfaces have embedded hardware CRC generation/verification. They can be operated by using the DMA controller and support SMBus V2.0/PMBus.

3.25 USART

HK32F103xCxDxE embeds three universal synchronous/asynchronous receivers/transmitters (USART1/2/3) and two universal asynchronous receivers/transmitters (UART4/5). These interfaces support asynchronous communication, IrDA SIR ENDEC, multi-processor communication, single-wire half-duplex communication, and LIN Master/Slave capability.

The USART1 interface communicates at a speed of up to 4.5 Mbit/s. The other USART and UART interfaces communicate at a speed of up to 2.25 Mbit/s.

Table 3-4 USART/UART features

Feature	USART1/2/3	UART4	UART5
Hardware flow control	Supported	Not supported	Not supported
DMA continuous transmission	Supported	Supported	Not supported
Multiprocessor communication	Supported	Supported	Supported
Synchronous mode	Supported	Not supported	Not supported
Smart Card mode	Supported	Not supported	Not supported
Single-wire half-duplex communication	Supported	Supported	Supported
IrDA SIR ENDEC	Supported	Supported	Supported
LIN Master/Slave mode	Supported	Supported	Supported

3.26 SPI

HK32F103xCxDxE has three serial peripheral interfaces (SPIs). In master or slave mode, the full-duplex and half-duplex communication speed is up to 18 Mbit/s. The 3-bit prescaler provides eight master mode frequencies. Each frame can be configured to 8-bit or 16-bit. The hardware CRC generation/verification supports the basic SD card and MMC mode.

All SPI interfaces can be operated by using the DMA controller.

Two SPI interfaces (SPI2/3) can operate in I2S mode. The two standard I2S interfaces can operate in master or slave mode and can be configured to operate with 16-bit, 24-bit, or 32-bit resolution. These interfaces can also be configured as input or output channels. The supported audio sampling frequency is from 8 kHz to 192 kHz. When an I2S interface is configured as a master, the master clock at 256 times the sampling frequency can be output to the external DAC or CODEC.

Table 3-5 SPI features

SPI Feature	SPI1	SPI2/3
Hardware CRC calculation	Supported	Supported
RX/TX buffer	Supported	Supported
I2S mode	Not supported	Supported

3.27 SDIO

An SD/SDIO/MMC host interface supports Multi-Media-Card (MMC) System Specification Version 4.2 in three different data bus modes:

- 1-bit (default)
- 4-bit
- 8-bit: In this mode, the interface allows data transfer at up to 48 MHz, and the interface is compliant with SD Memory Card Specification Version 2.0.

SD Memory Card Specification Version 2.0 supports two data bus modes: 1-bit (default) and 4-bit.

The MCU of the current version supports only one SD/SDIO/MMC 4.2 card each time but multiple cards of MMC 4.1 or earlier versions each time. In addition to SD/SDIO/MMC, this interface is compatible with the CE-ATA digital protocol version 1.1.

3.28 CAN

HK32F103xCxDxE has an independent controller area network (CAN) interface. The CAN interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN interface has three transmit mailboxes and two three-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.29 USB

HK32F103xCxDxE embeds a USB controller that complies with the full-speed USB device standard. The USB interface endpoint settings can be configured by using the software. It provides suspend/resume support. The dedicated 48 MHz clock for USB is generated by the internal main PLL.

3.30 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.31 ADC

HK32F103xCxDxE embeds three 12-bit analog-to-digital converters (ADCs) that share up to 16 external channels. The ADCs perform the conversions in single or scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface include:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be operated by using the DMA controller. The analog watchdog feature enables precise monitoring of the converted voltage of one, some, or all selected channels. When the monitored voltage exceeds the preset threshold, an interrupt is generated. The events generated by the general-purpose timers and advanced timers can be internally connected to the ADC start trigger events and injection trigger events respectively. The application program then synchronizes the A/D conversion with timers.

In Stop mode, RTC counts and sends signals to the ADC. The ADC samples the signals and wakes up the ADC clock. Then the ADC clock triggers ADC conversions and generates AWD events according to ADC conversion results. Then AWD events are sent to an EXTI line to wake up the system.

3.32 DAC

HK32F103xCxDxE embeds two 12-bit buffered DAC channels. They are used to convert 2-channel digital signals to 2-channel analog voltage signals and output the signals.

The two DAC interfaces support the following features:

- Each DAC has an output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Update synchronization
- Noise-wave generation
- Triangular-wave generation
- Independent or simultaneous conversions based on dual-DAC channels
- DMA can be used for each channel
- Externally-triggered conversion
- Input voltage reference V_{REF+}

HK32F103xCxDxE has eight DAC trigger inputs. The update outputs of timers can trigger the DAC channels and can be connected to different DMA channels.

3.33 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.34 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32F103xCxDxE MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process that has a security mechanism.

3.35 Debug and trace port

HK32F103xCxDxE embeds the ARM SWJ-DP which is a combined JTAG-DP and SW-DP that enables you to connect either a serial wire debug (SWD) or JTAG probe to a target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively. A special signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

The ARM® Embedded Trace Macrocell (ETM) outputs compressed data streams from HK32F103xCxDxE to an external trace port analyzer (TPA) device at a high rate by using a few ETM pins. This way, the instruction and data flow inside the CPU core is explicitly displayed to developers. The TPA can be connected to the debugging host by using USB or through other high-speed channels. The real-time instruction and data flows can be recorded by the debugging software installed on the debugging host and displayed in the required format. The TPA hardware obtained from the development tool vendors is compatible with third-party debugging software.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}–V_{SS}	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	3.63	V
V_{IN}	Input voltage on pins	V_{SS} – 0.3	V_{DD}	
$\|\Delta V_{DDx}\|$	Variation between different power pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Variation between different ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of the positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to +150	°C
T_J	Maximum junction temperature	125	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	60	
f_{PCLK2}	Internal APB2 clock frequency	0	120	
V_{DD}	Standard operating voltage	2	3.6	V
V_{DDA}(1)	Analog operating voltage	2	3.6	V
V_{BAT}	Backup domain operating voltage	1.8	3.6	V

Symbol	Description	Min	Max	Unit
T	Operating temperature	–40	105	℃

(1). It is recommended that you use the same power supply for V_{DD} and V_{DDA}.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0] = 000	2.183	2.188	2.196	V
		PLS[2:0] = 001	2.286	2.289	2.298	
		PLS[2:0] = 010	2.393	2.399	2.407	
		PLS[2:0] = 011	2.502	2.508	2.518	
		PLS[2:0] = 100	2.621	2.629	2.639	
		PLS[2:0] = 101	2.726	2.733	2.745	
		PLS[2:0] = 110	2.839	2.846	2.855	
		PLS[2:0] = 111	2.958	2.969	2.979	
	Programmable voltage detector level selection (falling edge)	PLS[2:0] = 000	2.116	2.119	2.125	
		PLS[2:0] = 001	2.208	2.211	2.220	
		PLS[2:0] = 010	2.305	2.310	2.320	
		PLS[2:0] = 011	2.399	2.406	2.416	
		PLS[2:0] = 100	2.506	2.512	2.521	
		PLS[2:0] = 101	2.596	2.602	2.613	
		PLS[2:0] = 110	2.693	2.701	2.710	
		PLS[2:0] = 111	2.798	2.805	2.817	

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge(2)	1.8	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset duration	-	1.50	2.50	4.50	ms

(1). PDR is based on the monitoring of V_{DD} and V_{DDA}. POR is based on the monitoring of only V_{DD}.

(2). The actual performance value is guaranteed to be smaller than the minimum $V_{POR/PDR}$ value.

(3). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to +105°C	0.74	0.8	0.811	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition	V_{DD} = 3.3 V				Unit
		–40°C	25°C	85°C	105°C	
Run mode	CPU operating at 120 MHz; Cache **enabled** APB clock **enabled**, using the 120 MHz clock; Four wait states to access Flash.	12.18	20.95	22.31	23.44	mA
	CPU operating at 120 MHz; Cache **disabled**; APB clock **enabled**, using the 120 MHz clock; Four wait states to access Flash.	11.2	19.34	20.71	21.82	mA
	CPU operating at 120 MHz; Cache **enabled** APB clock **disabled**, using the 120 MHz clock; Four wait states to access Flash.	6.71	11.50	12.74	13.81	mA

Mode	Condition	V_{DD} = 3.3 V				Unit
		–40°C	25°C	85°C	105°C	
	CPU operating at 120 MHz; Cache **disabled**; APB clock **disabled**, using the 120 MHz clock; Four wait states to access Flash.	6.1	10.44	11.66	12.75	mA
	CPU operating at 8 MHz; Cache **enabled** APB clock **enabled**, using the 8 MHz HSE; Zero wait states to access Flash.	1.83	1.98	3.08	4.1	mA
	CPU operating at 8 MHz; Cache **disabled**; APB clock **enabled**, using the 8 MHz HSE; Zero wait states to access Flash.	3.65	3.91	5.06	6.12	mA
	CPU operating at 8 MHz; Cache **enabled** APB clock **disabled**, using the 8 MHz HSE; Zero wait states to access Flash.	1.19	1.36	2.39	3.41	mA
	CPU operating at 8 MHz; Cache **disabled**; APB clock **disabled**, using the 8 MHz HSE; Zero wait states to access Flash.	1.15	1.25	2.32	3.36	mA
	CPU operating at 40 kHz; APB clock **enabled**, using the 40 kHz LSI;	0.23	0.31	1.34	2.33	mA
	CPU operating at 32.768 kHz; APB clock **enabled**, using the 32.768 kHz LSE;	0.23	0.3	1.35	2.32	mA
Sleep mode	CPU paused; APB clock **enabled**, using the 120 MHz clock;	8.52	14.63	15.92	17.01	mA
	CPU paused; APB clock **disabled**, using the 120 MHz clock;	3.3	5.65	6.82	7.85	mA
	CPU paused; APB clock **enabled**, using the 8 MHz HSI;	1.56	1.69	2.95	3.72	mA
	CPU paused; APB clock **disabled**, using the 8 MHz HSI;	0.88	1.01	2.85	3.04	mA
Stop mode	CPU paused; LDO **operating at full speed**; HSE/HSI/LSE disabled; IWDG disabled.	202.67	303	1322	2179	µA
	CPU paused; LDO in the **low-power state**; HSE/HSI/LSE disabled; IWDG disabled.	18.38	89.47	729	1374	µA
Standby mode	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off. Only the Standby circuitry works as normal; LSI oscillator **enabled**; IWDG **enabled**.	2.98	3.87	16.74	30.29	µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off. Only the Standby circuitry works as normal; LSI oscillator **disabled**; IWDG **disabled**.	2.96	3.87	16.68	30.22	µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off. Only the Standby circuitry works as normal; HSE, HSI, LSE, LSI **disabled**	2.35	3.36	16.16	29.72	µA

4.2.6 HSE clock characteristics

HK32F103xCxDxE integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

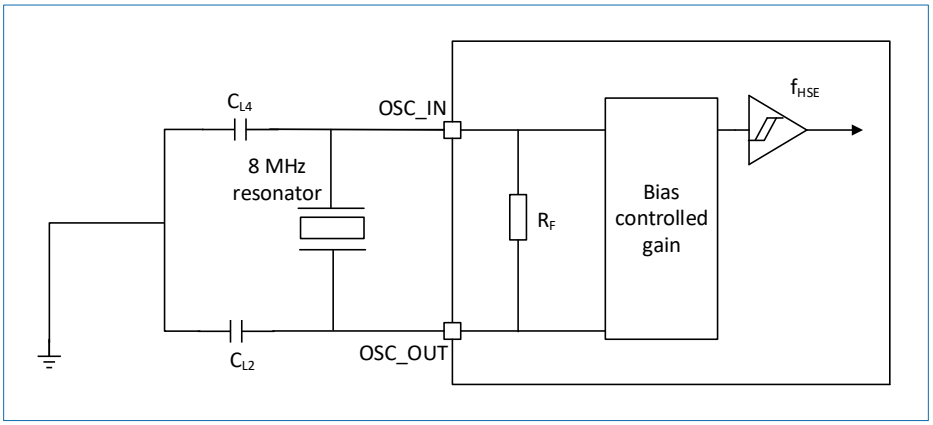

Figure 4-1 Recommended startup circuit outside the chip

Alternatively, an HSE signal can be directly input from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-9 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	Frequency	-	1	8	25	MHz
V_{HSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$T_{w(HSE)}$	Effective high/low level duration		5	-	-	ns
$T_{r(HSE)}$ $T_{f(HSE)}$	Rise/Fall time		-	-	20	
$Cin_{(HSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.7 LSE clock characteristics

HK32F103xCxDxE integrates an LSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

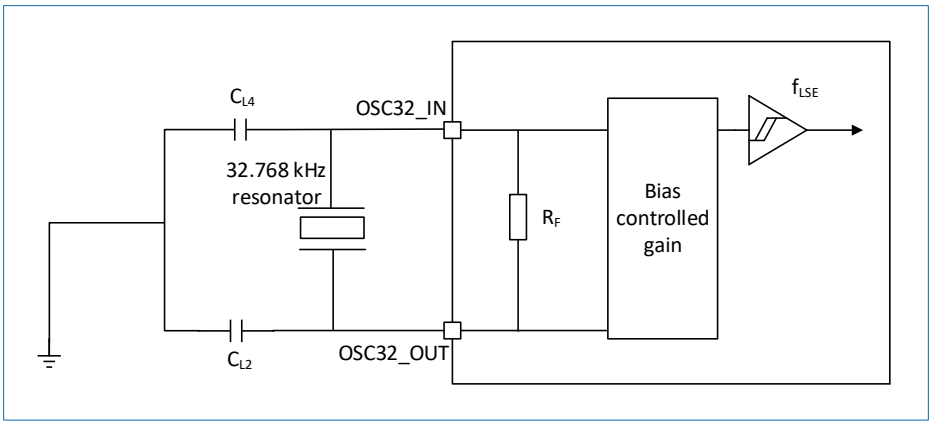

Figure 4-2 Recommended startup circuit outside the chip

Alternatively, an LSE signal can be directly input from the OSC32_IN pin. The following table lists the requirements for this clock signal:

Table 4-10 Characteristics of the input LSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{LSE_ext}	Frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$Tw_{(LSE)}$	Effective high/low level duration		450	-	-	ns
$Tr_{(LSE)}/Tf_{(LSE)}$	Rise/Fall time		-	-	50	
$Cin_{(LSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.8 HSI clock characteristics

Table 4-11 Characteristics of the HSI clock

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI} RC 56	RC oscillator	-		-	56	-	MHz
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Oscillator accuracy	Factory trimmed accuracy (ambient temperature)		–1	-	1	%
		Factory calibrated	TA= –40°C to 105°C	–2	-	2.5	%
			TA= –40°C to 85°C	–1.5	-	2.2	%
			TA = 0°C to 70°C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$Tsu_{(HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$I_{DD(HSI)}$	Oscillator power consumption	-		-	80	100	µA

4.2.9 LSI clock characteristics

Table 4-12 Characteristics of the LSI clock

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$	Oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$	Oscillator power consumption	-	0.65	1.2	µA

4.2.10 PLL characteristics

Table 4-13 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	1	8.0	80	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	120	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.11 GPIO input clock

Clocks can be input from PA1, PB1, PC7, and PB7. The input clocks must meet the following requirements:

Table 4-14 GPIO input clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{ext}	Input clock frequency	1	8.0	64	MHz
	Input clock duty cycle	40	-	60	%
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.12 Flash memory characteristics

Table 4-15 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-time programming time(1)	6	-	7.5	µs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
IDD_{PROG}	One-time programming current(1)	-	-	5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Read current@24 MHz	-	2	3	mA
	Read current@1 MHz	-	0.25	0.4	mA
N_{END}	Erasure endurance	100,000	-	-	Cycles
t_{RET}	Data retention	20	-	-	Years

(1) The one-time programming is in 16, 32, 64, or 128 bits, but the programming time and current values are not changed.

4.2.13 I/O pin input characteristics

Table 4-16 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	1.6	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.5	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	450	-	mV
I_{lkg}	Input leakage current	V_{IN} = 3.3 V	-	-	3	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.14 I/O pin output characteristics

Table 4-17 I/O pin output direct current characteristics

Mode[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	V_{OL}	Output low level voltage	V_{DD} = 3.3 V	-	0.4	V
	V_{OH}	Output high level voltage		2.4	-	V
01	V_{OL}	Output low level voltage	V_{DD} = 3.3 V	-	0.4	V
	V_{OH}	Output high level voltage		2.4	-	V
11	V_{OL}	Output low level voltage	V_{DD} = 3.3 V	-	0.4	V
	V_{OH}	Output high level voltage		2.4	-	V

Table 4-18 I/O pin output alternating current characteristics

Mode[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2.0 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2.0 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	5	ns
	$tr_{(IO)out}$	Output low to high level rise time		-	5	ns

4.2.15 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-19 NRST pin input characteristics

Symbol	Parameter	Min	Max	Unit
V_{IL}	NRST input low level voltage	-	0.8	V
V_{IH}	NRST input high level voltage	2	-	V
V_{hys}	Schmitt trigger voltage hysteresis	-	200	mV
R_{pull}	Internal weak pull-up resistor	-	50	kΩ
T_{Noise}	Low level ignored duration	-	100	ns

4.2.16 TIM characteristics

Table 4-20 TIM characteristics

Symbol	Condition	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIMxCLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}/2^{(1)}$	MHz
RES_{TIM}	Timer resolution	-	16	bit
$T_{counter}$	16-bit counter clock period when an internal clock is selected	1	65536	$T_{TIMxCLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536 × 65536	$T_{TIMxCLK}$

(1). $F_{TIMxCLK}$ == 120 or 60 MHz

4.2.17 ADC characteristics

Table 4-21 ADC characteristics

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} grounded)	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sample switch resistance	-	-	-	1	kΩ
C_{ADC}	Sample and hold capacitance	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
			-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
			14 to 252 (sampling time ts + 12.5 for successive approximation)			$1/f_{ADC}$
ADC bit width	12-bit (8 bits valid)	-	-			-

4.2.18 DAC characteristics

Table 4-22 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	2.0	3.3	3.6	V
V_{REF+}	Reference supply voltage	2.0	3.3	3.6	V
V_{SSA}	Ground	0	0	0	V
R_{LOAD}	Resistive load with buffer enabled	5		-	kΩ
R_O	Impedance output with buffer disabled	-	15	-	kΩ
C_{LOAD}	Capacitive load	-	-	-	pF
DAC_OUT min	Lower DAC_OUT voltage with buffer enabled	0.1	-	-	V
DAC_OUT max	Higher DAC_OUT voltage with buffer enabled	-	-	V_{DD}	V
DAC_OUT min	Lower DAC_OUT voltage with buffer disabled	0	-	-	mV
DAC_OUT max	Higher DAC_OUT voltage with buffer disabled	-	-	V_{REF}	V
$I_{DDVREF+}$	DAC direct current consumption in quiescent mode (standby mode)	108	135	162	µA
I_{DDA}	DAC direct current consumption in quiescent mode	-	-	429	µA
DNL	Differential non linearity (difference between two consecutive code – 1LSB)	-	-	±1	LSB
INL	Integral non linearity (difference between measured value at	-	-	±4	LSB

Symbol	Parameter	Min	Typ	Max	Unit
	code i and the value at code i on a line drawn between code 0 and last code 1023)				
Offset	Offset error (difference between the measured value at code 0x800 and the ideal value V_{REF+}/2)	-	-	±10	mV
		-	-	±12	LSB
Gain error	Gain error	-	-	±0.5	%
$t_{SETTLING}$	Settling time (full scale: when DAC_OUT reaches the final value ±1LSB, the transition for a 10-bit input code from the minimum to the maximum)	-	3	4	μs
Update rate	Maximum frequency of a correct DAC_OUT when the input code variation is small (from i to i+1LSB)	-	-	1	MS/s
t_{WAKEUP}	Wakeup time from the off state (setting the ENx bit in the DAC control register)	-	6.5	10	μs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	67	40	dB

4.2.19 Temperature sensor characteristics

Table 4-23 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Avg_Slope	Average slope	-	2.9	3	3.1	mV/°C

5 Typical circuitry

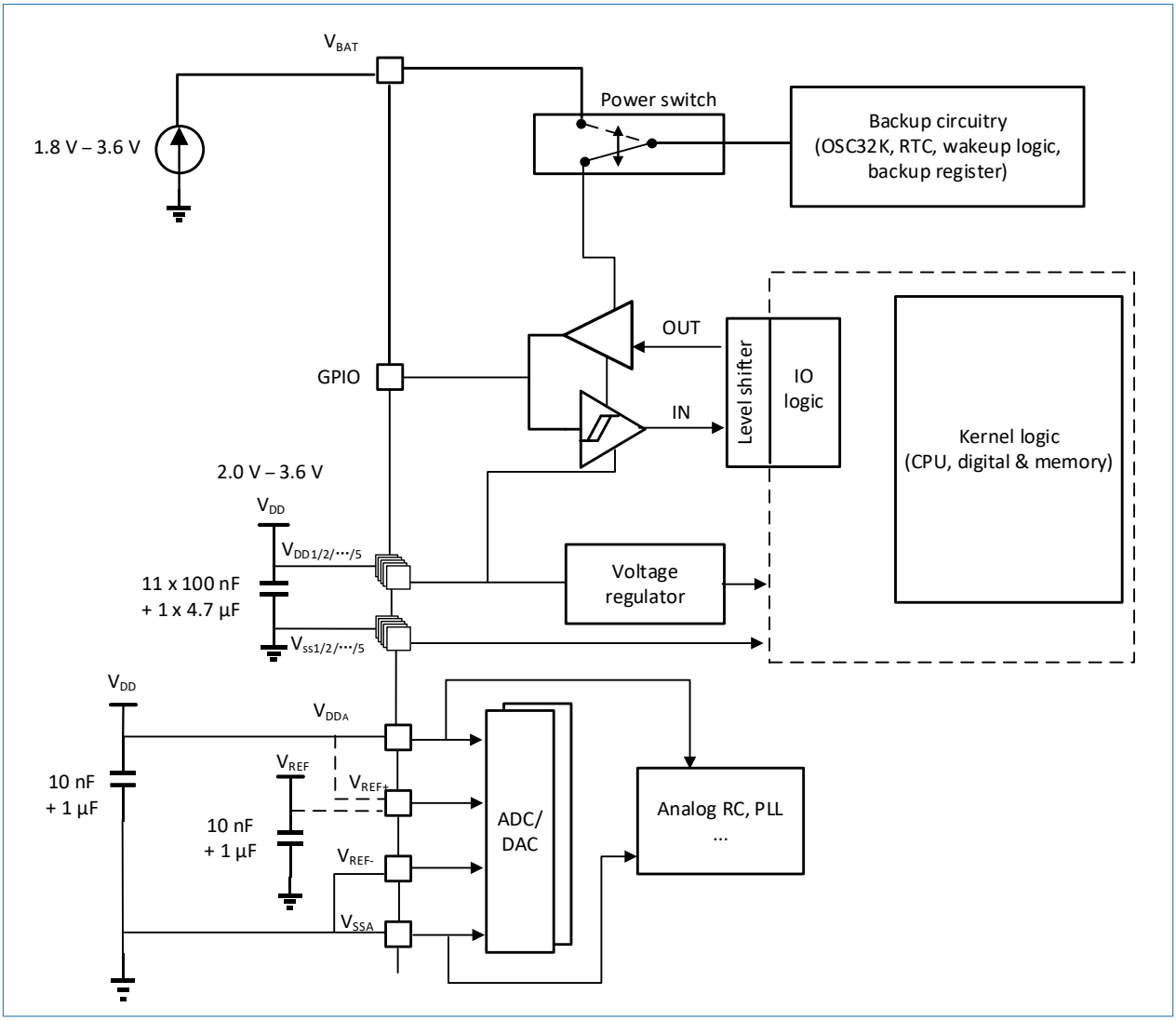

Figure 5-1 Power supply block diagram

6 Pinouts and pin descriptions

HK32F103xCxDxE MCUs are delivered in two packages: LQFP64 and LQFP100.

6.1 LQFP64

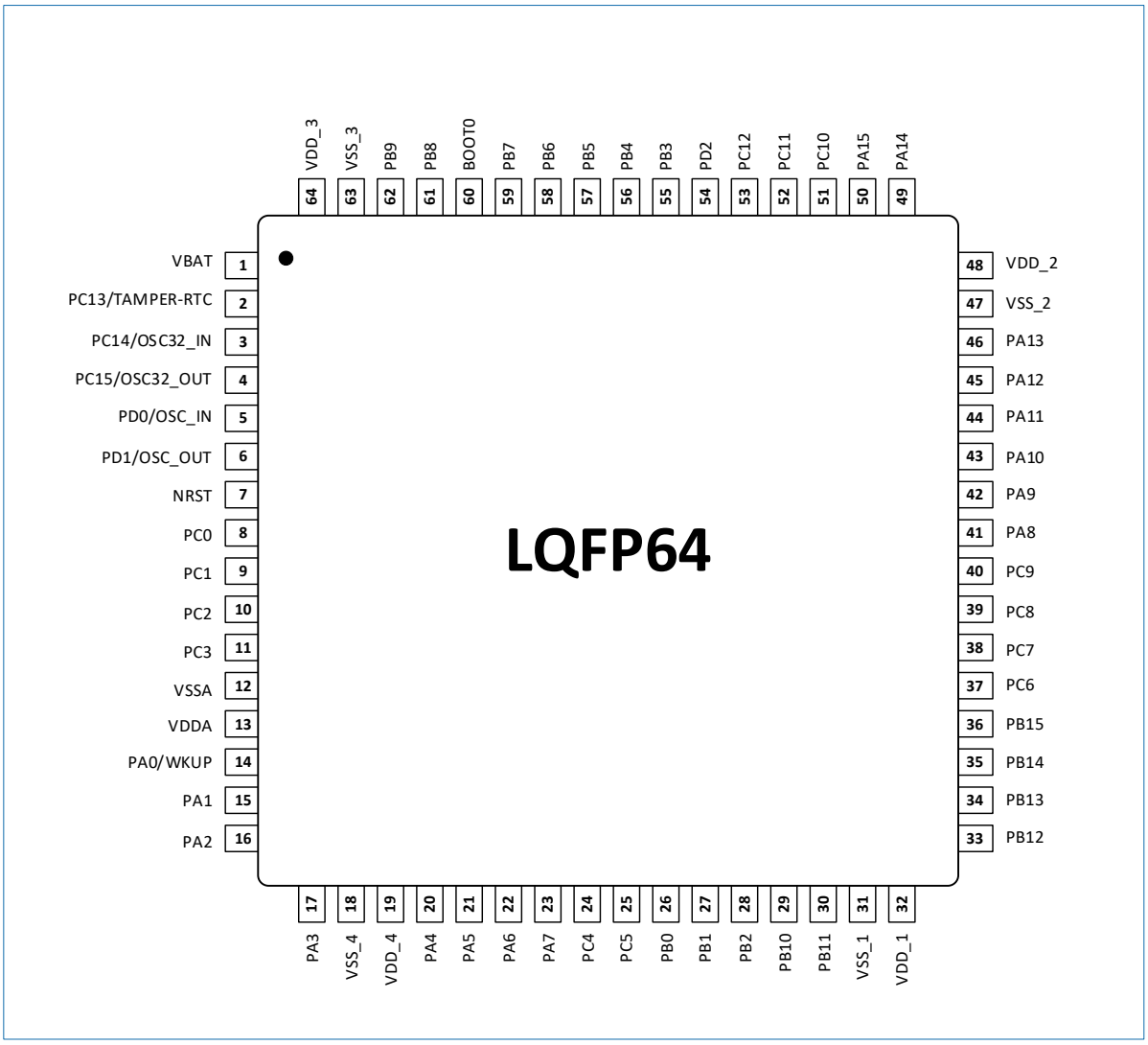

Figure 6-1 LQFP64 package pinout

6.2 LQFP100

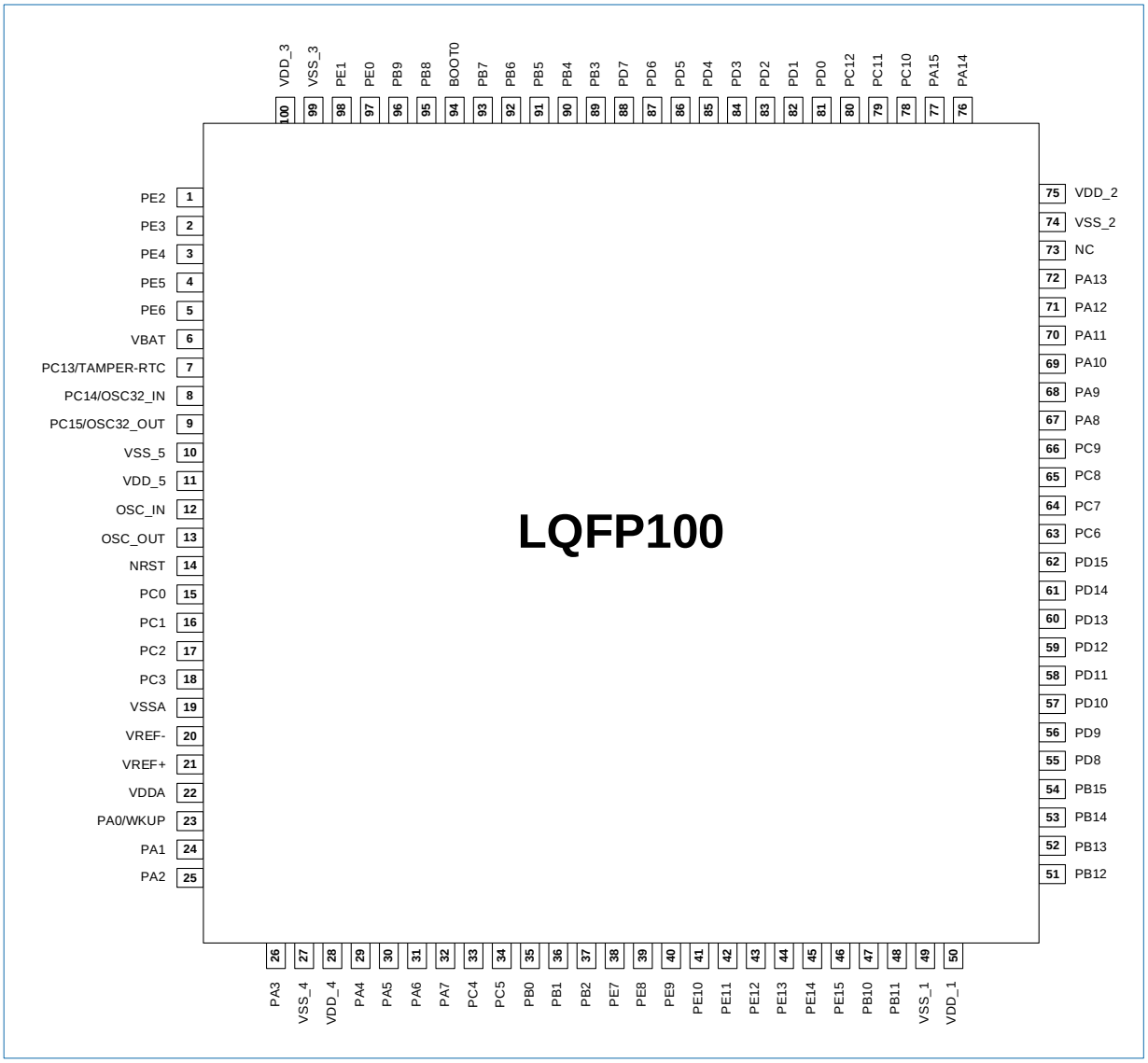

Figure 6-2 LQFP100 package pinout

6.3 LQFP64/LQFP100 pin description

The following table shows pin descriptions of the LQFP64 and LQFP100 packages.

Table 6-1 LQFP64/LQFP100 pin descriptions

LQFP64	LQFP100	Pin Name	Type(1)	5-V tolerant(2)	Main Function	Alternate Function	Additional Function
-	1	PE2	I/O	-	PE2	TRACECKO/FSMC_A23	TXEV/EXTIN2
-	2	PE3	I/O	-	PE3	TRACEDO0/FSMC_A19	TXEV/EXTIN3
-	3	PE4	I/O	-	PE4	TRACEDO1/FSMC_A20	TXEV/EXTIN4
-	4	PE5	I/O	-	PE5	TRACEDO2/FSMC_A21	TXEV/EXTIN5
-	5	PE6	I/O	FT	PE6	TRACEDO3/FSMC_A22	TXEV/EXTIN6
1	6	VBAT	S	-	VBAT	-	-
2	7	PC13/TAMPER-RTC	I/O (3)	-	PC13	TAMPER-RTC/WKUP1/RTCO	TXEV/EXTIN13
3	8	PC14/OSC32_IN	I/O (3)	-	PC14	OSC32_IN/LSE_CKI	TXEV/EXTIN14
4	9	PC15/OSC32_OUT	I/O (3)	-	PC15	OSC32_OUT	TXEV/EXTIN15
-	10	VSS_5	S	-	VSS_5	-	-
-	11	VDD_5	S	-	VDD_5	-	-

LQFP64	LQFP100	Pin Name	Type(1)	5-V tolerant(2)	Main Function	Alternate Function	Additional Function
5	-	PD0/OSC_IN	I/O	-	OSC_IN	OSC_IN/HSE_CKI	TXEV/PD0
6	-	PD1/OSC_OUT	I/O	-	OSC_OUT	OSC_OUT	TXEV/PD1
-	12	OSC_IN	I	-	OSC_IN	OSC_IN/HSE_CKI	-
-	13	OSC_OUT	O	-	OSC_OUT	OSC_OUT	-
7	14	NRST	I/O	-	NRST	-	-
8	15	PC0	I/O	-	PC0	ADC123_IN10	TXEV/EXTIN0
9	16	PC1	I/O	-	PC1	ADC123_IN11	TXEV/EXTIN1
10	17	PC2	I/O	-	PC2	ADC123_IN12	TXEV/EXTIN2
11	18	PC3	I/O	-	PC3	ADC123_IN13	TXEV/EXTIN3
12	19	VSSA	S	-	VSSA	-	-
-	20	VREF-	S	-	VREF-	-	-
-	21	VREF+	S	-	VREF+	-	-
13	22	VDDA	S	-	VDDA	-	-
14	23	PA0/WKUP	I/O (2)	-	PA0	WKUP0/USART2_CTS/ ADC123_IN0/TIM2_CH1 _ETR/TIM5_CH1/TIM8_ ETR/ EXTIN0	TXEV
15	24	PA1	I/O	-	PA1	USART2_RTS/ADC123_I N1/ TIM5_CH2/TIM2_CH2/ EXTIN1	TXEV
16	25	PA2	I/O	-	PA2	USART2_TX/TIM5_CH3/ ADC123_IN2/TIM2_CH3 / EXTIN2	TXEV
17	26	PA3	I/O	-	PA3	USART2_RX/TIM5_CH4/ ADC123_IN3/TIM2_CH4 / EXTIN3	TXEV
18	27	VSS_4	S	-	VSS_4	-	-
19	28	VDD_4	S	-	VDD_4	-	-
20	29	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK/ DAC1_OUT/ADC12_IN4 / EXTIN4	TXEV
21	30	PA5	I/O	-	PA5	SPI1_SCK/DAC2_OUT/ ADC12_IN5/EXTIN5	TXEV
22	31	PA6	I/O	-	PA6	SPI1_MISO/TIM8_BKIN/ ADC12_IN6/TIM3_CH1/ EXTIN6	TXEV/TIM1_BKIN
23	32	PA7	I/O	-	PA7	SPI1_MOSI/TIM8_CH1N /ADC12_IN7/TIM3_CH2 /EXTIN7	TXEV/TIM1_CH1N
24	33	PC4	I/O	-	PC4	ADC12_IN14	TXEV/EXTIN4
25	34	PC5	I/O	-	PC5	ADC12_IN15	TXEV/EXTIN5
26	35	PB0	I/O (3)	-	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TXEV/TIM1_CH2N/EXTIN0
27	36	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TXEV/TIM1_CH3N/EXTIN1
28	37	PB2	I/O	FT	PB2	BOOT1(4)	TXEV/EXTIN2
-	38	PE7	I/O	FT	PE7	FSMC_D4	TXEV/TIM1_ETR/EXTIN7
-	39	PE8	I/O	FT	PE8	FSMC_D5	TXEV/TIM1_CH1N/EXTIN8
-	40	PE9	I/O	FT	PE9	FSMC_D6	TXEV/TIM1_CH1/EXTIN9
-	41	PE10	I/O	FT	PE10	FSMC_D7	TXEV/TIM1_CH2N/EXTIN10
-	42	PE11	I/O	FT	PE11	FSMC_D8	TXEV/TIM1_CH2/EXTIN11
-	43	PE12	I/O	FT	PE12	FSMC_D9	TXEV/TIM1_CH3N/EXTIN12
-	44	PE13	I/O	FT	PE13	FSMC_D10	TXEV/TIM1_CH3/EXTIN13
-	45	PE14	I/O	FT	PE14	FSMC_D11	TXEV/TIM1_CH4/EXTIN14
-	46	PE15	I/O	FT	PE15	FSMC_D12	TXEV/TIM1_BKIN/EXTIN15
29	47	PB10	I/O	-	PB10	I2C2_SCL/USART3_TX	TXEV/TIM2_CH3/EXTIN10

LQFP64	LQFP100	Pin Name	Type(1)	5-V tolerant(2)	Main Function	Alternate Function	Additional Function
30	48	PB11	I/O	-	PB11	I2C2_SDA/USART3_RX	TXEV/TIM2_CH4/EXTIN11
31	49	VSS_1	S	-	VSS_1	-	-
32	50	VDD_1	S	-	VDD_1	-	-
33	51	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN	TXEV/EXTIN12
34	52	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK/ USART3_CTS/TIM1_CH1N	TXEV/EXTIN13
35	53	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N / USART3_RTS	TXEV/EXTIN14
36	54	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD/ TIM1_CH3N	TXEV/EXTIN15
-	55	PD8	I/O	FT	PD8	FSMC_D13	TXEV/USART3_TX/EXTIN8
-	56	PD9	I/O	FT	PD9	FSMC_D14	TXEV/USART3_RX/EXTIN9
-	57	PD10	I/O	FT	PD10	FSMC_D15	TXEV/USART3_CK/EXTIN10
-	58	PD11	I/O	FT	PD11	FSMC_A16_CLE	TXEV/USART3_CTS/ EXTIN11
-	59	PD12	I/O	FT	PD12	FSMC_A17_ALE	TXEV/TIM4_CH1/ USART3_RTS/EXTIN12
-	60	PD13	I/O	FT	PD13	FSMC_A18	TXEV/TIM4_CH2/EXTIN13
-	61	PD14	I/O	FT	PD14	FSMC_D0	TXEV/TIM4_CH3/EXTIN14
-	62	PD15	I/O	FT	PD15	FSMC_D1	TXEV/TIM4_CH4/EXTIN15
37	63	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/SDIO_D6	TXEV/TIM3_CH1/EXTIN6
38	64	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/SDIO_D7	TXEV/TIM3_CH2/EXTIN7
39	65	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TXEV/TIM3_CH3/EXTIN
40	66	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TXEV/TIM3_CH4/EXTIN9
41	67	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ RCC_MCO/EXTIN8	TXEV
42	68	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2/ EXTIN9	TXEV
43	69	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3/ EXTIN10	TXEV
44	70	PA11	I/O	FT	PA11	USART1_CTS/USB_DM/ CAN1_RX/TIM1_CH4/ EXTIN11	TXEV
45	71	PA12	I/O	FT	PA12	USART1_RTS/USB_DP/ CAN1_TX/TIM1_ETR/EXTIN12	TXEV
46	72	PA13/JTMS-SWDIO	I/O	FT	JTMS-SWDIO	-	TXEV/PA13
-	73	NC	-	-	-	-	-
47	74	VSS_2	S		VSS_2	-	-
48	75	VDD_2	S		VDD_2	-	-
49	76	PA14/JTCK-SWCLK	I/O	FT	JTCK-SWCLK	EXTIN14	TXEV/PA14
50	77	PA15/JTDI	I/O	FT	JTDI	SPI3_NSS/I2S3_WS/EXTIN15	TXEV/PA15/TIM2_CH1_ETR /SPI1_NSS
51	78	PC10	I/O	-	PC10	UART4_TX/SDIO_D2	TXEV/USART3_TX/EXTIN10
52	79	PC11	I/O	-	PC11	UART4_RX/SDIO_D3	TXEV/USART3_RX/EXTIN11
53	80	PC12	I/O	-	PC12	UART5_TX/SDIO_CK	TXEV/USART3_CK/EXTIN12
-	81	PD0	I/O	-	PD0	FSMC_D2	TXEV/CAN1_RX/EXTIN0
-	82	PD1	I/O	FT	PD1	FSMC_D3	TXEV/CAN1_TX/EXTIN1
54	83	PD2	I/O	-	PD2	TIM3_ETR/UART5_RX/ SDIO_CMD	TXEV/EXTIN2
-	84	PD3	I/O	FT	PD3	FSMC_CLK	TXEV/USART2_CTS/EXTIN3
-	85	PD4	I/O	FT	PD4	FSMC_NOE	TXEV/USART2_RTS/EXTIN4
-	86	PD5	I/O	FT	PD5	FSMC_NWE	TXEV/USART2_TX/EXTIN5

LQFP64	LQFP100	Pin Name	Type(1)	5-V tolerant(2)	Main Function	Alternate Function	Additional Function
-	87	PD6	I/O	FT	PD6	FSMC_NWAIT	TXEV/USART2_RX/EXTIN6
-	88	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	TXEV/USART2_CK/EXTIN7
55	89	PB3/JTDO	I/O	-	JTDO	TRACESWO/SPI3_SCK/ I2S3_CK	TXEV/PB3/TIM2_CH2/ SPI1_SCK/EXTIN3
56	90	PB4/NJRST	I/O	-	NJTRST	SPI3_MISO	TXEV/PB4/TIM3_CH1/ SPI1_MISO/EXTIN4
57	91	PB5	I/O	-	PB5	I2C1_SMBA/SPI3_MOSI / I2S3_SD	TXEV/TIM3_CH2/ SPI1_MOSI/EXTIN5
58	92	PB6	I/O	-	PB6	I2C1_SCL/TIM4_CH1	TXEV/USART1_TX/EXTIN6
59	93	PB7	I/O	FT	PB7	I2C1_SDA/FSMC_NADV / TIM4_CH2	TXEV/USART1_RX/EXTIN7
60	94	BOOT0(4)	I	-	BOOT0(4)	-	-
61	95	PB8	I/O	-	PB8	TIM4_CH3/SDIO_D4	TXEV/I2C1_SCL/CAN1_RX/ EXTIN8
62	96	PB9	I/O	-	PB9	TIM4_CH4/SDIO_D5	TXEV/I2C1_SDA/CAN1_TX/ EXTIN9
-	97	PE0	I/O	FT	PE0	TIM4_ETR/FSMC_NBL0	TXEV/EXTIN0
-	98	PE1	I/O	FT	PE1	FSMC_NBL1	TXEV/EXTIN1
63	99	VSS_3	S		VSS_3	-	-
64	100	VDD_3	S		VDD_3	-	-

(1). I = input, O = output, I/O = input/output, S = supply.

(2). FT: 5 V tolerant.

(3). Except for these pins, the other I/Os have the Schmitt function and can be configured via registers.

(4). BOOT0/BOOT1 pin is connected to an internal weak pull-down resistor.

7 Packages

7.1 Package outlines

7.1.1 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch package.

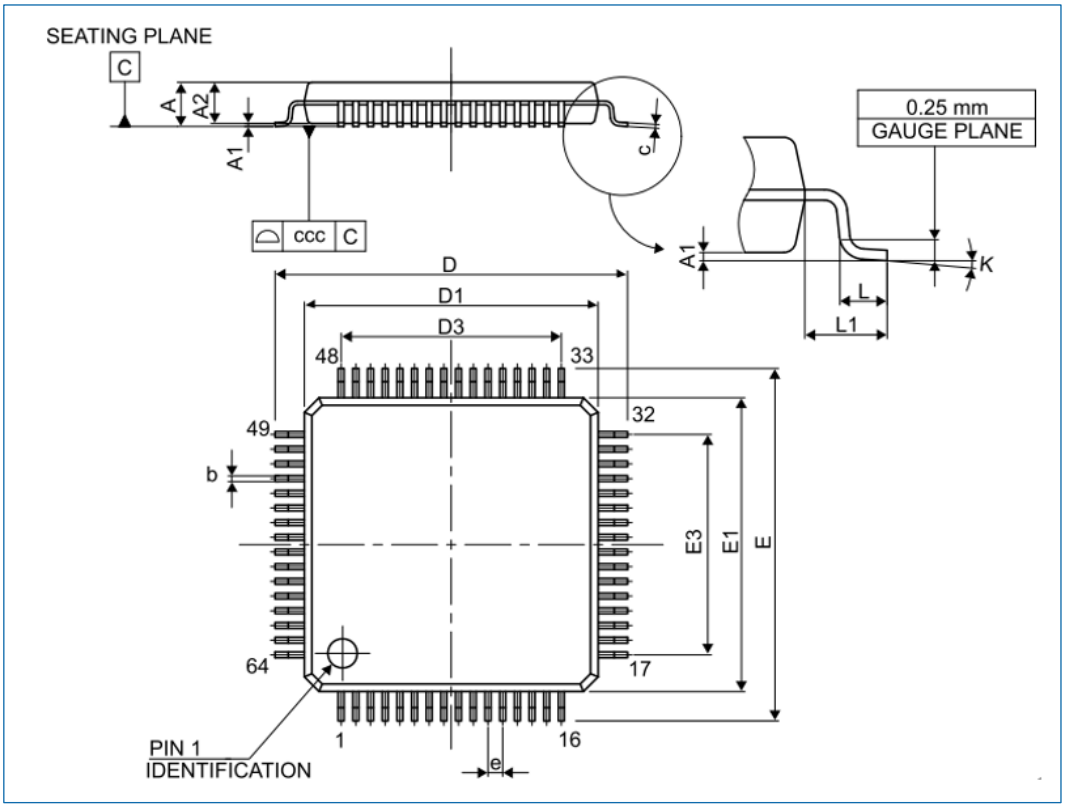

Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP100

LQFP100 is a 14 mm × 14 mm, 0.5 mm pitch package.

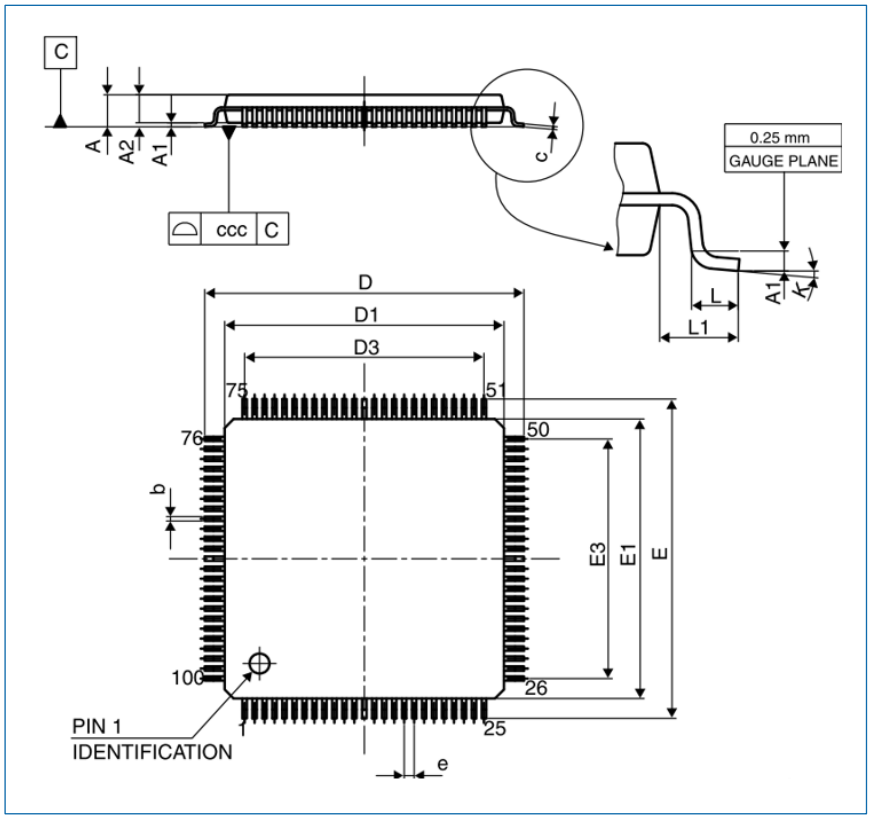

Figure 7-2 LQFP100 package outline

Table 7-2 LQFP100 package parameters

Symbol	Unit: mm			Inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-3 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP64 marking

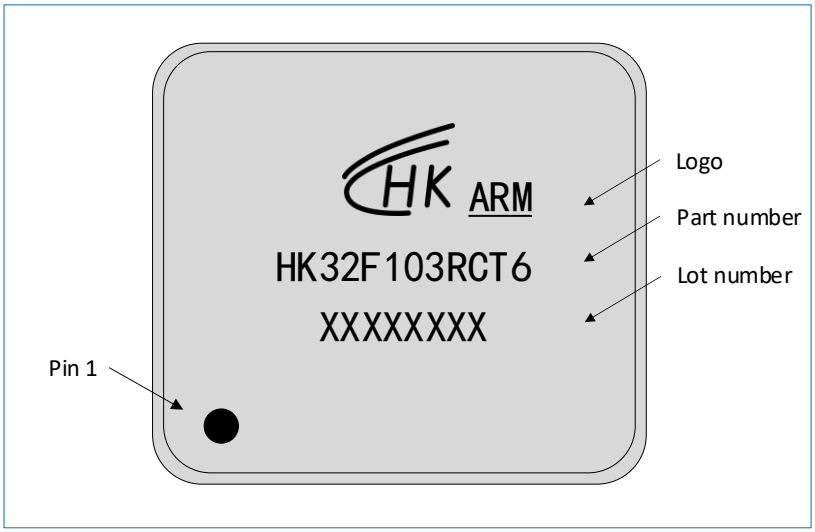

Figure 7-3 LQFP64 HK32F103RCT6 marking example

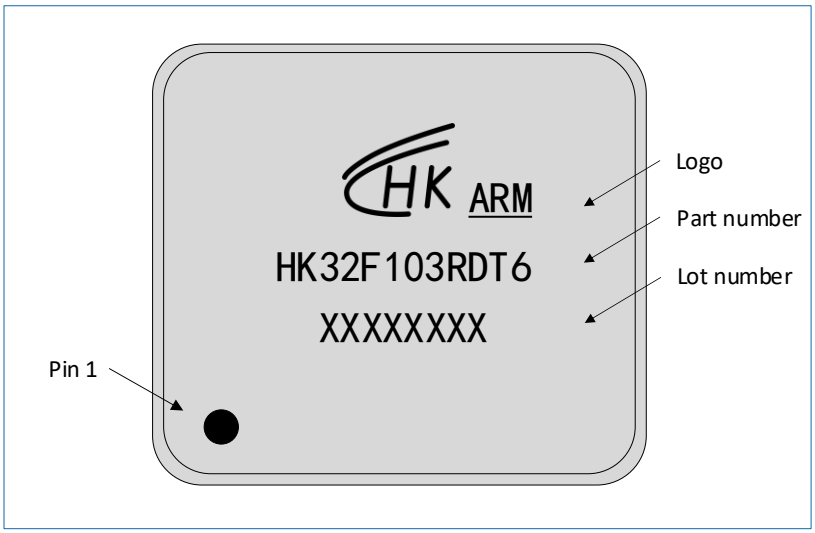

Figure 7-4 LQFP64 HK32F103RDT6 marking example

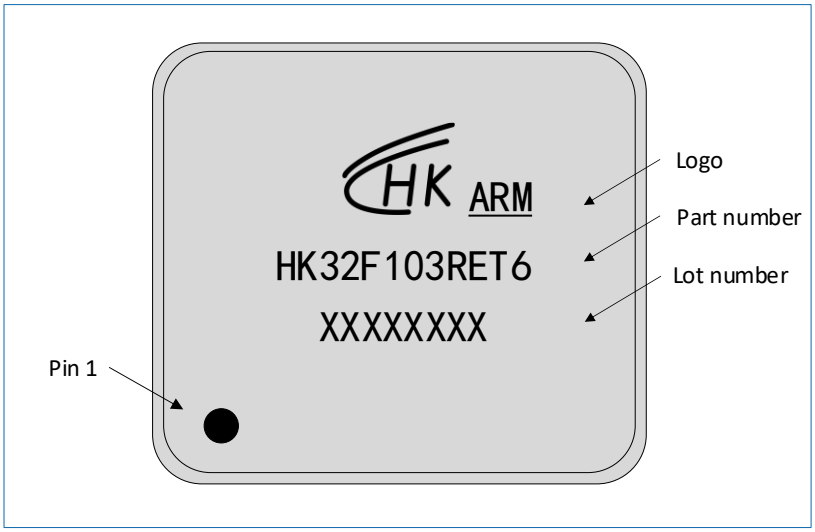

Figure 7-5 LQFP64 HK32F103RET6 marking example

7.2.2 LQFP100 marking

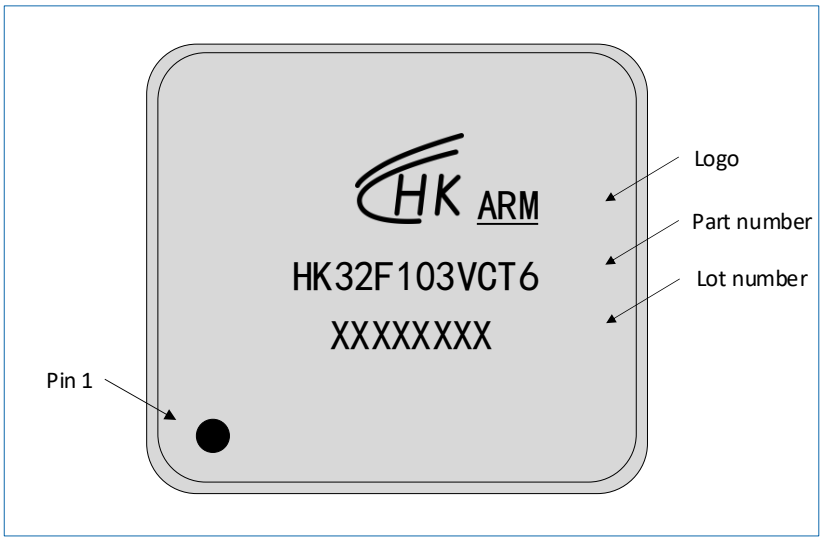

Figure 7-6 LQFP100 HK32F103VCT6 marking example

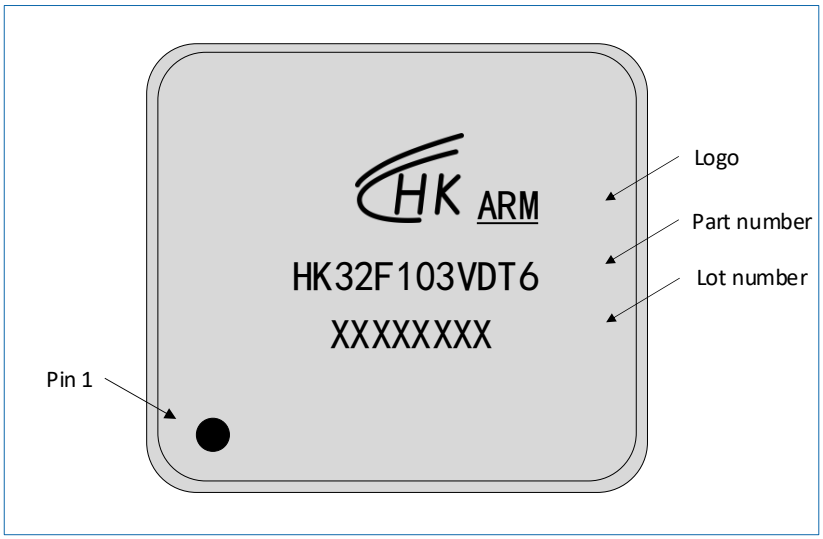

Figure 7-7 LQFP100 HK32F103VDT6 marking example

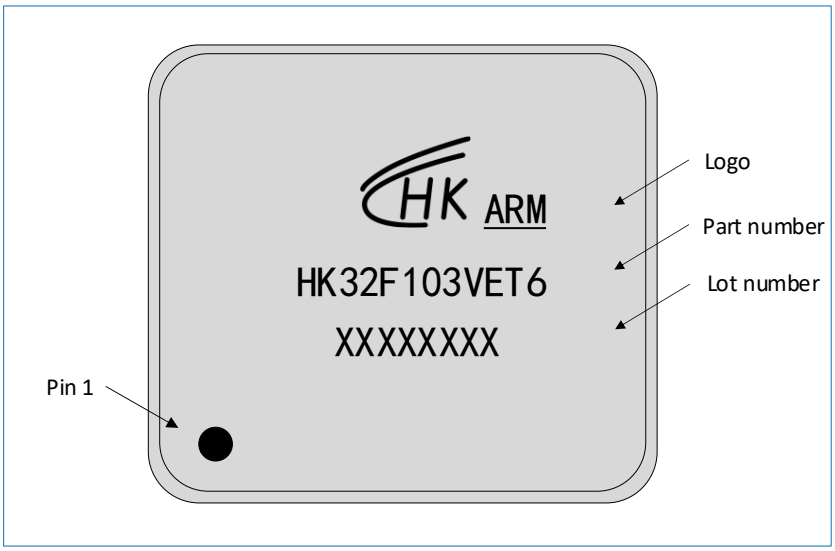

Figure 7-8 LQFP100 HK32F103VET6 marking example

8 Ordering information

8.1 Device numbering conventions

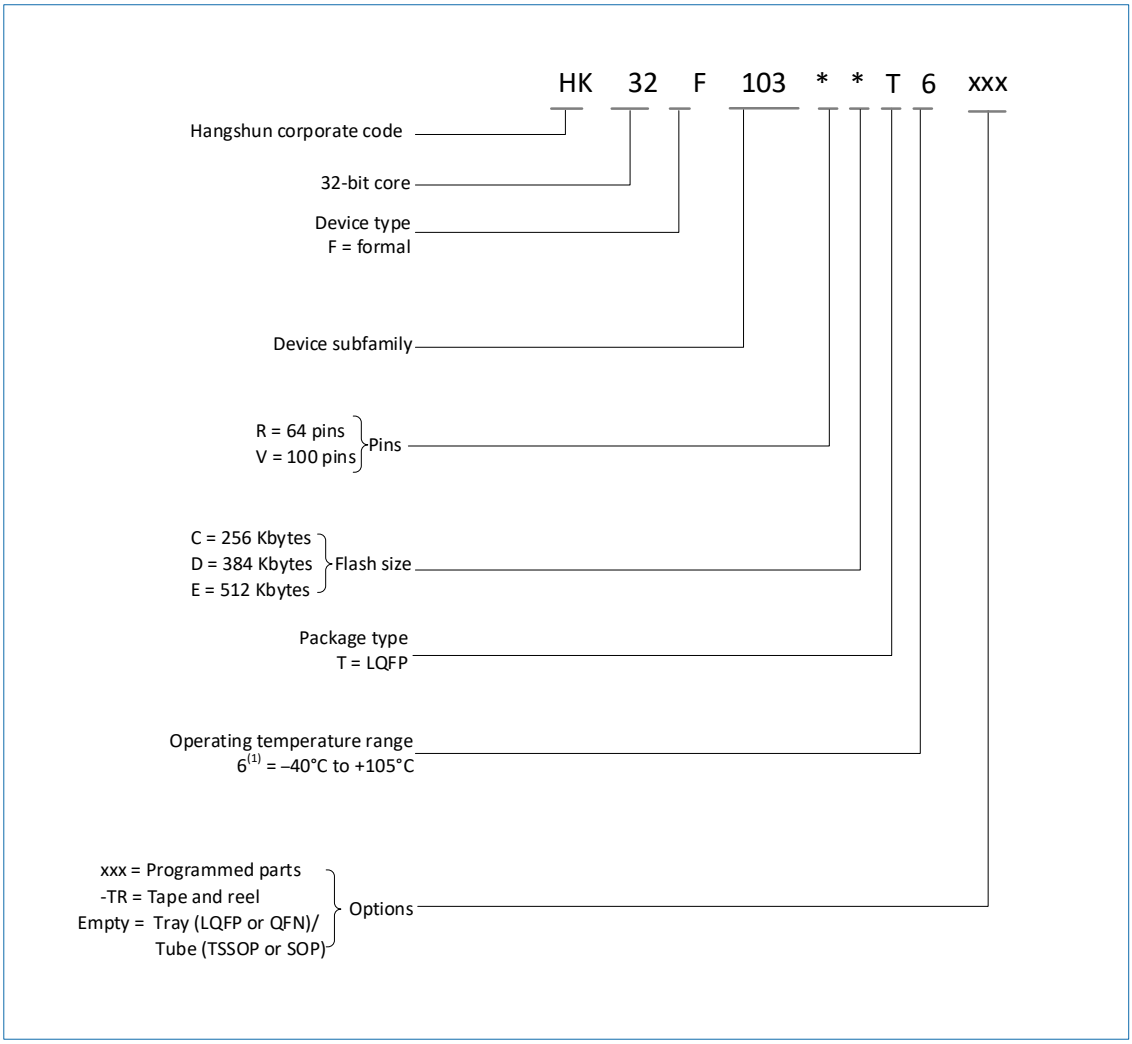

Figure 8-1 Device numbering conventions

(1). The HK32F103xCxDxE series was first released in earlier times, so its device numbering is based on *Hangshun Product Naming Conventions V0.9*, which is slightly different from the latest naming conventions.

8.2 Packaging information

Table 8-1 Packaging information

Package	Part Number	Shipping Option	Remarks
LQFP64	HK32F103RCT6	Tray	
LQFP64	HK32F103RCT6-TR	Tape and reel	
LQFP64	HK32F103RDT6	Tray	
LQFP64	HK32F103RDT6-TR	Tape and reel	
LQFP64	HK32F103RET6	Tray	
LQFP64	HK32F103RET6-TR	Tape and reel	
LQFP100	HK32F103VCT6	Tray	
LQFP100	HK32F103VCT6-TR	Tape and reel	
LQFP100	HK32F103VDT6	Tray	
LQFP100	HK32F103VDT6-TR	Tape and reel	
LQFP100	HK32F103VET6	Tray	
LQFP100	HK32F103VET6-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DCMI	Digital Camera Memory Interface
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
FM	Fast Mode
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSB	Least Significant Bit
LSE	Low-Speed External (clock signal)
LSI	Low-speed Internal (clock signal)
LVD	Low Voltage Detector
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSPS	Million Samples per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PVD	Programmable Voltage Detector
PWM output	Pulse Width Modulation
QSPI	Queued Serial Peripheral Interface
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTC	Real-time Clock
SAI	Serial Audio Interface
SDIO	Secure Digital Input and Output
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TRNG	True Random Number Generator
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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