HK32F103x8xB Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F103x8xB series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32F103x8xB.

Audience

This document is intended for:

- HK32F103x8xB developers
- HK32F103x8xB testers
- HK32F103x8xB users

Release Notes

This document is applicable to HK32F103x8xB series MCUs.

Revision History

Version	Date	Description
1.0.0	2018/06/08	The initial release.
1.1.0	2019/08/16	Added section "3.27 DVSQ unit".
1.1.1	2020/06/19	Updated section "3.14 DMA".
1.1.2	2020/08/23	Updated section "3.9.1 Clock tree".
1.1.3	2021/01/26	Updated section "4.2.14 ADC characteristics".
1.1.4	2021/07/06	Updated section "3.2 Memory mapping".
1.1.5	2021/07/20	Added sections "3.9 Reset" and "3.10 Clock".
1.2	2023/11/03	1. Updated sections "2.2 Device overview", "3.1 Block diagram", "3.8 NVIC", and "3.24 SPI". 2. Updated Table 3-2 Reset status flags. 3. Updated the clock tree in section "3.10 Clocks". 4. Updated section "5.3 LQFP48/LQFP64 pin descriptions".

Contents

1 Introduction

This document is the datasheet for HK32F103x8xB series MCUs. HK32F103x8xB is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun) for a wide range of purposes. This MCU family includes the HK32F103x8T6 and HK32F103xBT6 sub-series. Their part numbers include:

- HK32F103x8T6
  - HK32F103C8T6 (LQFP48 package)
  - HK32F103R8T6 (LQFP64 package)
- HK32F103xBT6
  - HK32F103CBT6 (LQFP48 package)
  - HK32F103RBT6 (LQFP64 package)

For more details on HK32F103x8xB, see *HK32F103x8xB User Manual*.

2 Product overview

HK32F103x8xB adopts the high-performance ARM® Cortex®-M3 core operating at a maximum frequency of 96 MHz.

HK32F103x8xB embeds a 64/128-Kbyte Flash and a 20-Kbyte SRAM.

HK32F103x8xB embeds an advanced timer and three general-purpose timers.

HK32F103x8xB has the following communication interfaces: two SPI interfaces, two I2C interfaces, three USART interfaces, a USB 2.0 full-speed communication interface, a CAN bus, two 12-bit SAR ADCs, and an internal temperature sensor.

With its diversified peripherals, HK32F103x8xB is suitable for a variety of applications:

- Industry applications, such as programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- CPU core
  - ARM® Cortex®-M3
  - Maximum frequency: 96 MHz
  - 24-bit SysTick timer
  - The CPU event signal can be input to the MCU pin to realize board-level communication with the CPU of other chips.
- Operating voltage range
  - Dual-power supply domains: main power supply V_{DD}: 2.0 V to 5.5 V; backup power supply V_{BAT}: 1.8 V to 5.5 V
  - When the main power supply is powered off:
    - The RTC can be powered from $V_{BAT.}$
    - V_{BAT} supplies power to 20-byte backup registers.
- Operating temperature range: –40°C to 105°C
- V_{DD} typical operating current
  - Run mode: 13.232 mA@96 MHz@3.3 V
  - Sleep mode: 5.441 mA@96 MHz@3.3 V
  - Stop mode:
    - LDO operating at full speed: 128 µA@3.3 V
    - LDO in the low-power state: 10.26 µA@3.3 V
  - Standby mode: 1.64 µA@3.3 V
- Memory

- 64/128-Kbyte Flash
  - No wait states to access Flash when the CPU frequency is 24 MHz or lower
  - Separate read and write protection to protect code
- 20-Kbyte on-chip SRAM

- DMA controller
  - Seven-channel DMA
  - Can be triggered by peripherals such as the timer, ADC, SPI, I2C, and USART
- Clock
  - High-speed external clock (HSE): 4 MHz to 16 MHz (typical value: 8 MHz)
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): 8 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL output clock: 96 MHz (maximum value)
- Reset
  - External pin reset
  - Power-on reset/Power-down reset (POR/PDR)
  - Software reset
  - Watchdog reset (IWDG and WWDG)
  - Low-power management reset
- GPIO
  - 51 GPIO pins in the 64-pin package/37 GPIO pins in the 48-pin package
  - Each GPIO can be used as an external interrupt input
  - Provide up to 20 mA drive current
- Encryption
  - CRC calculation unit
- Data communication interface
  - 3 × USARTs
  - 2 × SPIs
  - 2 × I2Cs
  - 1 × CAN 2.0A/2.0B
  - 1 × full-speed USB 2.0
- Timer
  - 1 × advanced timer: TIM1 (Channels 1-3 support complementary PWM output with programmable inserted dead-times)
  - 3 × general-purpose timers: TIM2/TIM3/TIM4
- Clock-calendar function provided by RTC counter in cooperation with software
- PVD
  - Adjustable eight-level thresholds for detecting voltage
  - Rising edge and falling edge detection configurable
- On-chip analog circuitry

- 2 × 12-bit 1 MSPS ADCs
  - 16 analog input channels in total
  - Support the automatic scan and scan conversion
  - Can be cascaded for master/slave parallel conversion and alternate conversion
- 1 × temperature sensor
  - The analog output is connected to an independent ADC channel.

- Debug and trace port
  - Dual-wire SW-DP
  - Five-wire JTAG
  - Data Watchpoint and Trace (DWT) unit, Flash Patch and Breakpoint (FPB) unit, Instrumentation Trace Macrocell (ITM) unit, and Trace Port Interface Unit (TPIU) embedded
- Reliability
  - Passes HBM1300V/CDM500V/MM200V/LU200mA level tests
  - Meets the AEC-Q100 standard
  - Passes the ATE test under high, low, and normal temperatures
  - Meets the zero-defect IATF 16949 standards

2.2 Device overview

Table 2-1 HK32F103x8xB series features

Feature	HK32F103RBT6	HK32F103R8T6	HK32F103CBT6	HK32F103C8T6
Operating voltage (V_{DD})	2.0 V to 5.5 V			
Operating temperature	–40°C to +105°C			
CPU frequency	96 MHz			
Flash (Kbyte)	128	64	128	64
SRAM (Kbyte)	20			
DMA	1 (7 channels)			
CRC	1			
IWDG	1			
WWDG	1			
USART	3			
I2C	2			
USB	1			
CAN	1			
SPI	2			
SysTick timer	1			
DVSQ	1			
Advanced timer	1			
General-purpose timer	3			
GPIO	51		37	
ADC	2 (each with 16 external channels)		2 (each with 10 external channels)	
Programmable voltage detector (PVD)	1			
Temperature sensor	1			
Package	LQFP64		LQFP48	

3 Function description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor that provides an MCU platform featuring low cost, high performance, and ultra-low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With the ARM Cortex®-M3 core embedded, the HK32F103x8xB family is compatible with ARM tools and software.

The block diagram of HK32F103RBT6 is as follows:

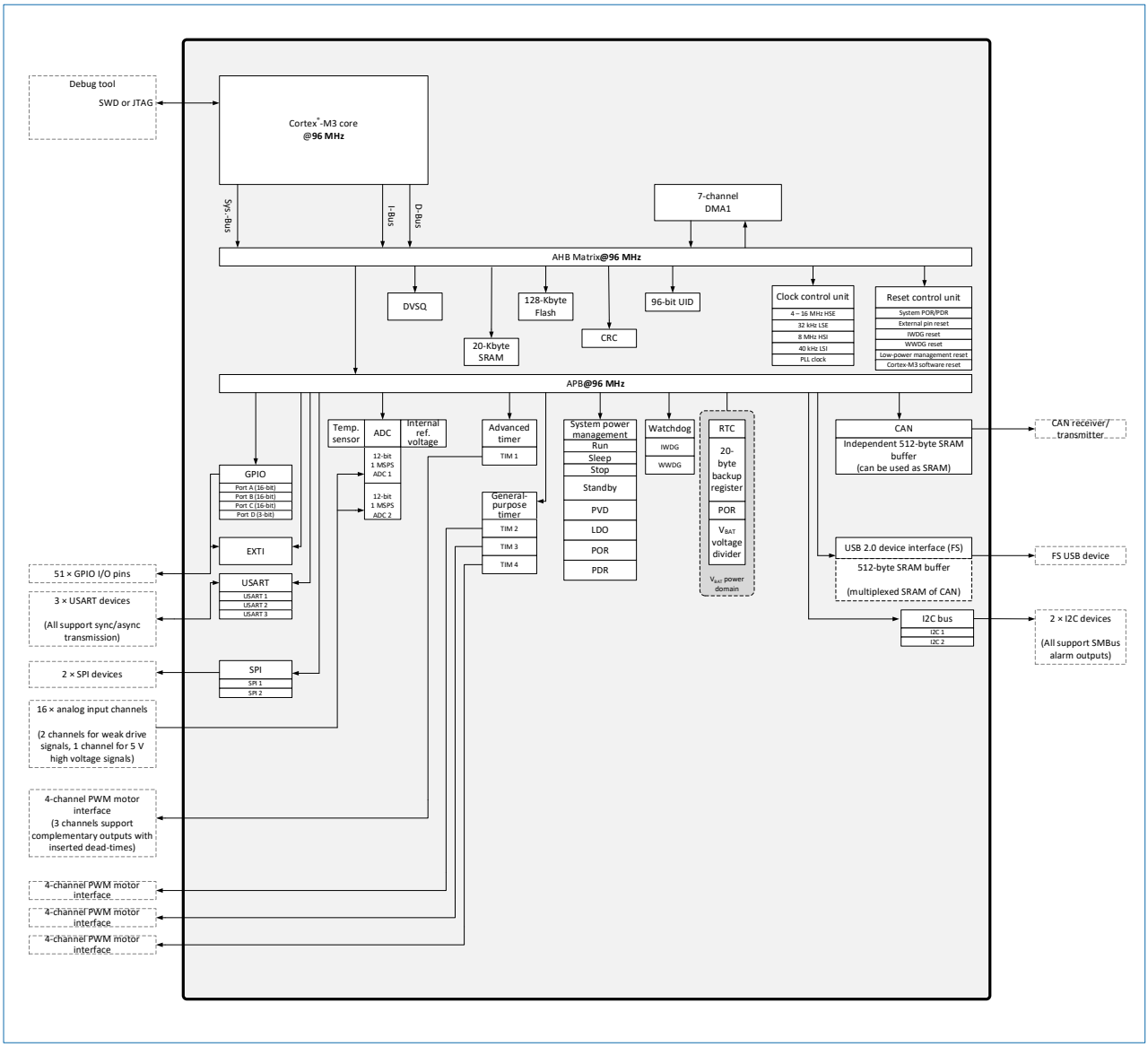

Figure 3-1 HK32F103RBT6 block diagram

3.2 Memory mapping

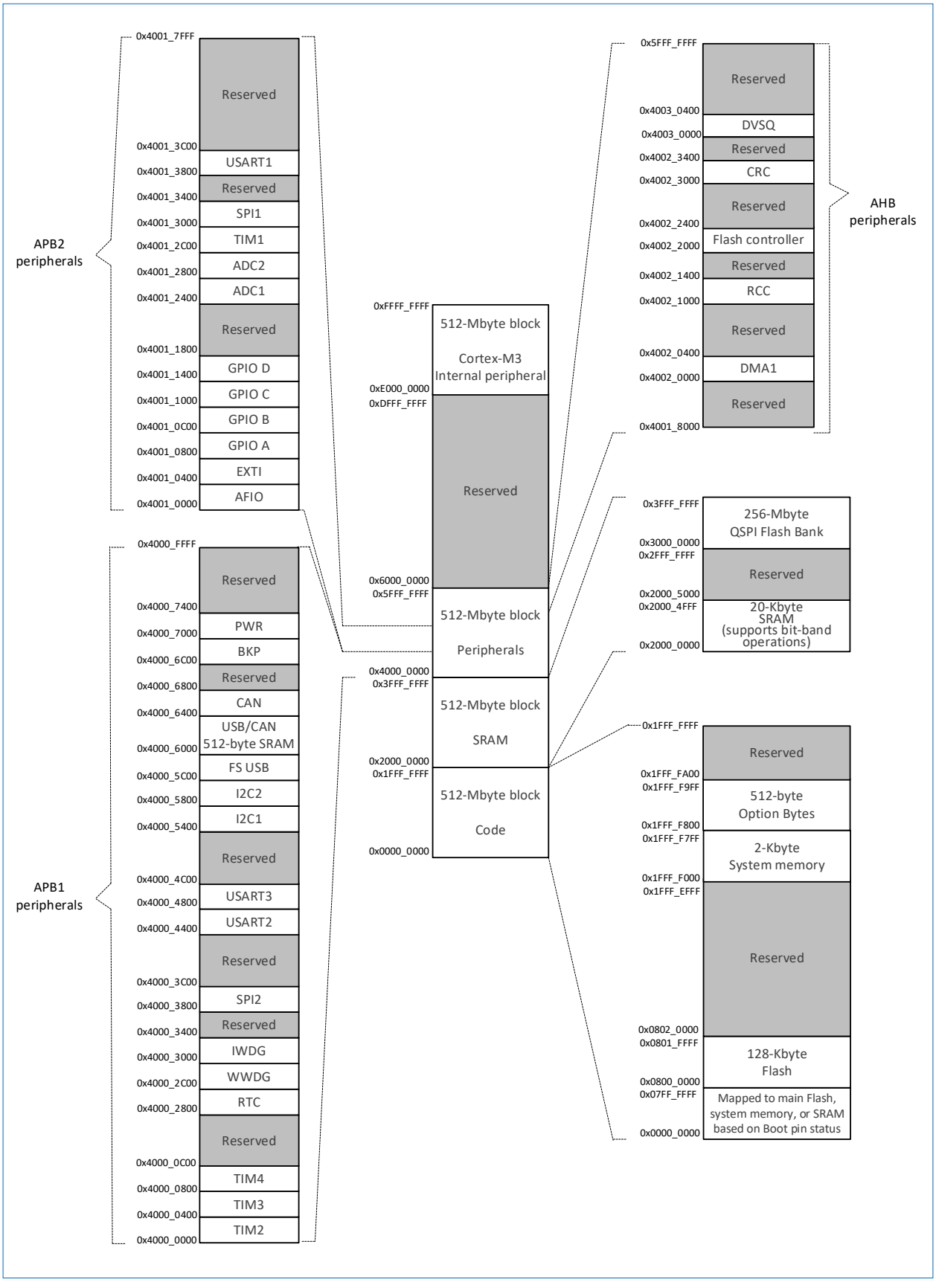

Figure 3-2 Memory mapping

3.3 Flash

HK32F103x8xB integrates a Flash memory of 128 Kbytes to store programs and data. The Flash supports about

1000 cycles of erase and write operations.

3.4 SRAM

HK32F103x8xB integrates a 20-Kbyte SRAM. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.5 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32F103x8xB integrates a CRC calculation unit to reduce the application processing burden and accelerate processing.

3.6 DVSQ calculation unit

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - Supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - High-precision root calculation can be selected for unsigned integer root calculation by using the software.
  - The MOD operation is supported in division.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports divide-by-zero interrupt and overflow interrupt.

3.7 NVIC

HK32F103x8xB incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 44 maskable interrupt channels (excluding 16 Cortex®-M3 interrupt lines) and 16 interrupt priorities while maintaining the lowest interrupt latency.

- The NVIC closely coupled with the core interface ensures low latencies in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

3.8 EXTI

The extended interrupt/event controller (EXTI) is comprised of 19 edge detectors that are used to generate interrupt/event requests. The trigger event of each EXTI line can be independently configured to a rising edge, a falling edge, or both. Each EXTI line can be masked independently. HK32F103x8xB has a pending register that stores the status of each interrupt request.

3.9 Resets

HK32F103x8xB supports the system reset, power reset, and backup domain reset.

3.9.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain.

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW reset)
- Low-power management reset

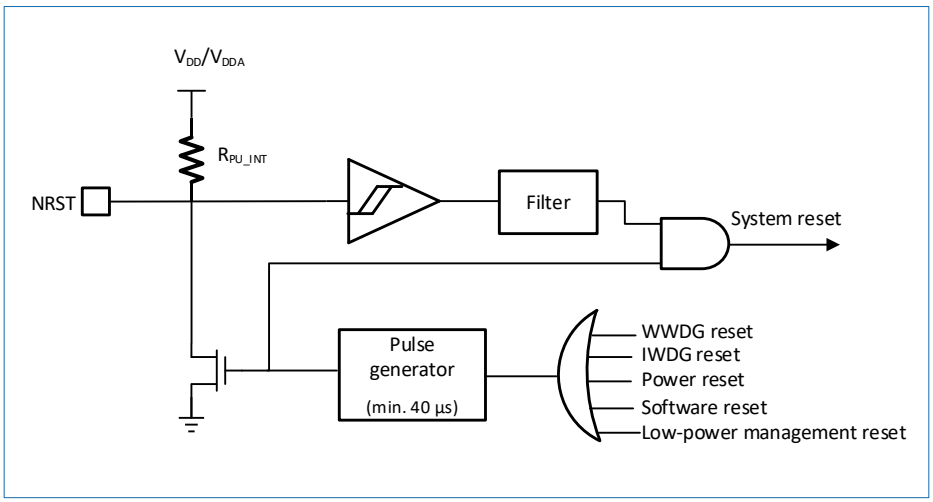

Figure 3-3 Reset signal

The internal reset signal is output on the NRST pin. The pulse generator guarantees a pulse duration of at least 40 µs for each internal or external reset source. When the NRST pin is pulled low and an external reset is generated, a reset pulse is generated.

You can identify a reset source by checking reset status flags in the RCC_CSR register.

Table 3-1 Software reset and low-power management reset

Reset Type	Configuration
Software reset	The SYSRESETREQ bit in Cortex®-M3 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
Low-power management reset	Generating a low-power management reset when entering the Standby mode: Set the nRST_STDBY bit in the option byte to 0 to generate the low-power management reset. This way, even if the system is in the process of entering the Standby mode, it will be reset instead of entering the Standby mode.
	Generating a low-power management reset when entering the Stop mode: Set the nRST_STOP bit in the option byte to 0 to generate the low-power management reset. This way, even if the system is in the process of entering the Stop mode, it will be reset instead of entering the Stop mode.

3.9.2 Power reset

The power reset resets all registers, except for the registers in the backup domain. The reset sources eventually act on the reset pin. The reset pin keeps the low level during resets. The reset entry vector is fixed on address 0x0000_0004.

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Exit from Standby mode

HK32F103x8xB MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system

runs properly when the power supply exceeds the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuits are required.

3.9.3 Backup domain reset

The backup domain has two dedicated resets that only affect the backup domain. A backup domain reset is generated when one of the following events occurs:

- The BDRST bit in the RCC_BDCR register is set. (This also triggers the software reset.)
- V_{DD} or V_{BAT} is powered on after being powered off.

3.10 Clocks

A system clock is selected when the system starts. When a reset occurs, the 8 MHz HSI is selected as the system clock by default. When a failure of the 8 MHz HSI is detected, the 4 – 16 MHz HSE can be selected as the system clock. When a failure of the HSE is detected, the system switches to the internal RC oscillator. If the software interrupt is enabled, a software interrupt is generated. The full interrupt management of the PLL clock can be used as needed (for example, when the external oscillator fails).

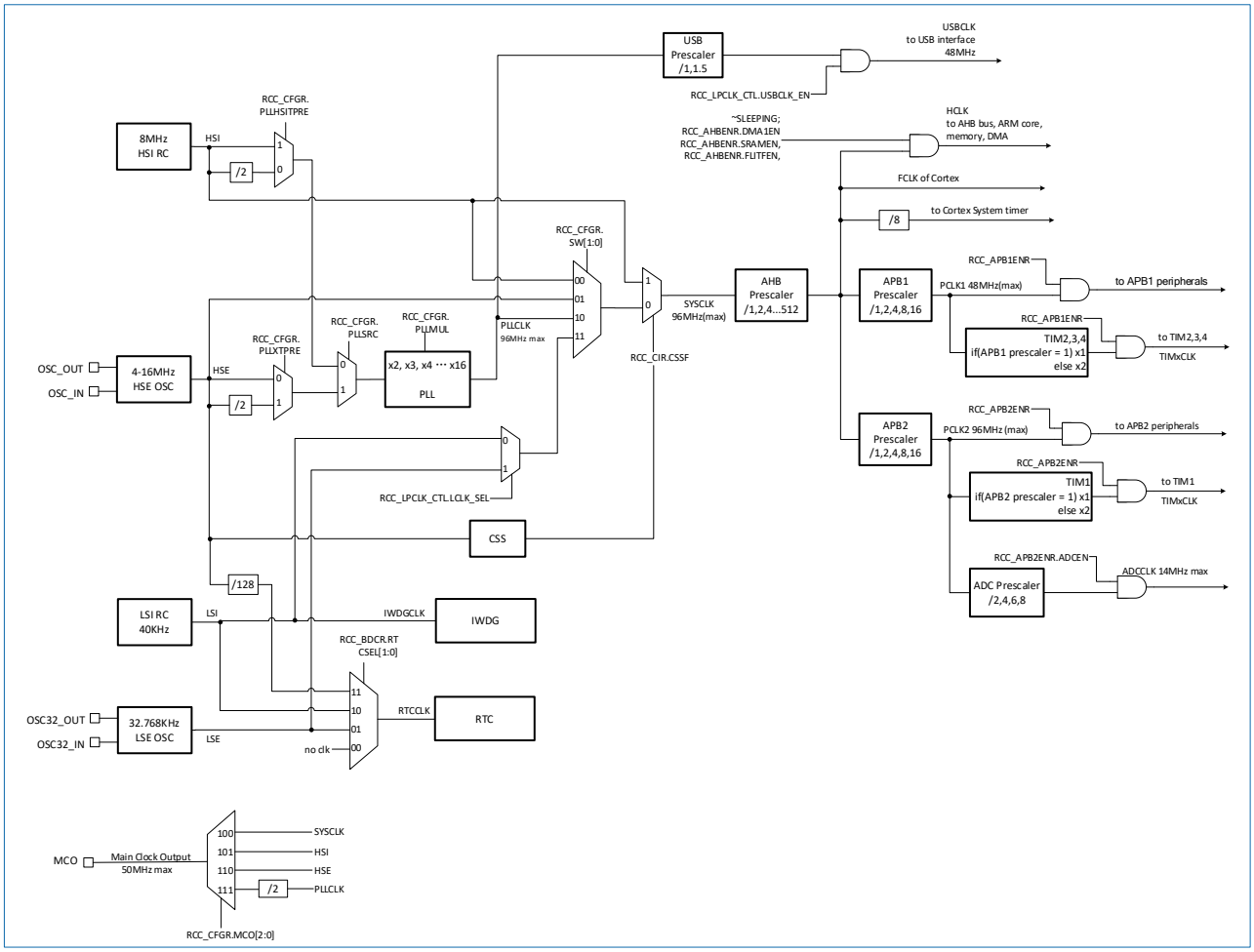

Figure 3-4 Clock tree

3.11 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from main Flash
- Boot from system memory
- Boot from internal SRAM

Bootloader program is stored in the system memory. It can reprogram Flash via the USART1 interface.

3.12 Power supply scheme

- V_{DD} = 2.0 V to 5.5 V

  V_{DD} supplies power to I/O pins and internal low dropout regulators (LDOs).

- V_{DDA} = 2.0 V to 5.5 V

  V_{DDA} supplies power to the analog circuitry, such as the ADC and temperature sensor.

- V_{BAT}: 1.8 V to 5.5 V

  When V_{DD} is powered off, V_{BAT} supplies power to the RTC, external 32.768 kHz oscillator, and backup registers.

3.13 PVD

HK32F103x8xB integrates a programmable voltage detector (PVD). The PVD monitors V_{DD} power supply and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated. The interrupt program may send a warning message or set the MCU to the safe state. The PVD is enabled by setting the register.

3.14 Low-power modes

HK32F103x8xB supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the phase-locked loop (PLL), HSE oscillator, and HSI oscillator are disabled.

  MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any of the 16 external I/O pins, a PVD output, or an RTC alarm signal.

- Standby mode

  In Standby mode, MCUs achieve the lowest power consumption. The internal LDO is disabled. The PLL, HSE oscillator, and HSI oscillator are also disabled. In Standby mode, the SRAM content and register content are lost, except for the registers in the backup domain. The Standby circuitry works as normal.

  MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

  Note: For more information about the power consumption of different low-power modes, see Table 4-7.

3.15 DMA

The general-purpose direct memory access (DMA) controller (with seven channels) manages the data transfer from memories to memories, from peripherals to memories, and from memories to peripherals. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel has a dedicated hardware DMA request logic, and can also be triggered by software. The data size, source address, and destination address of each channel can be set by using the software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, and ADC.

3.16 RTC and BKP

The power supply to RTC and backup registers is controlled by a switch. When V_{DD} is effective, V_{DD} supplies power to RTC and backup registers. Otherwise, V_{BAT} supplies power to RTC and backup registers.

3.16.1 RTC

The real-time clock (RTC) has a set of continuously running counters and can provide the clock calendar function via software. In addition, the RTC provides alarm interrupt and periodic interrupt functions.

The 32.768 kHz external oscillator or an internal low-power RC oscillator can drive RTC. The typical frequency of the internal low-power RC oscillator is 40 kHz. An external 512 Hz signal is used for the compensation of natural quartz deviation. The RTC has a 32-bit programmable counter for long-term measurement in conjunction with the compare register. The RTC has a 20-bit prescaler which is used to generate the time base clock. When the RTC is clocked by the 32.768 kHz crystal oscillator (LSE), a one-second time base is generated.

3.16.2 BKP

Backup registers (BKP) are used to store user application data. The system reset and power reset do not reset backup registers. Backup registers are not reset upon wakeup from Standby mode.

3.17 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. IWDG can be configured as a software or hardware watchdog through the option bytes. In debug mode, the counter can be frozen.

3.18 WWDG

The window watchdog (WWDG) is based on a 7-bit downcounter. The counter can be set to the free running mode or used to reset the system when a problem occurs. The WWDG is clocked by the system clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.19 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.20 General-purpose timer

Every general-purpose timer (TIM2/TIM3/TIM4) provides a 16-bit auto-reload up/down counter, a 16-bit prescaler, and four independent channels. Every channel can be used for input capture, output compare, PWM output, and one-pulse mode output. In the LQFP64 package, up to 16 channels are available for the input capture, output compare, and PWM output. The general-purpose timers can work with the advanced timer through the Timer Link feature for synchronization and event chaining. In debug mode, the counter can be frozen.

Every general-purpose timer can generate PWM outputs and has an independent DMA request mechanism.

3.21 Advanced timer

HK32F103x8xB integrates the advanced timer TIM1. TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare

- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). In debug mode, the counter can be frozen. Many functions of the advanced timer are the same as those of general-purpose timers, and the two types of timers have the same structure. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

3.22 I2C bus

HK32F103x8xB has two I2C bus interfaces. The I2C bus interfaces can work as a master or slave and support the standard and fast modes. They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interfaces have embedded hardware CRC generation/verification. They can be operated by using the DMA controller and support SMBus V2.0/PMBus.

3.23 USART

HK32F103x8xB embeds three universal synchronous/asynchronous receivers/transmitters (USART1/USART2/USART3). These interfaces support asynchronous communication, IrDA SIR ENDEC, multi-processor communication, single-wire half-duplex communication, and LIN Master/Slave capability. All the USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (compliant with ISO 7816), and SPI-like communication mode.

The USART1 interface communicates at a speed of up to 4.5 Mbit/s. The USART2 and USART3 interfaces communicate at a speed of up to 2.25 Mbit/s.

3.24 SPI

HK32F103x8xB has two serial peripheral interfaces (SPIs). In master or slave mode, the full-duplex and half-duplex communication speeds reach 18 Mbit/s. The 3-bit prescaler provides eight master mode frequencies. Each frame can be configured to 8-bit or 16-bit. The hardware CRC generation/verification supports the basic SD card and MMC mode.

All SPI interfaces can be operated by using the DMA controller.

3.25 CAN

HK32F103x8xB has a controller area network (CAN) interface. The CAN interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN interface has three transmit mailboxes and two three-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.26 USB

HK32F103x8xB embeds a USB controller which complies with the full-speed USB device standard. The USB interface endpoint settings can be configured by using the software. It provides suspend/resume support. The dedicated 48 MHz clock of USB is generated by the internal PLL.

3.27 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.28 ADC

HK32F103x8xB embeds two 12-bit analog-to-digital converters (ADCs), each of which has up to 16 external channels. The ADCs perform the conversions in single or scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface include:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be operated by using the DMA controller. The analog watchdog function can realize precise monitoring of the converted voltage of one, some, or all selected channels. When the monitored voltage exceeds the preset threshold, an interrupt is generated. The event generated by the general-purpose timers and advanced timer can be internally connected to the ADC start trigger event and injection trigger event respectively. The application program synchronizes the A/D conversion with timers.

3.29 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.30 Debug and trace port

HK32F103x8xB embeds the ARM SWJ-DP which is a combined JTAG-DP and SW-DP that enables you to connect either a serial wire debug (SWD) or JTAG probe to a target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively. A special signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD} – V_{SS}	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	6.0	V
V_{IN}	Input voltage on pins	V_{SS} – 0.3	V_{DD} + 4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variation between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	mA
I_{IO}	Output current sunk by any I/O and control pin	25	mA
	Output current sourced by any I/O and control pin	–25	mA
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	mA
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	mA

(1). All power (VDD, VDDA) and ground (VSS, VSSA) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When VIN is larger than VDD, a positive injected current is induced; when VIN is smaller than VSS, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum ∑IINJ (PIN) is the sum of the absolute instantaneous values of the positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to +150	°C
T_J	Maximum junction temperature	125	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	48	MHz
f_{PCLK2}	Internal APB2 clock frequency	0	96	MHz
V_{DD}	Standard operating voltage	2	5.5	V

Symbol	Description	Min	Max	Unit
V_{DDA}(1)	Analog operating voltage	2	5.5	V
V_{BAT}	Backup domain operating voltage	1.8	5.5	V
T	Operating temperature	–40	105	°C

(1). It is recommended that you use the same power supply for V_{DD} and V_{DDA}.

4.2.2 Reset characteristics

Table 4-5 Reset characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{delay}	NRST signal establishment time	-	-	40	-	μs
$V_{Threshold}$	Reset threshold	-	-	1.75	-	V

4.2.3 PVD characteristics

Table 4-6 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0] = 000	2.183	2.188	2.196	V
		PLS[2:0] = 001	2.286	2.289	2.298	V
		PLS[2:0] = 010	2.393	2.399	2.407	V
		PLS[2:0] = 011	2.502	2.508	2.518	V
		PLS[2:0] = 100	2.621	2.629	2.639	V
		PLS[2:0] = 101	2.726	2.733	2.745	V
		PLS[2:0] = 110	2.839	2.846	2.855	V
		PLS[2:0] = 111	2.958	2.969	2.979	V
	Programmable voltage detector level selection (falling edge)	PLS[2:0] = 000	2.116	2.119	2.125	V
		PLS[2:0] = 001	2.208	2.211	2.220	V
		PLS[2:0] = 010	2.305	2.310	2.320	V
		PLS[2:0] = 011	2.399	2.406	2.416	V
		PLS[2:0] = 100	2.506	2.512	2.521	V
		PLS[2:0] = 101	2.596	2.602	2.613	V
		PLS[2:0] = 110	2.693	2.701	2.710	V
		PLS[2:0] = 111	2.798	2.805	2.817	V

4.2.4 Operating current characteristics

Table 4-7 Operating current characteristics

Mode	Condition	V_{DD}@25°C			Unit
		2.0 V	3.3 V	5.0 V	
Run mode	HCLK = 96 MHz, three wait states to access Flash, APB clock enabled	21.505	22.63	22.85	mA
	HCLK = 96 MHz, three wait states to access Flash, APB clock disabled	12.908	13.232	13.301	mA
	HCLK = HSE (8 MHz), zero wait states to access Flash, APB clock enabled	3.151	3.418	3.533	mA
	HCLK = HSE (8 MHz), zero wait states to access Flash, APB clock disabled	2.316	2.559	2.653	mA
	HCLK = LSI (40 kHz)	196	208	212	μA
	HCLK = LSE (32.768 kHz)	190	205	215	μA
Sleep mode	HCLK = 96 MHz, APB clock disabled	5.199	5.441	5.483	mA
	HCLK = HSI (8 MHz), APB clock disabled	0.778	0.845	0.937	mA
Stop mode	LDO operating at full speed, HSE, HSI, and LSE disabled	126	128	130	μA
	LDO in low-power mode, HSE, HSI, and LSE disabled	9.22	10.26	12.47	μA
Standby mode	LSI and IWDG disabled	1.13	1.64	3.17	μA
V_{BAT} mode	RTC clocked by LSE	1.56	2.29	5.34	μA
	LSE and RTC stopped	0.03	0.04	0.09	μA

4.2.5 HSE clock characteristics

HK32F103x8xB integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the

chip is recommended:

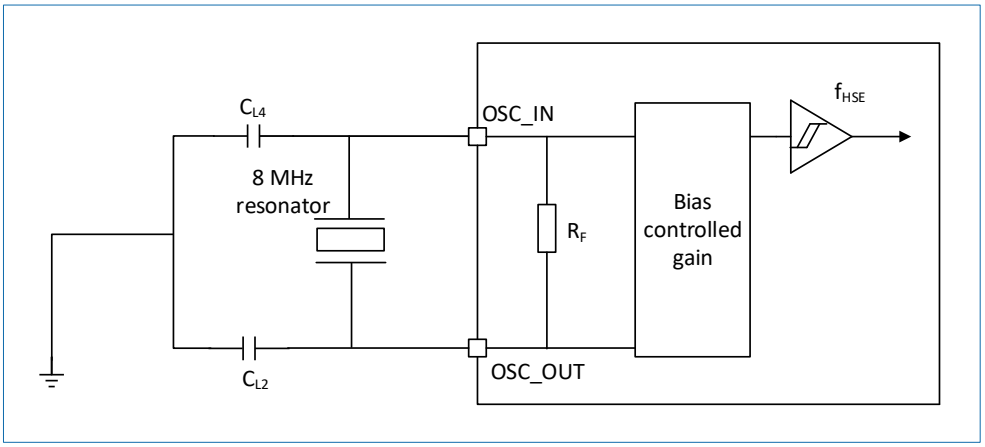

Figure 4-1 Recommended startup circuit outside the chip

Alternatively, an HSE signal can be directly input from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-8 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	Frequency	-	1	8	25	MHz
V_{HSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$T_{w(HSE)}$	Effective high/low level duration		5	-	-	ns
$T_{r(HSE)}/T_{f(HSE)}$	Rise/Fall time		-	-	20	
$Cin_{(HSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.6 LSE clock characteristics

HK32F103x8xB integrates an LSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

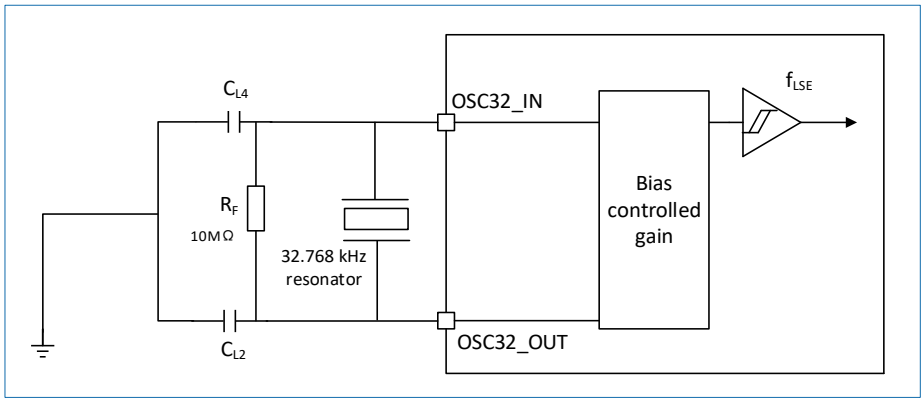

Figure 4-2 Recommended startup circuit outside the chip

Alternatively, an LSE signal can be directly input from the OSC32_IN pin. The following table lists the requirements for this clock signal:

Table 4-9 Characteristics of the input LSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{LSE_ext}	Frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	V
$Tw_{(LSE)}$	Effective high/low level duration		450	-	-	ns
$Tr_{(LSE)}/Tf_{(LSE)}$	Rise/Fall time		-	-	50	ns
$Cin_{(LSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.7 HSI clock characteristics

Table 4-10 Characteristics of the HSI clock

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Oscillator accuracy	Factory trimmed accuracy (ambient temperature)		–2	-	2	
		Factory calibrated	TA= –40°C to 105°C	–2	-	2.5	%
			TA= –40°C to 85°C	–1.5	-	2.2	%
			TA = 0°C to 70°C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$Tsu_{(HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$I_{DD(HSI)}$	Oscillator power consumption	-		-	80	100	µA

4.2.8 LSI clock characteristics

Table 4-11 Characteristics of the LSI clock

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$tsu_{(LSI)}$	Oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$	Oscillator power consumption	-	0.65	1.2	µA

4.2.9 PLL characteristics

Table 4-12 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	1	8.0	25	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	96	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.10 Flash memory characteristics

Table 4-13 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-byte programming time	6	-	7.5	µs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
IDD_{PROG}	One-byte programming current	-	-	5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Read current@24 MHz	-	2	3	mA
	Read current@1 MHz	-	0.25	0.4	mA
N_{END}	Erasure endurance	1000	-	-	Cycles
t_{RET}	Data retention	20	-	-	Years
Vprog	Programming current	2.0	3.3	5.5	V

4.2.11 I/O static characteristics

Table 4-14 I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} > 2 V	0.42 × (V_{DD} – 2 V) + 1 V	-	5.5	V
		$V_{DD} \le$ 2 V			5.2	V
V_{IL}	Input low level voltage	-	–0.3	-	0.32 × (V_{DD} – 2 V) + 0.75 V	V
V_{hys}	Schmitt trigger voltage hysteresis	-	300 mV@5 V, 450 mV@3.3 V	-	-	mV
I_{lkg}	Input leakage current	V_{IN} = 5 V	-	-	3	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.12 I/O pin output alternating current characteristics

Table 4-15 I/O pin output alternating current characteristics

MODEy[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 5.5 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	ns
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 5.5 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	ns
11	$f_{max(IO)out}$	Max frequency	CL = 30 pF, V_{DD} = 2.7 V to 5.5 V	-	50	MHz
			CL = 50 pF, V_{DD} =2.7 V to 5.5 V	-	30	MHz
			CL = 50 pF, V_{DD} =2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	CL = 30 pF, V_{DD} = 2.7 V to 5.5 V	-	5	ns
			CL = 50 pF, V_{DD} =2.7 V to 5.5 V	-	8	ns
			CL = 50 pF, V_{DD} =2 V to 2.7 V	-	12	ns
	$tr_{(IO)out}$	Output low to high level rise time	CL = 30 pF, V_{DD} = 2.7 V to 5.5 V	-	5	ns
			CL = 50 pF, V_{DD} =2.7 V to 5.5 V	-	8	ns
			CL = 50 pF, V_{DD} =2 V to 2.7 V	-	12	ns

4.2.13 TIM characteristics

Table 4-16 TIM pin input characteristics

Symbol	Condition	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIMxCLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}/2^{(1)}$	MHz
RES_{TIM}	Timer resolution	-	16	bit
$T_{counter}$	16-bit counter clock period when an internal clock is selected	1	65536	$T_{TIMxCLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536 × 65536	$T_{TIMxCLK}$

(1). $f_{TIMxCLK}$ = 96/48 MHz

4.2.14 ADC characteristics

Table 4-17 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Reference input current	-	-	150	480	μA
INL	Integral non linearity (maximum difference between the actual conversion point and the end point correlation line)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration: V_{DDA} = 2.4 V to 3.6 V	-	±1.5	±4	LSB
DNL	Differential non linearity (maximum difference between the actual step and the ideal	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration:	-	±1	±3	LSB

Item	Description	Condition	Min	Typ	Max	Unit
	step)	V_{DDA} = 2.4 V to 3.6 V				
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} grounded)	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sample switch resistance	-	-	-	1	kΩ
C_{ADC}	Sample and hold capacitance	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}	Input trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (sampling time ts + 12.5 for successive approximation)			$1/f_{ADC}$
ADC bit width	12-bit (8 bits valid)	-	-			-

4.2.15 Temperature sensor characteristics

Table 4-18 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Avg_Slope	Average slope	-	2.9	3	3.1	mV/°C

5 Pinouts and pin descriptions

HK32F103x8xB MCUs are delivered in two packages: LQFP48 and LQFP64.

5.1 LQFP48

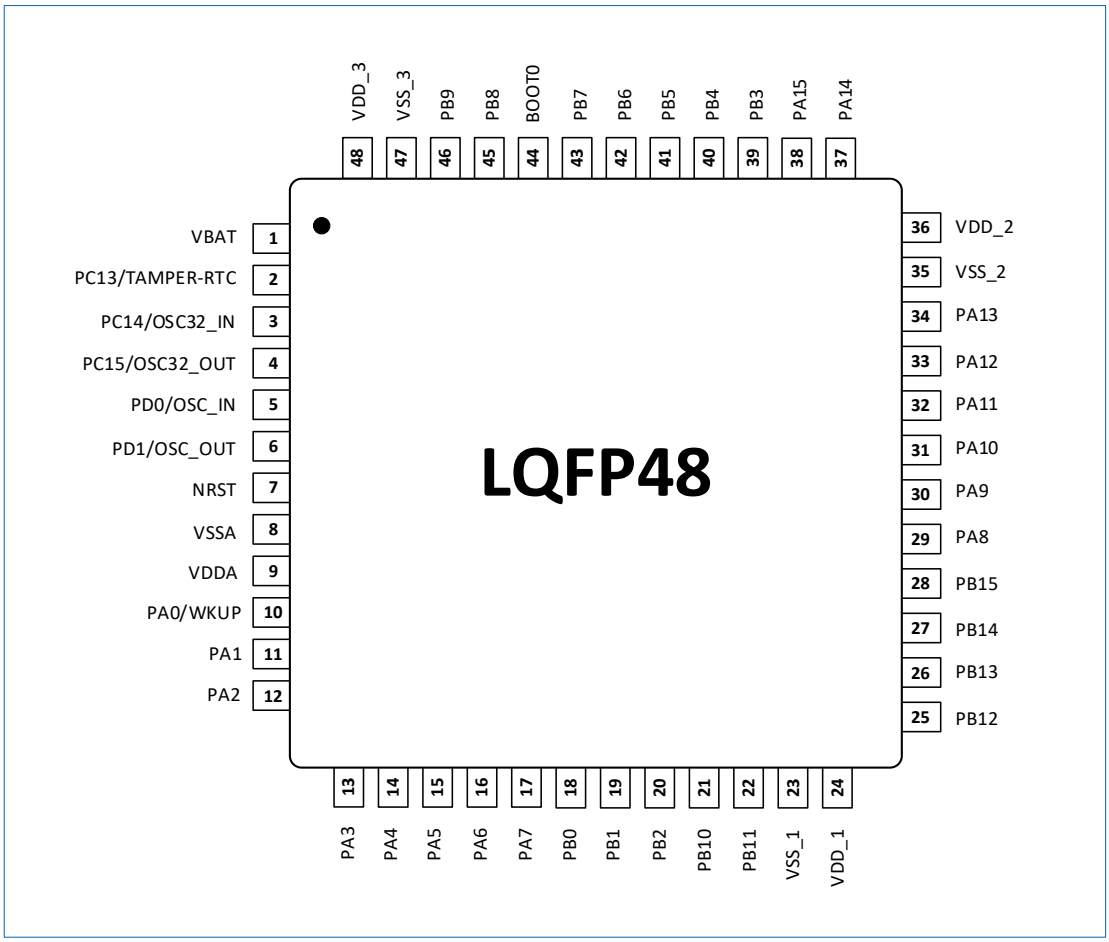

Figure 5-1 LQFP48 package pinout

5.2 LQFP64

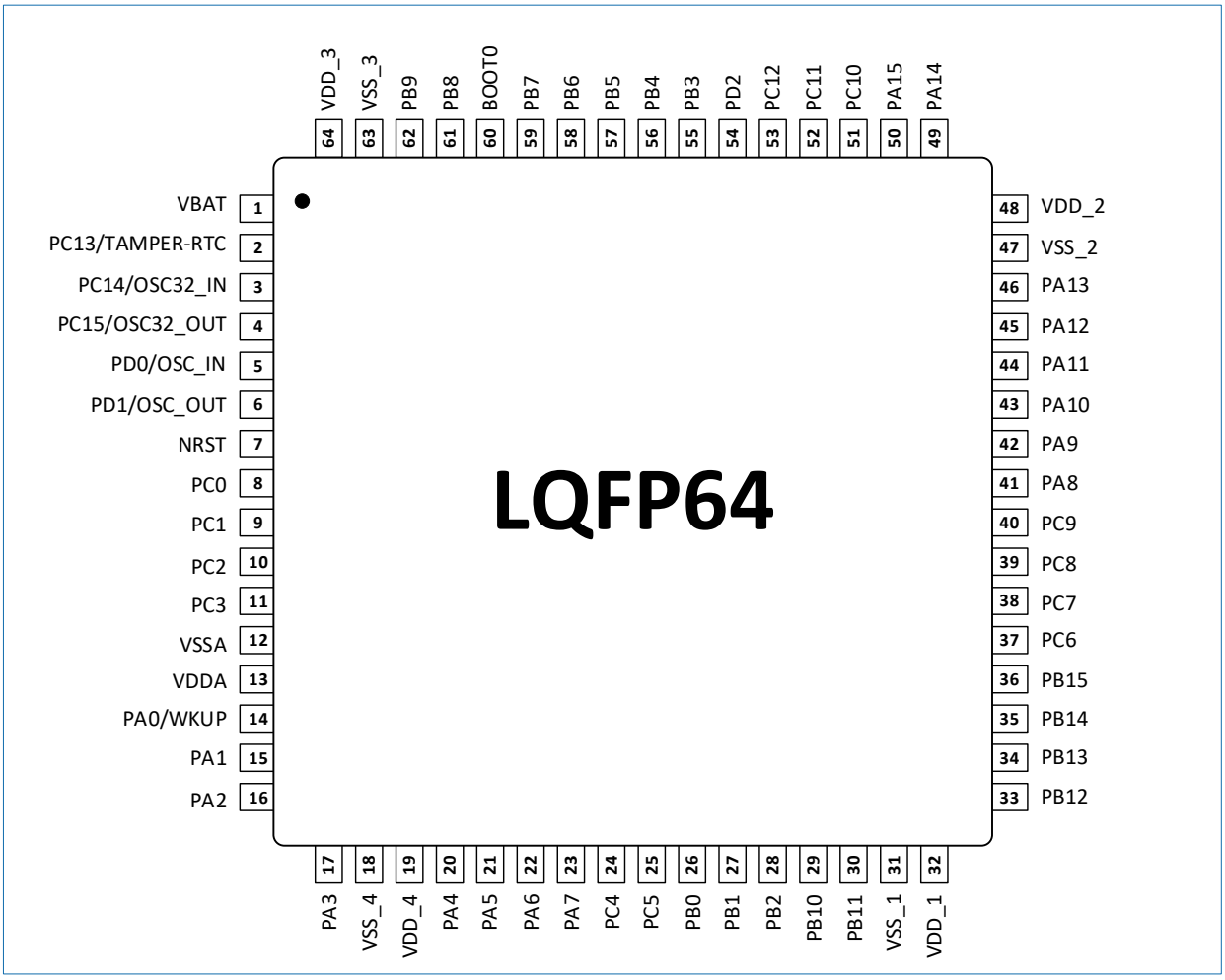

Figure 5-2 LQFP64 package pinout

5.3 LQFP48/LQFP64 pin descriptions

The following table shows pin descriptions of LQFP48 and LQFP64 packages.

Table 5-1 HK32F103x8xB pin descriptions

LQFP48	LQFP64	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
1	1	VBAT	S(1)	-	VBAT	-	-
2	2	PC13/TAMPER-RTC	I/O(1)	-	PC13	TAMPER-RTC/WKUP1/RTCO	TXEV/EXTIN13
3	3	PC14/OSC32_IN	I/O	-	PC14	OSC32_IN/LSE_CKI	TXEV/EXTIN14
4	4	PC15/OSC32_OUT	I/O	-	PC15	OSC32_OUT	TXEV/EXTIN15
5	5	PD0/OSC_IN	I	-	OSC_IN	OSC_IN/HSE_CKI	TXEV/PD0
6	6	PD1/OSC_OUT	O	-	OSC_OUT	OSC_OUT	TXEV/PD1
7	7	NRST	I/O	-	NRST	-	-
-	8	PC0	I/O	-	PC0	ADC12_IN10	TXEV/EXTIN0
-	9	PC1	I/O	-	PC1	ADC12_IN11	TXEV/EXTIN1
-	10	PC2	I/O	-	PC2	ADC12_IN12	TXEV/EXTIN2
-	11	PC3	I/O	-	PC3	ADC12_IN13	TXEV/EXTIN3
8	12	VSSA	S	-	VSSA	VREFN	-
9	13	VDDA	S	-	VDDA	VREFP	-

LQFP48	LQFP64	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
10	14	PA0/WKUP	I/O	-	PA0	WKUP0/USART2_CTS/ADC12_IN0/ TIM2_CH1_ETR/EXTIN0	TXEV
11	15	PA1	I/O	-	PA1	USART2_RTS/ADC12_IN1/ TIM2_CH2/EXTIN1	TXEV
12	16	PA2	I/O	-	PA2	USART2_TX/ADC12_IN2/ TIM2_CH3/EXTIN2	TXEV
13	17	PA3	I/O	-	PA3	USART2_RX/ADC12_IN3/ TIM2_CH4/EXTIN3	TXEV
-	18	VSS_4	S	-	VSS_4	-	-
-	19	VDD_4	S	-	VDD_4	-	-
14	20	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK/ ADC12_IN4/EXTIN4	TXEV
15	21	PA5	I/O	-	PA5	SPI1_SCK/ADC12_IN5/EXTIN5	TXEV
16	22	PA6	I/O	-	PA6	SPI1_MISO/ADC12_IN6/TIM3_CH1/EXTIN6	TXEV/TIM1_BKIN
17	23	PA7	I/O	-	PA7	SPI1_MOSI/ADC12_IN7/TIM3_CH2/EXTIN7	TXEV/TIM1_CH1N
-	24	PC4	I/O	-	PC4	ADC12_IN14	TXEV/EXTIN4
-	25	PC5	I/O	-	PC5	ADC12_IN15	TXEV/EXTIN5
18	26	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3	TXEV/TIM1_CH2N/EXTIN0
19	27	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4	TXEV/TIM1_CH3N/EXTIN1
20	28	PB2	I/O	FT	PB2	BOOT1(3)	TXEV/EXTIN2
21	29	PB10	I/O	-	PB10	I2C2_SCL/USART3_TX	TXEV/TIM2_CH3/EXTIN10
22	30	PB11	I/O	-	PB11	I2C2_SDA/USART3_RX	TXEV/TIM2_CH4/EXTIN11
23	31	VSS_1	S	-	VSS_1	-	-
24	32	VDD_1	S	-	VDD_1	-	-
25	33	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/USART3_CK/TIM1_BKIN	TXEV/EXTIN12
26	34	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N	TXEV/EXTIN13
27	35	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N/ USART3_RTS	TXEV/EXTIN14
28	36	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	TXEV/EXTIN15
-	37	PC6	I/O	FT	PC6	-	TXEV/TIM3_CH1/EXTIN6
-	38	PC7	I/O	FT	PC7	-	TXEV/TIM3_CH2/EXTIN7
-	39	PC8	I/O	FT	PC8	-	TXEV/TIM3_CH3/EXTIN8
-	40	PC9	I/O	FT	PC9	-	TXEV/TIM3_CH4/EXTIN9
29	41	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/RCC_MCO/EXTIN8	TXEV
30	42	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2/EXTIN9	TXEV
31	43	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3/EXTIN10	TXEV
32	44	PA11	I/O	FT	PA11	USART1_CTS/USB_DM/CAN1_RX/ TIM1_CH4/EXTIN11	TXEV
33	45	PA12	I/O	FT	PA12	USART1_RTS/USB_DP/CAN1_TX/ TIM1_ETR/EXTIN12	TXEV
34	46	PA13/JTMS-SWDIO	I/O	FT	JTMS-SWDIO	-	TXEV/PA13
35	47	VSS_2	S		VSS_2	-	-
36	48	VDD_2	S		VDD_2	-	-
37	49	PA14/JTCK-SWCLK	I/O	FT	JTCK-SWCLK	EXTIN14	TXEV/PA14

LQFP48	LQFP64	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
38	50	PA15/JTDI	I/O	FT	JTDI	EXTIN15	TXEV/PA15/TIM2_CH1_ETR/SPI1_NSS
-	51	PC10	I/O	-	PC10	-	TXEV/USART3_TX/EXTIN10
-	52	PC11	I/O	-	PC11	-	TXEV/USART3_RX/EXTIN11
-	53	PC12	I/O	-	PC12	-	TXEV/USART3_CK/EXTIN12
-	54	PD2	I/O	-	PD2	TIM3_ETR	TXEV/EXTIN2
39	55	PB3	I/O	-	JTDO	TRACESWO	TXEV/PB3/TIM2_CH2/SPI1_SCK/EXTIN3
40	56	PB4	I/O	-	NJTRST	-	TXEV/PB4/TIM3_CH1/SPI1_MISO/EXTIN4
41	57	PB5	I/O	-	PB5	I2C1_SMBA	TXEV/TIM3_CH2/SPI1_MOSI/EXTIN5
42	58	PB6	I/O	-	PB6	I2C1_SCL/TIM4_CH1	TXEV/USART1_TX/EXTIN6
43	59	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	TXEV/USART1_RX/EXTIN7
44	60	BOOT0(3)	I	-	BOOT0	-	-
45	61	PB8	I/O	-	PB8	TIM4_CH3	TXEV/I2C1_SCL/CAN1_RX/EXTIN8
46	62	PB9	I/O	-	PB9	TIM4_CH4	TXEV/I2C1_SDA/CAN1_TX/EXTIN9
-	-	PE0	I/O	FT	PE0	TIM4_ETR	TXEV/EXTIN0
-	-	PE1	I/O	FT	PE1	-	TXEV/EXTIN1
47	63	VSS_3	S	-	VSS_3	-	-
48	64	VDD_3	S	-	VDD_3	-	-

(1). I = input, O = output, I/O = input/output, S = supply.

(2). FT: 5 V tolerant.

(3). BOOT0/BOOT1 pin is connected to an internal weak pull-down resistor.

6 Packages

6.1 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

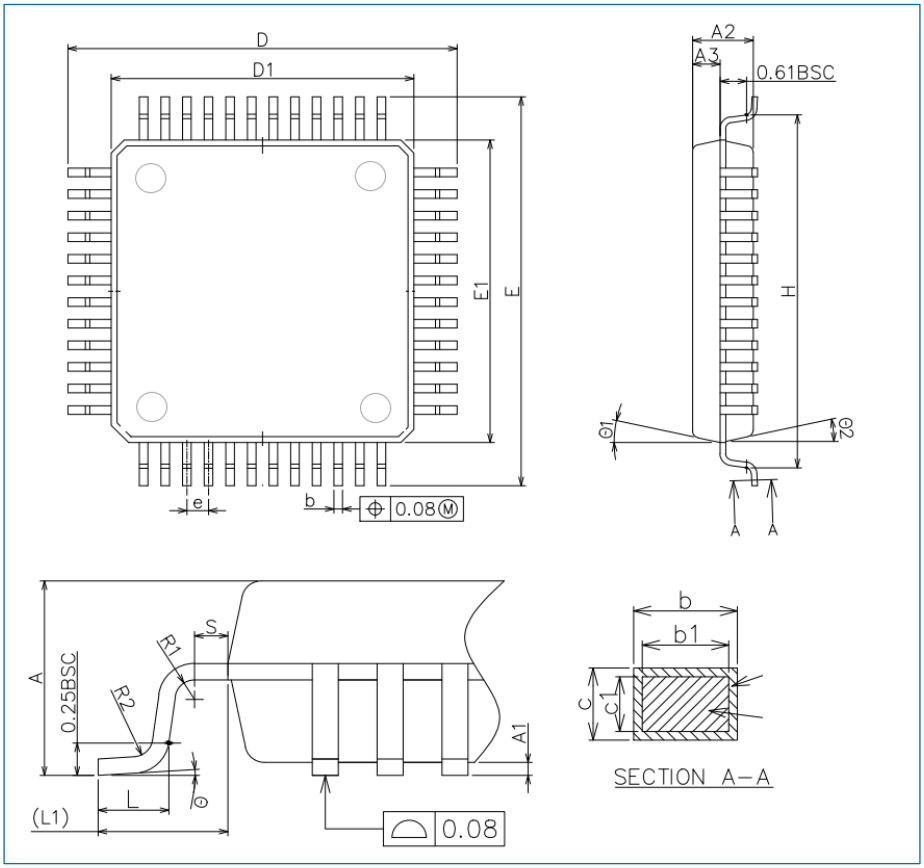

Figure 6-1 LQFP48 package outline

Table 6-1 LQFP48 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.063
A1	0.050	-	0.150	0.002	-	0.006
A2	1.280	1.360	1.450	0.050	0.054	0.057
A3	0.540	0.610	0.690	0.021	0.024	0.027
b	0.180	-	0.270	0.007	-	0.011
c	0.130	-	0.180	0.005	-	0.007
D	8.800	9.000	9.200	0.346	0.354	0.362
D1	6.900	7.000	7.100	0.272	0.276	0.280
E	8.800	9.000	9.200	0.346	0.354	0.362
E1	6.900	7.000	7.100	0.272	0.276	0.280
e	0.400	0.500	0.600	0.016	0.020	0.024
H	8.100	8.180	8.260	0.319	0.322	0.325
L	0.440	-	0.700	0.017	-	0.028
L1	1.00REF					
R1	0.080	-	-	0.003	-	-
R2	0.080	-	0.200	0.003	-	0.008
S	0.180	-	-	0.007	-	-
θ	0°	4°	8°	0°	4°	8°
Θ1	8°	12°	16°	8°	12°	16°
Θ2	8°	12°	16°	8°	12°	16°

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

6.2 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch package.

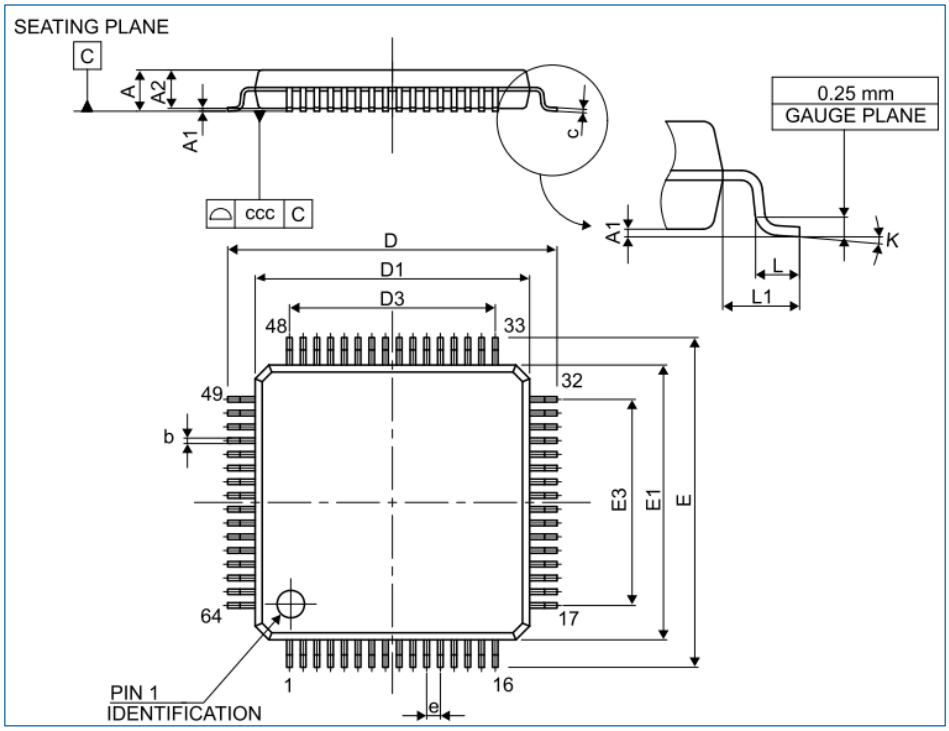

Figure 6-2 LQFP64 package outline

Table 6-2 LQFP64 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7 Ordering information

Table 7-1 HK32F103x8xB ordering information

Package	Part Number	Shipping Option	Remarks
LQFP48	HK32F103C8T6	Tape and reel/Tray	-
	HK32F103CBT6	Tape and reel/Tray	-
LQFP64	HK32F103R8T6	Tape and reel/Tray	-
	HK32F103RBT6	Tape and reel/Tray	-

8 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
FM	Fast Mode
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
IWDG	Independent Watchdog
LSB	Least Significant Bit
LSE	Low-Speed External (clock signal)
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PVD	Programmable Voltage Detector
PWM output	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTC	Real-time Clock
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

9 Legal and contact information

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