HK32F103x8xBT6A Datasheet

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Shenzhen Hangshun Chip Technology R&D Co., Ltd.

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F103x8xBT6A series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32F103x8xBT6A.

Audience

This document is intended for:

- HK32F103x8xBT6A developers
- HK32F103x8xBT6A testers
- HK32F103x8xBT6A users

Release Notes

This document is applicable to HK32F103x8xBT6A series MCUs.

Revision History

Version	Date	Description
1.0.0	2018/06/08	The initial release.
1.1.0	2019/10/22	Added section "3.27 DVSQ unit".
1.1.1	2020/06/19	Updated section "3.14 DMA".
1.1.2	2020/08/23	Updated section "3.9.1 Clock tree".
1.1.3	2021/01/26	Updated section "4.2.14 ADC characteristics".
1.1.4	2021/07/06	Updated section "3.2 Memory mapping".
1.1.5	2021/08/11	Added section "3.9 Reset".
1.2	2022/10/24	Deleted section "3.5 Coprocessor, and all related description".
1.3	2023/11/03	1. Updated the reliability test data in section "2.1 Features". 2. Updated section "2.2 Device overview". 3. Updated Figure 3-3 Reset signal. 4. Updated Table 3-4 Relationships between ADC channels and pins. 5. Added section "3.5 Cache". 6. Updated the PLL clock frequency (the same as in section "4.2.10 PLL characteristics") in section "3.10.1 Clock sources". 7. Updated section "3.10.2 Clock tree". 8. Updated the condition in section "4.2.5 Operating current characteristics". 9. Updated section "5.5 Pin descriptions". 10. Updated the package outline figure and data in section "6.1.1 QFN48". 11. Added the device marking and ordering information. 12. Added the HK32F103CET6A part number. 13. Added the HK32F103CCU6A QFN48 package. 14. Corrected trivial errors in the whole document.

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1 Introduction

This document is the datasheet for HK32F103x8xBT6A series MCUs. HK32F103x8xBT6A is a family of high-performance MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32F103CCU6A (QFN48 package)
- HK32F103CxT6A (LQFP48 package)
  - HK32F103C8T6A
  - HK32F103CBT6A
  - HK32F103CCT6A
  - HK32F103CET6A
- HK32F103RxT6A (LQFP64 package)
  - HK32F103R8T6A
  - HK32F103RBT6A
- HK32F103VxT6A (LQFP100 package)
  - HK32F103V8T6A
  - HK32F103VBT6A

For more details, see *HK32F103x8xBT6A User Manual*.

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2 Product overview

HK32F103x8xBT6A adopts the ARM® Cortex®-M3 core operating at a maximum frequency of 120 MHz.

HK32F103x8xBT6A embeds a 64/128/256/512-Kbyte Flash and a 20/64-Kbyte SRAM.

HK32F103x8xBT6A embeds an advanced timer and three general-purpose timers.

HK32F103x8xBT6A has the following communication interfaces: two SPI interfaces, two I2C interfaces, three USART interfaces, a USB 2.0 full-speed communication interface, a CAN bus interface, two 12-bit ADCs, and an internal temperature sensor.

With its diversified peripherals, HK32F103x8xBT6A is suitable for a wide range of applications:

- Industry applications, such as programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- CPU core
  - ARM® Cortex®-M3 core
  - Maximum frequency: 120 MHz
  - 24-bit SysTick timer
  - The CPU event signal can be input to the MCU pin to realize board-level communication with the CPU of other chips.
- Operating voltage range
  - Dual power domains
    - Main power supply V_{DD}: 2.0 V to 3.6 V
    - Backup power supply V_{BAT}: 1.8 V to 3.6 V
  - When the main power supply is powered off:
    - The RTC can be powered from $V_{BAT.}$
    - The 20-byte backup registers are available under V_{BAT}.
- Operating temperature range: –40°C to 105°C
- V_{DD} typical operating current
  - Run mode: 20.95 mA@120 MHz@3.3 V
  - Sleep mode: 14.63 mA@120 MHz@3.3 V
  - Stop mode:
    - LDO operating at full speed: 303 µA@3.3 V
    - LDO in the low-power state: 89.47 µA@3.3 V
  - Standby mode: 3.36 µA@3.3 V
- Memory

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- Up to 512 Kbytes of Flash
  - No wait states to access Flash when the CPU frequency is 24 MHz or lower
  - Separate read and write protection to protect code
- 20-Kbyte SRAM (64-Kbyte SRAM in HK32F103CET6A)

- DMA controller
  - 7-channel DMA controller
  - Can be triggered by multiple peripherals such as the timer, ADC, SPI, I2C, and USART
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): 56 MHz/28 MHz/8 MHz
  - Low-speed internal clock (kHz): 40 kHz
  - PLL output clock: 120 MHz (maximum value)
  - GPIO external input clock: 1 MHz to 64 MHz
- Reset
  - External pin reset
  - Power-on reset (POR)/Power-down reset (PDR)
  - Software reset
  - IWDG reset and WWDG reset
  - Low-power management reset
- GPIO
  - 80/51/37 GPIO pins in the 100/64/48-pin packages
  - Each GPIO can be used as an external interrupt input
  - Provide up to 20 mA drive current
- Encryption
  - CRC calculation unit
- Data communication interface
  - 3 x USARTs (support the ISO-7816 smart card standard)
  - 2 x SPIs
  - 2 × I2C
  - 1 × CAN 2.0A/2.0B
  - 1 × full-speed USB 2.0
- Timer
  - Advanced timer: TIM1 (Channels 1-3 support complementary PWM output with programmable inserted dead-times)
  - General-purpose timer: TIM2/TIM3/TIM4
- Clock-calendar function provided by RTC counter in cooperation with software
- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detecting voltage
  - Rising edge and falling edge detection configurable

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- On-chip analog circuitry
  - 2 × 12-bit SAR ADC
    - Support the automatic scan and scan conversion
    - Can be cascaded for master/slave parallel conversion and alternate conversion
  - 1 × temperature sensor
    - The analog output is connected to an independent ADC channel.
- Debug and trace port
  - Dual-wire SW-DP
  - Five-wire JTAG
  - Data Watchpoint and Trace (DWT) unit, Flash Patch and Breakpoint (FPB) unit, Instrumentation Trace Macrocell (ITM) unit, and Trace Port Interface Unit (TPIU) embedded
- Reliability
  - Passed HBM2000V/CDM500V/MM200V/LU200mA level tests.

2.2 Device overview

Table 2-1 HK32F103x8xBT6A features

Part Number		HK32F103 C8T6A	HK32F103 CBT6A	HK32F103 CCT6A	HK32F103 CET6A	HK32F103 CCU6A	HK32F103 R8T6A	HK32F103 RBT6A	HK32F103 V8T6A	HK32F103 VBT6A
CPU	Core	Cortex®-M3								
	Frequency (MHz)	120								
Memory	Flash (Kbyte)	64	128	256	512	256	64	128	64	128
	SRAM (Kbyte)	20	20	20	64	20	20	20	20	20
	Cache (Kbyte)	1								
DMA (Channels)		1 (7 channels)								
Timer	Advanced timer (16-bit)	1 (TIM1)								
	General-purpose timer (16-bit)	3 (TIM2/3/4)								
	SysTick timer	1								
	RTC	1								
	IWDG	1								
	WWDG	1								
Peripheral comm. interface	USART	3								
	I2C	2								
	SPI	2								
	CAN	1								
	USB	1								
CRC		1								
ADC	ADC	ADC1 (12) + ADC2 (10)					ADC1 (18) + ADC2 (16)			

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Part Number		HK32F103 C8T6A	HK32F103 CBT6A	HK32F103 CCT6A	HK32F103 CET6A	HK32F103 CCU6A	HK32F103 R8T6A	HK32F103 RBT6A	HK32F103 V8T6A	HK32F103 VBT6A
	(Channels)									
	Sampling rate	1 MSPS								
	Accuracy	12-bit								
Temperature sensor		1								
Programmable voltage detector (PVD)		1								
96-bit UID		1								
GPIO		37	37	37	37	37	37	51	80	80
Package		LQFP48	LQFP48	LQFP48	LQFP48	QFN48	LQFP64	LQFP64	LQFP100	LQFP100
Operating voltage		2.0 V – 3.6 V								
Backup power supply		1.8 V – 3.6 V								
Operating temperature		–40°C to 105°C								

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3 Function description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor that provides an MCU platform featuring low power consumption and high performance. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M3 core, the HK32F103x8xBT6A family is compatible with ARM tools and software.

The following figure shows the block diagram of HK32F103VBT6A:

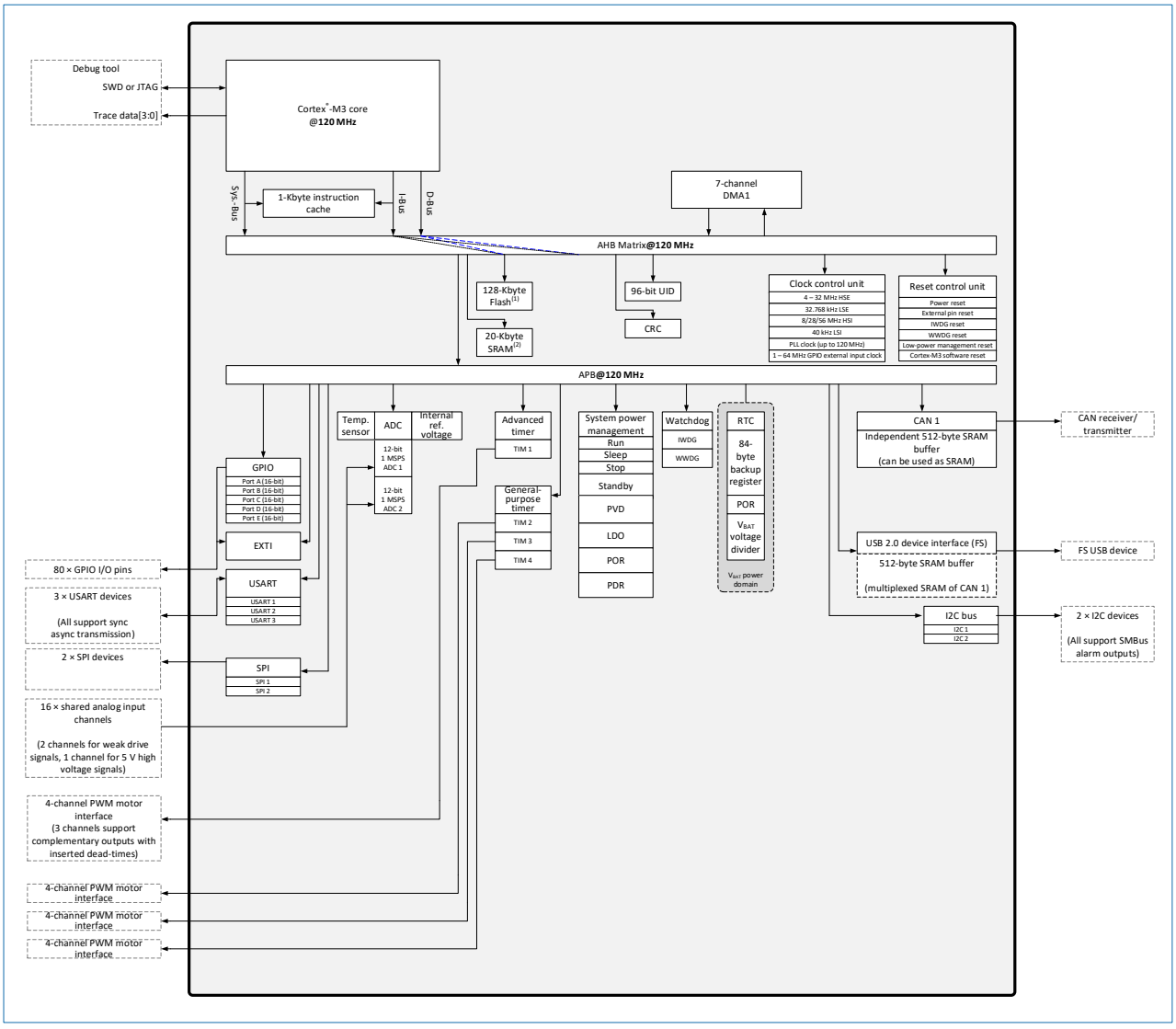

Figure 3-1 HK32F103VBT6A block diagram

Note:

(1). The maximum Flash size of HK32F103x8xBT6A can be 512 Kbytes (HK32F103CET6A).

(2). The maximum SRAM size of HK32F103x8xBT6A can be 64 Kbytes (HK32F103CET6A).

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3.2 Memory mapping

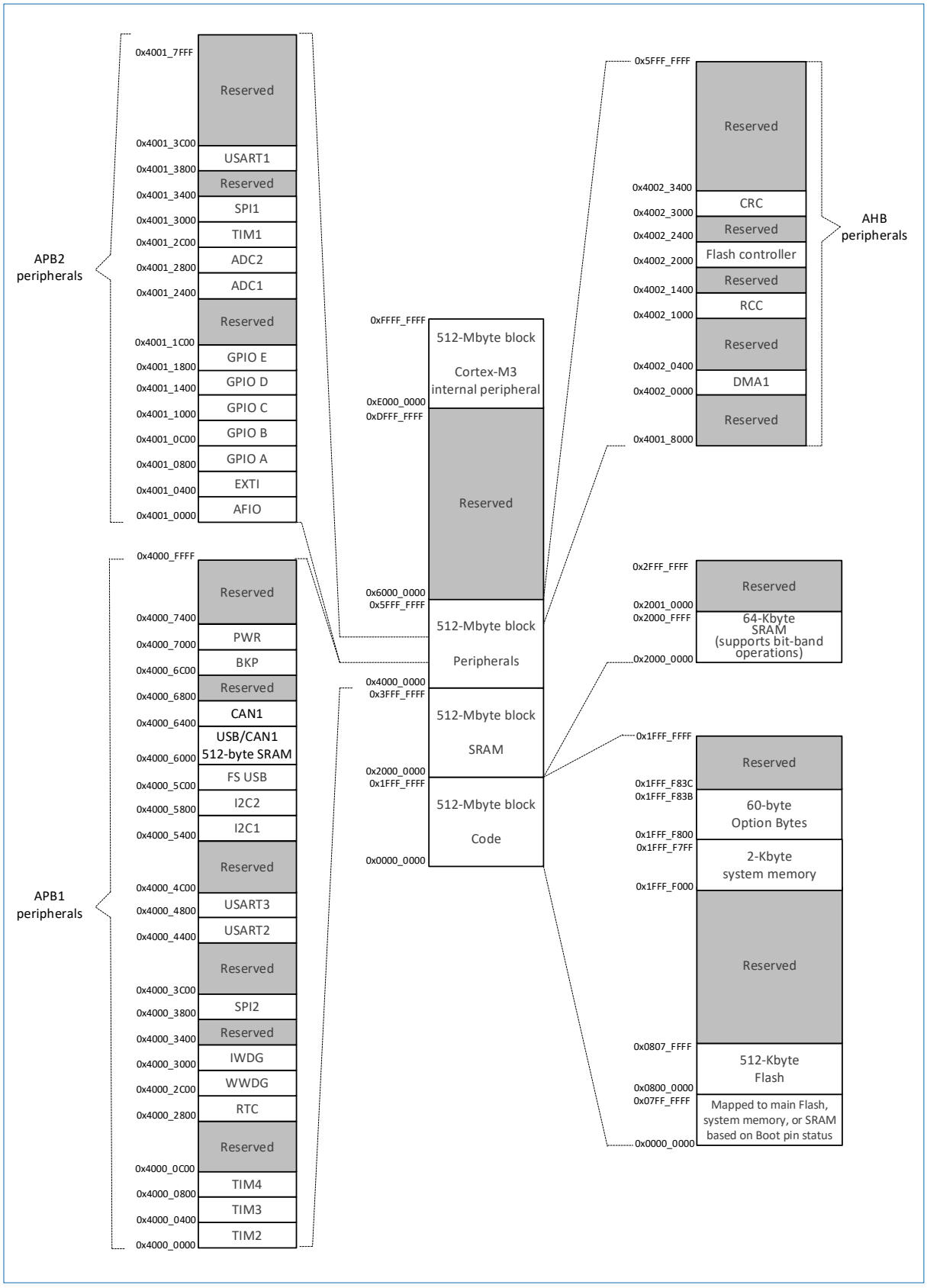

Figure 3-2 HK32F103x8xBT6A memory mapping

3.3 Flash

HK32F103x8xBT6A integrates a Flash memory of 512 Kbytes to store programs and data. The Flash supports about 100,000 cycles of erase and write operations.

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3.4 SRAM

HK32F103x8xBT6A integrates an up to 64-Kbyte SRAM. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.5 Cache

The device integrates 1 Kbyte of high-speed cache for storing instructions.

- 8-way set associative
- The least recently used (LRU) strategy is adopted.
- The embedded counter counts the hit rate of instructions stored in the cache.
- The cache control register can be configured to cache instructions of specific types. The instructions fetched by I-Bus from internal Flash can be stored in the cache.

3.6 CRC calculation unit

Cyclic redundancy check (CRC) is used to verify data integrity during transmission and storage. HK32F103x8xBT6A integrates a CRC calculation unit to reduce the application processing burden and accelerate processing.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with a reference signature, which is generated at link time and stored at a specified memory location.

3.7 NVIC

HK32F103x8xBT6A incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 43 maskable interrupt channels (excluding 16 Cortex®-M3 interrupt lines) and 16 interrupt priorities while maintaining the lowest interrupt latency.

- The closely coupled NVIC ensures low latency in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

3.8 EXTI

The extended interrupt/event controller (EXTI) is comprised of 19 edge detectors that are used to generate interrupt/event requests. The trigger event of each EXTI line can be independently configured to a rising edge, a falling edge, or both. Each EXTI line can be masked independently. The EXTI has a pending register that stores the status of each interrupt request.

3.9 Resets

HK32F103x8xBT6A supports the system reset, power reset, and backup domain reset.

3.9.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain. A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)

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- Independent watchdog counting terminates (IWDG reset)
- Power reset
- Software reset (SW reset)
- Low-power management reset

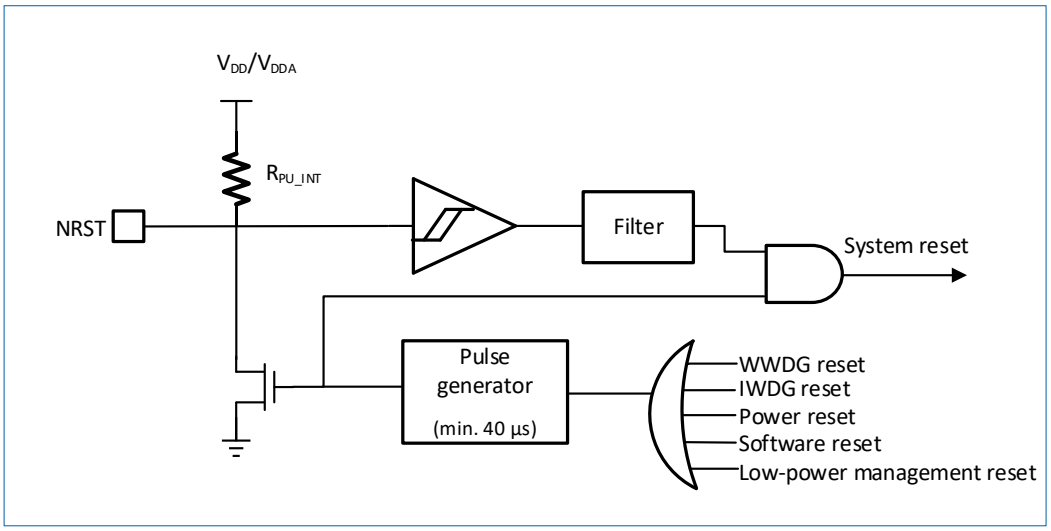

Figure 3-3 Reset signal

The internal reset signal is output on the NRST pin. The pulse generator guarantees a pulse duration of at least 40 µs for each internal or external reset source. When the NRST pin is pulled low and an external reset is generated, a reset pulse is generated.

You can identify a reset source by checking reset status flags in the RCC_CSR register.

Table 3-1 Reset setting

Reset Type	Configuration
Software reset	The SYSRESETREQ bit in Cortex®-M3 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
Low-power management reset	Generating a low-power management reset when entering the Standby mode: Set the nRST_STDBY bit in the option byte to 0 to generate the low-power management reset. Then, even if the system is in the process of entering the Standby mode, it will be reset instead of entering the Standby mode.
	Generating a low-power management reset when entering the Stop mode: Set the nRST_STOP bit in the option byte to 0 to generate the low-power management reset. Then, even if the system is in the process of entering the Stop mode, it will be reset instead of entering the Stop mode.

3.9.2 Power reset

The power reset resets all registers, except for the registers in the backup domain. The reset sources finally act on the reset pin. The reset pin keeps the low level during resets. The reset entry vector is fixed on address 0x0000_0004.

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Exit from Standby mode

HK32F103x8xBT6A embeds the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply is over the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuit is required.

3.9.3 Backup domain reset

The backup domain has two dedicated resets, which only affect the backup domain. A backup domain reset is generated when one of the following events occurs:

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- The BDRST bit in the RCC_BDCR register is set. (This also triggers the software reset.)
- V_{DD} or V_{BAT} is powered on after being powered off.

3.10 Clocks

A system clock is selected when the system starts. When a reset occurs, the 8 MHz HSI is selected as the system clock by default. When a failure of the 8 MHz HSI is detected, the 4 – 32 MHz HSE can be selected as the system clock. When a failure of the HSE is detected, the system switches to the internal RC oscillator. If the software interrupt is enabled, a software interrupt is generated. The full interrupt management of the PLL clock can be used as needed (for example, when the external oscillator fails.)

HK32F103x8xBT6A also provides LSI, LSE, and GPIO input as clock sources for the low-power and low-cost design scheme.

HK32F103x8xBT6A integrates the clock security system (CSS) circuit. The threshold for the detection of HSE frequency is adjustable.

3.10.1 Clock sources

Table 3-2 Clock sources

Clock	Clock Source
HSI clock	Output frequency: 56 MHz, which can be divided into 28 MHz or 8 MHz Accuracy: full temperature range ± 2%
HSE clock	Frequency: 4 MHz to 32 MHz Clock up to 64 MHz can be input from the OSC_IN pin
PLL clock	Input frequency: 2 MHz to 80 MHz Output frequency: 16 MHz to 120 MHz
LSI clock	Frequency: 30 kHz to 60 kHz. Typical value: 40 kHz
LSE clock	Frequency: 32.768 kHz Clock can be input from the OSC32_IN pin
GPIO input clock	PA1, PB1, PC7, PB7: up to 64 MHz

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3.10.2 Clock tree

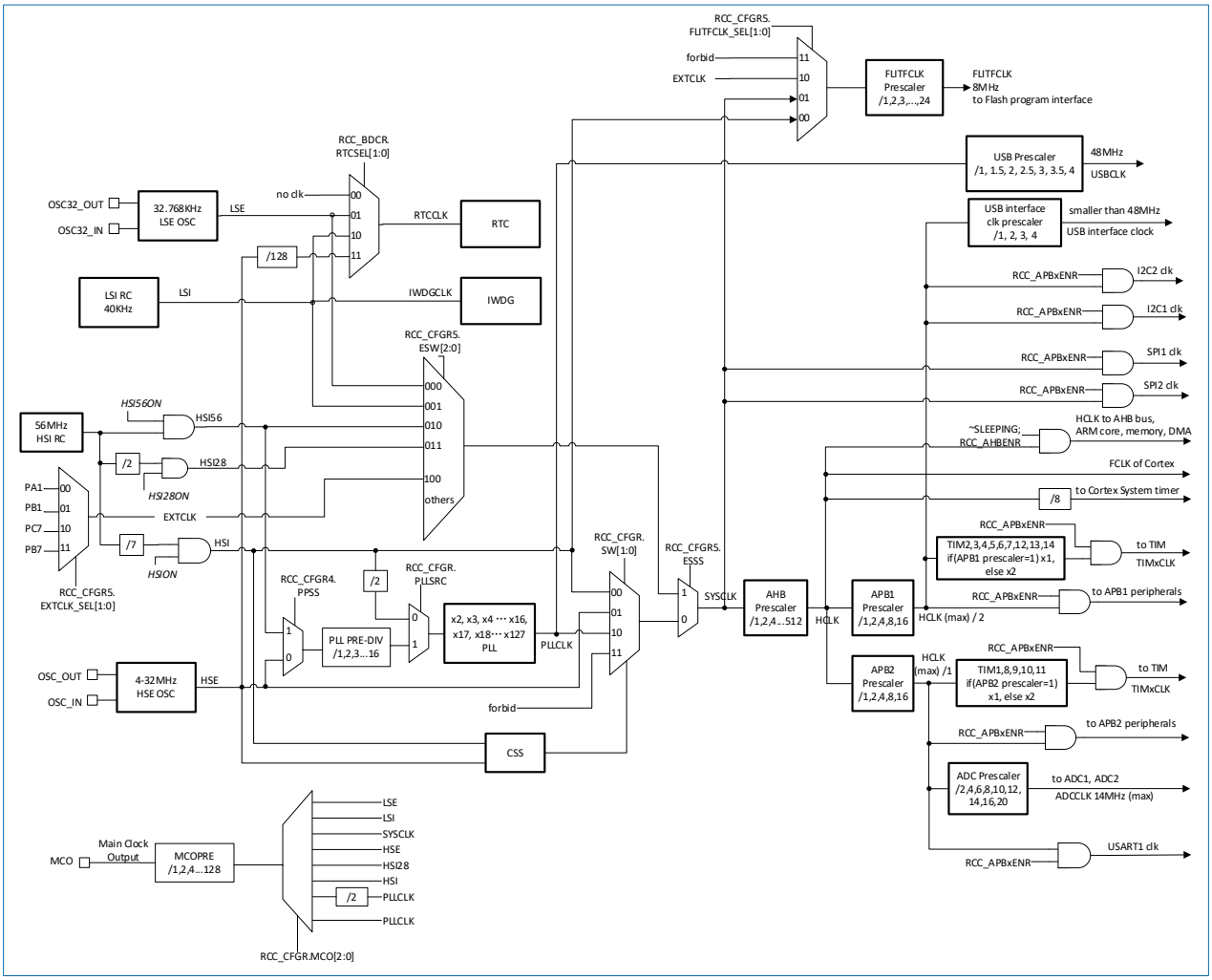

Figure 3-4 Clock tree

Note:

- PLL input clock: HSI8M/2, HSI56M/PREDIV, and HSE/PREDIV are available.
- SYSCLK: HSI8M, HSI28M, HSI56M, HSE, PLL, LSI, LSE, and GPIO input clock are available. HSI8M is the default clock.
- FLITFCLK: HSI8M, GPIO input clock, and SYSCLK clock are available.

3.11 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the USART1 interface.

3.12 Power supply scheme

- V_{DD} = 2.0 V to 3.6 V. V_{DD} supplies power to I/O pins and internal low dropout regulators (LDOs).
- V_{DDA} = 2.0 V to 3.6V. V_{DDA} supplies power to the analog circuitry, including the ADC and temperature sensor.
- V_{BAT} = 1.8 V to 3.6 V. When V_{DD} is powered off, V_{BAT} supplies power to the RTC, external 32.768 kHz oscillator,

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and backup registers.

3.13 PVD

HK32F103x8xBT6A integrates a programmable voltage detector (PVD). The PVD monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated. The interrupt program may send a warning message or set the MCU to the safe state. The PVD is enabled by setting the register.

3.14 Low-power modes

HK32F103x8xBT6A supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the PLL, HSI oscillator, and HSE oscillator are disabled.

  MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any of the 16 external I/O pins, a PVD output, or an RTC alarm.

- Standby mode

  In Standby mode, MCUs achieve the lowest power consumption. The internal LDO is disabled. The PLL, HSE oscillator, and HSI oscillator are also disabled. In Standby mode, the SRAM content and register content are lost, except for registers in the backup domain. The Standby circuitry works as normal.

  MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: For more information about the power consumption of different low-power modes, see Table 4-8.

3.15 DMA

The general-purpose direct memory access (DMA) controller (with seven channels) manages the data transfer from memories to memories, from peripherals to memories, and from memories to peripherals. The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by software. The length, source, and destination of data to be transferred can be independently set by using software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, and ADC.

3.16 RTC and BKP

The power supply to RTC and backup registers is controlled by a switch. When V_{DD} is enabled, V_{DD} supplies power to RTC and backup registers. Otherwise, V_{BAT} supplies power to RTC and backup registers.

3.16.1 RTC

The real-time clock (RTC) has a set of continuously running counters and can provide the clock calendar function via software. In addition, the real-time clock provides alarm interrupt and periodic interrupt functions.

The 32.768 kHz external oscillator or an internal low-power RC oscillator can drive RTC. The typical frequency of the internal RC oscillator is 40 kHz. An external 512 Hz signal is used for the compensation of natural quartz deviation. The RTC has a 32-bit programmable counter for long-term measurement in conjunction with the compare register. The RTC has a 20-bit prescaler which is used to generate the time base clock. When the RTC is clocked by the 32.768 kHz crystal oscillator (LSE), a 1-second time base is generated.

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3.16.2 BKP

Backup registers (BKP) are used to store user application data. The system reset and power reset do not reset backup registers. Backup registers are not reset upon wakeup from Standby mode.

3.17 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked from an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. IWDG can be configured as a software or hardware watchdog through the option bytes. In debug mode, the counter can be frozen.

3.18 WWDG

The window watchdog (WWDG) is based on a 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.19 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter and has the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.20 Timers

3.20.1 General-purpose timer

Every general-purpose timer (TIM2/TIM3/TIM4) provides a 16-bit auto-reload up/down counter, a 16-bit prescaler, and four independent channels. Every channel can be used for input capture, output compare, PWM output, and one-pulse mode output. The general-purpose timers can work with the advanced timer through the Timer Link feature for synchronization and event chaining. In debug mode, the counter can be frozen.

Every general-purpose timer can generate PWM outputs and has an independent DMA request mechanism.

3.20.2 Advanced timer

HK32F103x8xBT6A integrates the advanced timer TIM1. TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a standard 16-bit timer, it has the same functions as general-purpose TIMx. If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0-100%). In debug mode, the counter can be frozen. Many functions of the advanced timer are the same as those of general-purpose timers, and the two types of timers have the same structure. Therefore, the advanced timer can work

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together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

3.21 I2C bus

HK32F103x8xBT6A has two I2C bus interfaces. The I2C bus interfaces can work as a master or slave and support the standard and fast modes. The I2C interfaces support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interfaces have embedded hardware CRC generation/verification. They can be operated by using the DMA controller and support SMBus V2.0/PMBus.

3.22 USART

HK32F103x8xBT6A embeds three universal synchronous/asynchronous receivers/transmitters (USART1/USART2/USART3). These interfaces support asynchronous communication, IrDA SIR ENDEC, multi-processor communication, single-wire half-duplex communication, and LIN Master/Slave capability.

The USART1 interface communicates at a speed of up to 4.5 Mbit/s. The USART2 and USART3 interfaces communicate at a speed of up to 2.25 Mbit/s. All the USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (compliant with ISO 7816), and SPI-like communication mode.

3.23 SPI

HK32F103x8xBT6A has two serial peripheral interfaces (SPIs). In master or slave mode, the full-duplex and half-duplex communication speed is up to 18 Mbit/s. The 3-bit prescaler provides eight master mode frequencies. Each frame can be configured to 8-bit or 16-bit. The hardware CRC generation/verification supports the basic SD card and MMC mode.

The two SPI interfaces support the I2S function.

All SPI interfaces can be operated by using the DMA controller.

3.24 CAN

HK32F103x8xBT6A has a controller area network (CAN) interface. The CAN interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN interface has three transmit mailboxes and two 3-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.25 USB

HK32F103x8xBT6A embeds a USB controller that complies with the full-speed USB device standard. The USB interface endpoint settings can be configured by using the software. It provides suspend/resume support. The dedicated 48 MHz clock for USB is generated by the internal main PLL.

3.26 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.27 ADC

HK32F103x8xBT6A has two 12-bit analog-to-digital converters (ADCs): ADC1 and ADC2. They can perform conversions in single or scan mode. Every ADC can use up to 16 external channels. In scan mode, the conversion is automatically performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface include:

- Simultaneous sample and hold
- Interleaved sample and hold

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- Single sample

The ADC can be operated by using the DMA controller.

The analog watchdog feature provides precise voltage monitoring of one, some, or all selected channels. When the monitored voltage exceeds the preset threshold, an interrupt is generated. The events generated by the general-purpose timers and advanced timer can be internally connected to the ADC start trigger events and injection trigger events respectively. The application program then synchronizes the A/D conversion with timers.

Table 3-3 Relationships between ADC channels and pins

External Channel	External Pin	ADC1 Channel	ADC2 Channel
Channel 0	PA0	ADC1_IN0	ADC2_IN0
Channel 1	PA1	ADC1_IN1	ADC2_IN1
Channel 2	PA2	ADC1_IN2	ADC2_IN2
Channel 3	PA3	ADC1_IN3	ADC2_IN3
Channel 4	PA4	ADC1_IN4	ADC2_IN4
Channel 5	PA5	ADC1_IN5	ADC2_IN5
Channel 6	PA6	ADC1_IN6	ADC2_IN6
Channel 7	PA7	ADC1_IN7	ADC2_IN7
Channel 8	PB0	ADC1_IN8	ADC2_IN8
Channel 9	PB1	ADC1_IN9	ADC2_IN9
Channel 10	PC0	ADC1_IN10(1)	ADC2_IN10(1)
Channel 11	PC1	ADC1_IN11(1)	ADC2_IN11(1)
Channel 12	PC2	ADC1_IN12(1)	ADC2_IN12(1)
Channel 13	PC3	ADC1_IN13(1)	ADC2_IN13(1)
Channel 14	PC4	ADC1_IN14(1)	ADC2_IN14(1)
Channel 15	PC5	ADC1_IN15(1)	ADC2_IN15(1)
-	-	ADC1_IN16 (Internal channel: connected to the temperature sensor)	-
-	-	ADC1_IN17 (Internal channel: connected to the internal power supply module VREFINT)	-

(3). In the LQFP48 package, ADC1 and ADC2 do not provide channels 10 to 15.

3.28 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.29 Debug and trace port

HK32F103x8xBT6A embeds the ARM SWJ-DP which is a combined JTAG-DP and SW-DP that enables you to connect either a serial wire debug (SWD) or JTAG probe to a target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively. A specific signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}–V_{SS}	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	3.63	V
V_{IN}	Input voltage on pins	V_{SS} – 0.3	V_{DD}	V
$\|\Delta V_{DDx}\|$	Variation between different power pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	mA
I_{IO}	Output current sunk by any I/O and control pin	25	mA
	Output current sourced by any I/O and control pin	–25	mA
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	mA
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	mA

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of the positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to +150	°C
T_J	Maximum junction temperature	+125	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	60	MHz
f_{PCLK2}	Internal APB2 clock frequency	0	120	MHz
V_{DD}	Standard operating voltage	2	3.6	V

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Symbol	Description	Min	Max	Unit
V_{DDA}(1)	Analog operating voltage	2	3.6	V
V_{BAT}	Backup domain operating voltage	1.8	3.6	V
T	Operating temperature	–40	+105	°C

(1). It is recommended that you use the same power supply for V_{DD} and V_{DDA}.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0] = 000	2.183	2.188	2.196	V
		PLS[2:0] = 001	2.286	2.289	2.298	V
		PLS[2:0] = 010	2.393	2.399	2.407	V
		PLS[2:0] = 011	2.502	2.508	2.518	V
		PLS[2:0] = 100	2.621	2.629	2.639	V
		PLS[2:0] = 101	2.726	2.733	2.745	V
		PLS[2:0] = 110	2.839	2.846	2.855	V
		PLS[2:0] = 111	2.958	2.969	2.979	V
	Programmable voltage detector level selection (falling edge)	PLS[2:0] = 000	2.116	2.119	2.125	V
		PLS[2:0] = 001	2.208	2.211	2.220	V
		PLS[2:0] = 010	2.305	2.310	2.320	V
		PLS[2:0] = 011	2.399	2.406	2.416	V
		PLS[2:0] = 100	2.506	2.512	2.521	V
		PLS[2:0] = 101	2.596	2.602	2.613	V
		PLS[2:0] = 110	2.693	2.701	2.710	V
		PLS[2:0] = 111	2.798	2.805	2.817	V

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge(2)	1.8	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset duration	-	1.50	2.50	4.50	ms

(1). PDR is based on the monitoring of V_{DD} and V_{DDA}. POR is based on the monitoring of only V_{DD}.

(2). The actual performance value is guaranteed to be smaller than the minimum $V_{POR/PDR}$ value.

(3). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	0.74	0.8	0.811	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition	V_{DD} = 3.3 V				Unit
		–40°C	25°C	85°C	105°C	
Run mode	CPU operating at 120 MHz; Cache **enabled**; APB clock **enabled**, using the 120 MHz clock; Four wait states to access Flash.	12.18	20.95	22.31	23.44	mA
	CPU operating at 120 MHz; Cache **disabled**; APB clock **enabled**, using the 120 MHz clock; Four wait states to access Flash.	11.2	19.34	20.71	21.82	mA
	CPU operating at 120 MHz; Cache **enabled**; APB clock **disabled**, using the 120 MHz clock;	6.71	11.50	12.74	13.81	mA

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Mode	Condition	V_{DD} = 3.3 V				Unit
		–40°C	25°C	85°C	105°C	
	Four wait states to access Flash.					
	CPU operating at 120 MHz; Cache **disabled**; APB clock **disabled**, using the 120 MHz clock; Four wait states to access Flash.	6.1	10.44	11.66	12.75	mA
	CPU operating at 8 MHz; Cache **enabled**; APB clock **enabled**, using the 8 MHz HSE; Zero wait states to access Flash.	1.83	1.98	3.08	4.1	mA
	CPU operating at 8 MHz; Cache **disabled**; APB clock **enabled**, using the 8 MHz HSE; Zero wait states to access Flash.	3.65	3.91	5.06	6.12	mA
	CPU operating at 8 MHz; Cache **enabled**; APB clock **disabled**, using the 8 MHz HSE; Zero wait states to access Flash.	1.19	1.36	2.39	3.41	mA
	CPU operating at 8 MHz; Cache **disabled**; APB clock **disabled**, using the 8 MHz HSE; Zero wait states to access Flash.	1.15	1.25	2.32	3.36	mA
	CPU operating at 40 kHz; APB clock **enabled**, using the 40 kHz LSI.	0.23	0.31	1.34	2.33	mA
	CPU operating at 32.768 kHz; APB clock **enabled**, using the 32.768 kHz LSE.	0.23	0.3	1.35	2.32	mA
Sleep mode	CPU paused; APB clock **enabled**, using the 120 MHz clock.	8.52	14.63	15.92	17.01	mA
	CPU paused; APB clock **disabled**, using the 120 MHz clock.	3.3	5.65	6.82	7.85	mA
	CPU paused; APB clock **enabled**, using the 8 MHz HSI.	1.56	1.69	2.95	3.72	mA
	CPU paused; APB clock **disabled**, using the 8 MHz HSI.	0.88	1.01	2.85	3.04	mA
Stop mode	CPU paused; LDO **operating at full speed**; HSE/HSI/LSE disabled; IWDG disabled.	202.67	303	1322	2179	µA
	CPU paused; LDO in the **low-power state**; HSE/HSI/LSE disabled; IWDG disabled.	18.38	89.47	729	1374	µA
Standby mode	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; Only the Standby circuitry works as normal; LSI oscillator **enabled**; IWDG **enabled**.	2.98	3.87	16.74	30.29	µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; Only the Standby circuitry works as normal; LSI oscillator **disabled**; IWDG **disabled**.	2.96	3.87	16.68	30.22	µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; Only the Standby circuitry works as normal; HSE, HSI, LSE, LSI **disabled.**	2.35	3.36	16.16	29.72	µA

4.2.6 HSE clock characteristics

HK32F103x8xBT6A integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

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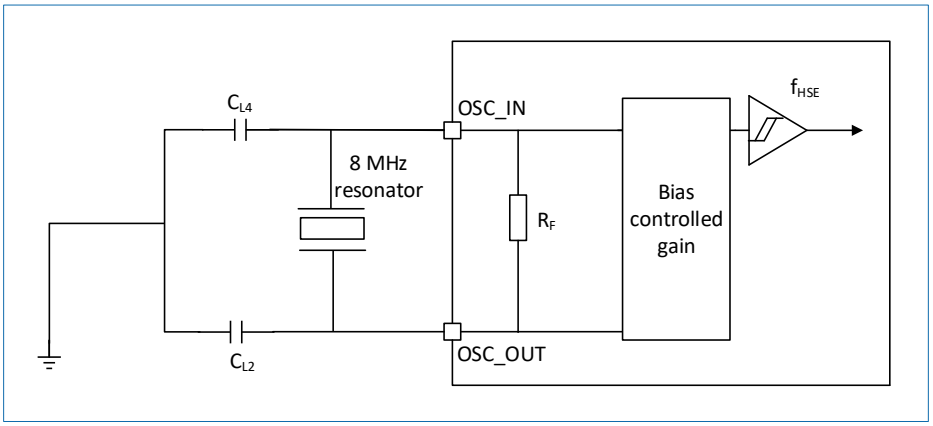

Figure 4-1 Recommended oscillator circuit outside the chip

Table 4-9 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	Frequency	-	1	8	25	MHz
V_{HSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$T_{w(HSE)}$	Effective high/low level duration		5	-	-	ns
$T_{r(HSE)}$ $T_{f(HSE)}$	Rise/Fall time		-	-	20	
$Cin_{(HSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.7 LSE clock characteristics

HK32F103x8xBT6A integrates an LSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

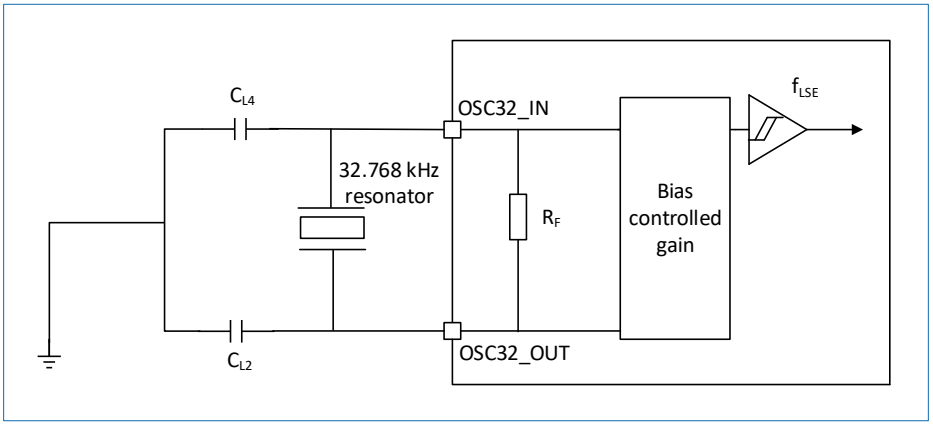

Figure 4-2 Recommended oscillator circuit outside the chip

Alternatively, an LSE signal can be directly input from the OSC32_IN pin. The following table lists the requirements for this clock signal.

Table 4-10 LSE clock characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	2		MΩ
$T_{su\ (LSE)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	2000	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12.5	-	pF
g_m	Oscillator transconductance	Started	-	-	-	
i_2	LSE driving current	-	-	400	-	nA

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Table 4-11 Characteristics of the input LSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{LSE_ext}	Frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$Tw_{(LSE)}$	Effective high/low level duration		450	-	-	ns
$Tr_{(LSE)}$/$Tf_{(LSE)}$	Rise/Fall time		-	-	50	ns
$Cin_{(LSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.8 HSI clock characteristics

Table 4-12 Characteristics of the HSI clock

Symbol	Parameter	Condition		Min	Typ	Max	Unit
F_{HSI} RC 56	RC oscillator	-		-	56	-	MHz
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Oscillator accuracy	Factory trimmed accuracy (ambient temperature)		–1	-	1	
		Factory calibrated	TA= –40°C to +105°C	-	-	2.5	%
			TA= –40°C to +85°C	-	-	2.2	%
			TA = 0°C to +70°C	-	-	2	%
			T_A = +25 °C	-	-	1.8	%
$T_{su(HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$I_{DD(HSI)}$	Oscillator power consumption	-		-	80	100	µA

4.2.9 LSI clock characteristics

Table 4-13 Characteristics of the LSI clock

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$	Oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$	Oscillator power consumption	-	0.65	1.2	µA

4.2.10 PLL characteristics

Table 4-14 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	8.0	80	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	120	MHz
t_{LOCK}	PLL lock time	-	80	200	µs
Jitter	Cycle-to-cycle jitter	-	5	13	ps

4.2.11 GPIO input clock

Clocks can be input from PA1, PB1, PC7, and PB7 of HK32F103x8xBT6A.

Table 4-15 GPIO input clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{ext}	Input clock frequency	1	8	64	MHz
	Input clock duty cycle	40	-	60	%

4.2.12 Flash memory characteristics

Table 4-16 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-byte programming time	6	-	7.5	µs

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Symbol	Parameter	Min	Typ	Max	Unit
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
IDD_{PROG}	One-byte programming current	-	-	5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Read current@24 MHz	-	2	3	mA
	Read current@1 MHz	-	0.25	0.4	mA
N_{END}	Erasure endurance	100,000	-	-	Cycles
t_{RET}	Data retention	20	-	-	Years
V_{PROG}	Programming current	1.8	3.3	3.6	V

4.2.13 I/O pin input characteristics

Table 4-17 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	1.6	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.5	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	1.56	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.26	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	300	-	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V 0 < V_{IN} < 3.3 V	-	-	1	μA
		V_{DD} = 3.3 V V_{IN} = 5 V	-	-	1	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	35	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	35	-	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.14 I/O pin output characteristics

Table 4-18 I/O pin output direct current characteristics

Mode[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Output high level voltage		-	125	ns
01	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Output high level voltage		-	125	ns
11	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	MHz
	V_{OH}	Output high level voltage		-	125	ns

Table 4-19 I/O pin output alternating current characteristics

Mode[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	5	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	5	ns

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4.2.15 TIM timer characteristics

Table 4-20 TIM characteristics

Symbol	Condition	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIMxCLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2$(1)	MHz
RES_{TIM}	Timer resolution	-	16	bit
$T_{counter}$	16-bit counter clock period when an internal clock is selected	1	65536	$T_{TIMxCLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536 × 65536	$T_{TIMxCLK}$

(1). $F_{TIMxCLK}$ = 60 MHz or 120 MHz

4.2.16 ADC characteristics

Table 4-21 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Reference input current	-	-	150	480	µA
INL	Integral non linearity (maximum difference between the actual conversion point and the end point correlation line)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1.5	±4	LSB
DNL	Differential non linearity (maximum difference between the actual step and the ideal step)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1	±3	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} grounded)	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sample switch resistance	-	-	-	1	kΩ
C_{ADC}	Sample and hold capacitance	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}	Input trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
			-	-	3	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
			-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
			14 to 252 (sampling time ts + 12.5 for successive approximation)			$1/f_{ADC}$

4.2.17 Temperature sensor characteristics

Table 4-22 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Avg_Slope	Average slope	-	2.9	3	3.1	mV/°C

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5 Pinouts and pin descriptions

This section describes the pinout and pin description of HK32F103x8xBT6A. HK32F103x8xBT6A are delivered in QFN48, LQFP48, LQFP64, and LQFP100 packages.

5.1 QFN48

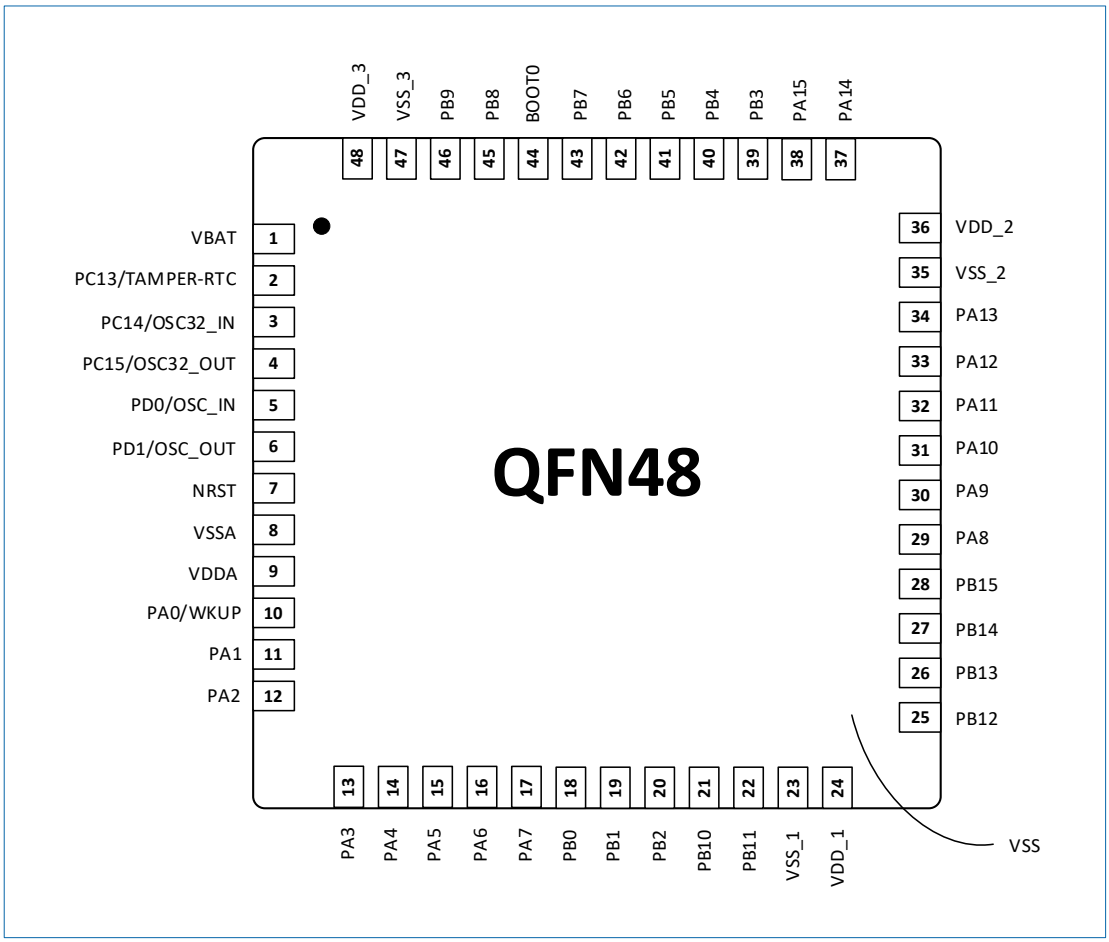

Figure 5-1 QFN48 package pinout

5.2 LQFP48

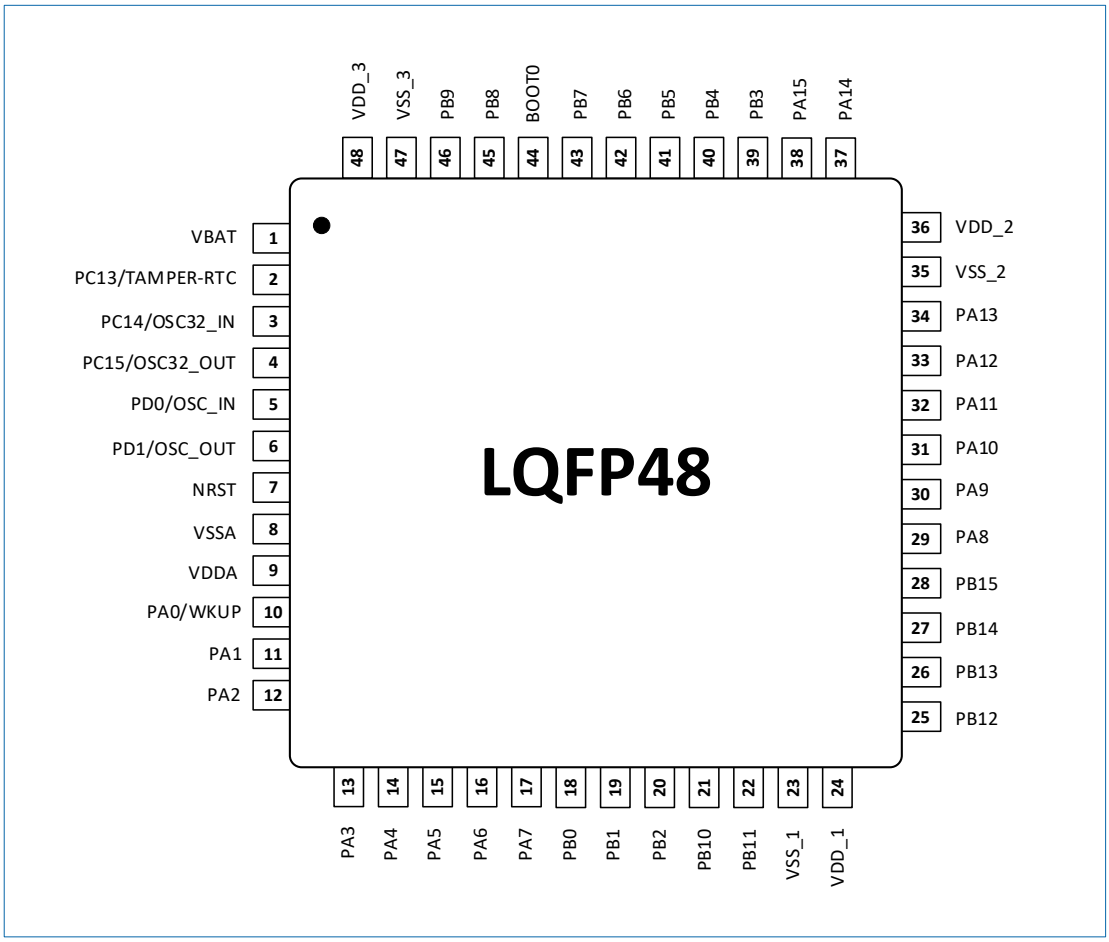

Figure 5-2 LQFP48 package pinout

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5.3 LQFP64

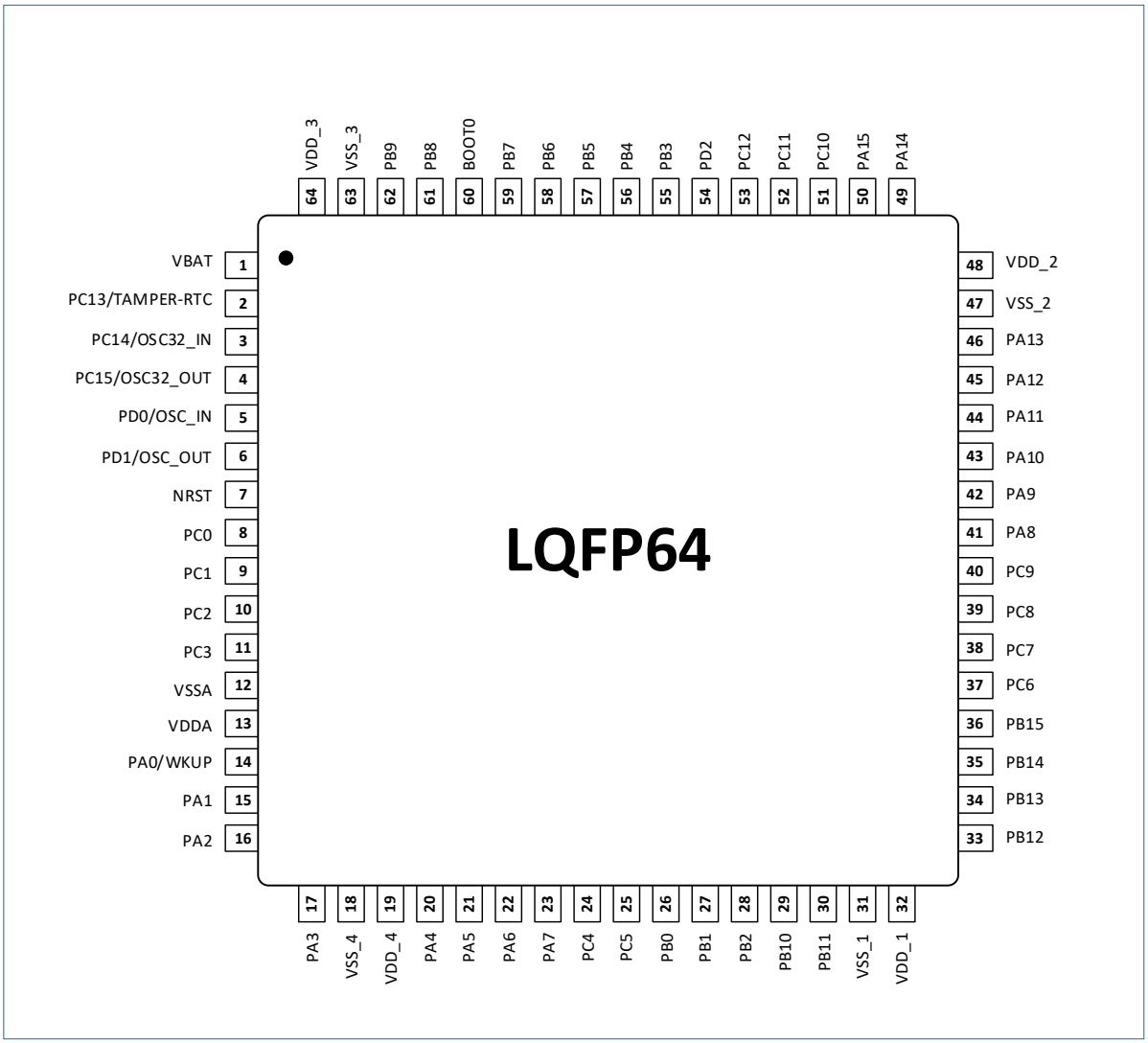

Figure 5-3 LQFP64 package pinout

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5.4 LQFP100

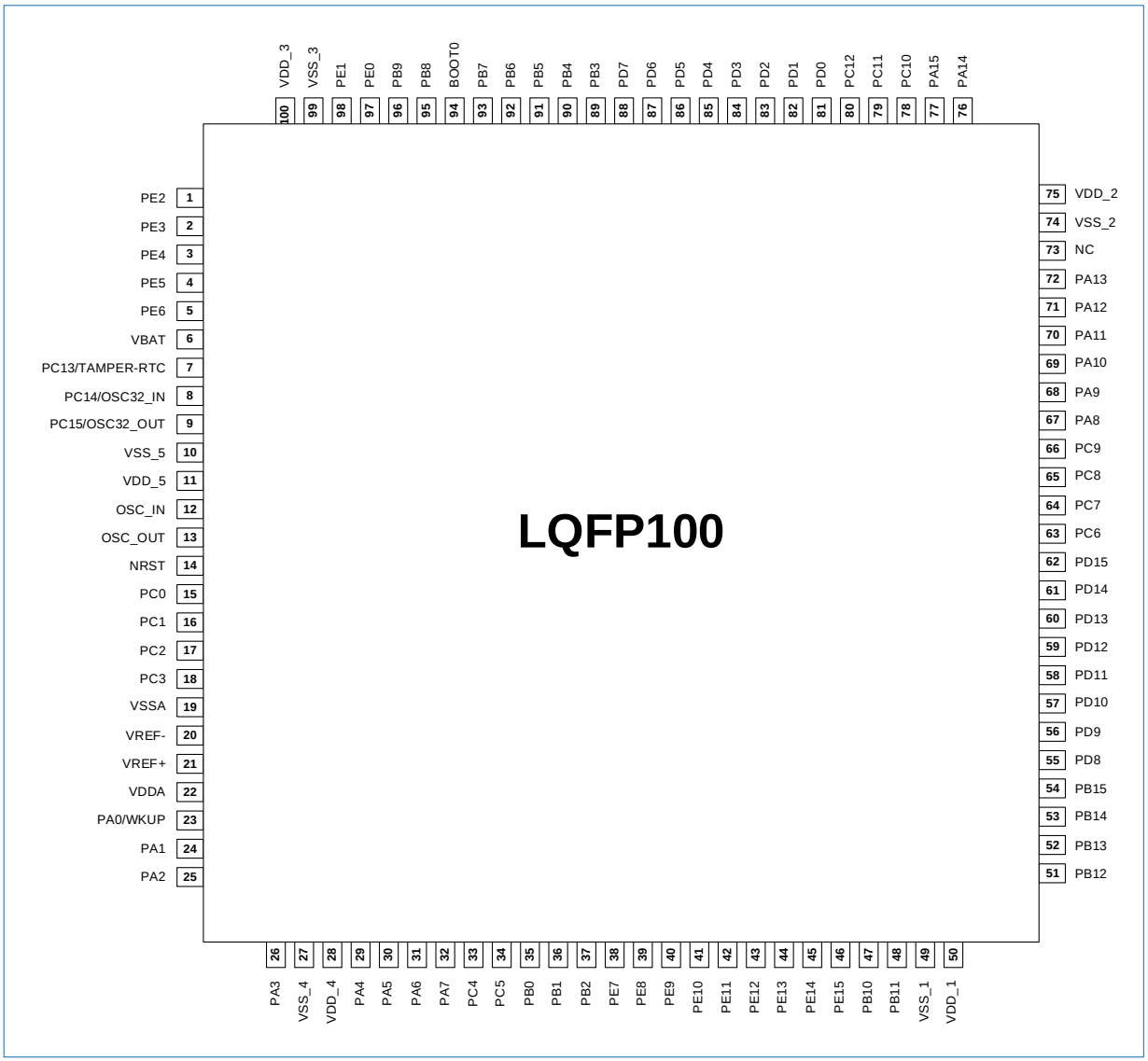

Figure 5-4 LQFP100 package pinout

5.5 Pin descriptions

Table 5-1 Pin description of each package

LQFP48	QFN48	LQFP64	LQFP100	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
0	-	-	-	VSS	S	-	VSS	Ground (Pin 0 is the thermal pad on the QFN package bottom.)	
-	-	-	1	PE2	I/O	-	PE2	TRACECKO	TXEV/EXTIN2
-	-	-	2	PE3	I/O	-	PE3	TRACEDO0	TXEV/EXTIN3
-	-	-	3	PE4	I/O	-	PE4	TRACEDO1	TXEV/EXTIN4
-	-	-	4	PE5	I/O	-	PE5	TRACEDO2	TXEV/EXTIN5
-	-	-	5	PE6	I/O	FT	PE6	TRACEDO3	TXEV/EXTIN6
1	1	1	6	VBAT	S	-	VBAT	-	-
2	2	2	7	PC13/TAMPER-RTC	I/O(3)	-	PC13	TAMPER-RTC/WKUP1/RTCO	TXEV/EXTIN13
3	3	3	8	PC14/OSC32_IN	I/O(3)	-	PC14	OSC32_IN/LSE_CKI	TXEV/EXTIN14
4	4	4	9	PC15/OSC32_OUT	I/O(3)	-	PC15	OSC32_OUT	TXEV/EXTIN15

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LQFP48	QFN48	LQFP64	LQFP100	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
-	-	-	10	VSS_5	S	-	VSS_5	-	-
-	-	-	11	VDD_5	S	-	VDD_5	-	-
5	5	5	-	PD0/OSC_IN	I	-	OSC_IN	OSC_IN/HSE_CKI	TXEV/PD0
6	6	6	-	PD1/OSC_OUT	O	-	OSC_OUT	OSC_OUT	TXEV/PD1
-	-	-	12	OSC_IN	I	-	OSC_IN	OSC_IN/HSE_CKI	-
-	-	-	13	OSC_OUT	O	-	OSC_OUT	OSC_OUT	-
7	7	7	14	NRST	I/O	-	NRST	-	-
-	-	8	15	PC0	I/O	-	PC0	ADC12_IN10	TXEV/EXTIN0
-	-	9	16	PC1	I/O	-	PC1	ADC12_IN11	TXEV/EXTIN1
-	-	10	17	PC2	I/O	-	PC2	ADC12_IN12	TXEV/EXTIN2
-	-	11	18	PC3	I/O	-	PC3	ADC12_IN13	TXEV/EXTIN3
8	8	12	19	VSSA	S	-	VSSA	-	-
-	-	-	20	VREF-	S	-	VREF-	-	-
-	-	-	21	VREF+	S	-	VREF+	-	-
9	9	13	22	VDDA	S	-	VDDA	-	-
10	10	14	23	PA0/WKUP	I/O(3)	-	PA0	WKUP0/USART2_CTS/ ADC12_IN0/TIM2_CH1_ETR/EXTIN0	TXEV
11	11	15	24	PA1	I/O	-	PA1	USART2_RTS/ADC12_IN1/ TIM2_CH2/EXTIN1	TXEV
12	12	16	25	PA2	I/O	-	PA2	USART2_TX/ADC12_IN2/ TIM2_CH3/EXTIN2	TXEV
13	13	17	26	PA3	I/O	-	PA3	USART2_RX/ADC12_IN3/ TIM2_CH4/EXTIN3	TXEV
-	-	18	27	VSS_4	S	-	VSS_4	-	-
-	-	19	28	VDD_4	S	-	VDD_4	-	-
14	14	20	29	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK/ ADC12_IN4/EXTIN4	TXEV
15	15	21	30	PA5	I/O	-	PA5	SPI1_SCK/ADC12_IN5/ EXTIN5	TXEV
16	16	22	31	PA6	I/O	-	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1/EXTIN6	TXEV/TIM1_BKIN
17	17	23	32	PA7	I/O	-	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2/EXTIN7	TXEV/TIM1_CH1N
-	-	24	33	PC4	I/O	-	PC4	ADC12_IN14	TXEV/EXTIN4
-	-	25	34	PC5	I/O	-	PC5	ADC12_IN15	TXEV/EXTIN5
18	18	26	35	PB0	I/O(3)	-	PB0	ADC12_IN8/TIM3_CH3	TXEV/TIM1_CH2N/EXTIN0
19	19	27	36	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4	TXEV/TIM1_CH3N/EXTIN1
20	20	28	37	PB2	I/O	FT	PB2	BOOT1(4)	TXEV/EXTIN2
-	-	-	38	PE7	I/O	FT	PE7	-	TXEV/TIM1_ETR/EXTIN7
-	-	-	39	PE8	I/O	FT	PE8	-	TXEV/TIM1_CH1N/EXTIN8
-	-	-	40	PE9	I/O	FT	PE9	-	TXEV/TIM1_CH1/EXTIN9
-	-	-	41	PE10	I/O	FT	PE10	-	TXEV/TIM1_CH2N/EXTIN10
-	-	-	42	PE11	I/O	FT	PE11	-	TXEV/TIM1_CH2/EXTIN11
-	-	-	43	PE12	I/O	FT	PE12	-	TXEV/TIM1_CH3N/EXTIN12
-	-	-	44	PE13	I/O	FT	PE13	-	TXEV/TIM1_CH3/EXTIN13
-	-	-	45	PE14	I/O	FT	PE14	-	TXEV/TIM1_CH4/EXTIN14
-	-	-	46	PE15	I/O	FT	PE15	-	TXEV/TIM1_BKIN/EXTIN15

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LQFP48	QFN48	LQFP64	LQFP100	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
21	21	29	47	PB10	I/O	-	PB10	I2C2_SCL/USART3_TX	TXEV/TIM2_CH3/EXTIN10
22	22	30	48	PB11	I/O	-	PB11	I2C2_SDA/USART3_RX	TXEV/TIM2_CH4/EXTIN11
23	23	31	49	VSS_1	S	-	VSS_1	-	-
24	24	32	50	VDD_1	S	-	VDD_1	-	-
25	25	33	51	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/USART3_CK/ TIM1_BKIN	TXEV/EXTIN12
26	26	34	52	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N	TXEV/EXTIN13
27	27	35	53	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N/ USART3_RTS	TXEV/EXTIN14
28	28	36	54	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	TXEV/EXTIN15
-	-	-	55	PD8	I/O	FT	PD8	-	TXEV/USART3_TX/EXTIN8
-	-	-	56	PD9	I/O	FT	PD9	-	TXEV/USART3_RX/EXTIN9
-	-	-	57	PD10	I/O	FT	PD10	-	TXEV/USART3_CK/EXTIN10
-	-	-	58	PD11	I/O	FT	PD11	-	TXEV/USART3_CTS/EXTIN11
-	-	-	59	PD12	I/O	FT	PD12	-	TXEV/TIM4_CH1/USART3_RTS/EXTIN12
-	-	-	60	PD13	I/O	FT	PD13	-	TXEV/TIM4_CH2/EXTIN13
-	-	-	61	PD14	I/O	FT	PD14	-	TXEV/TIM4_CH3/EXTIN14
-	-	-	62	PD15	I/O	FT	PD15	-	TXEV/TIM4_CH4/EXTIN15
-	-	37	63	PC6	I/O	FT	PC6	-	TXEV/TIM3_CH1/EXTIN6
-	-	38	64	PC7	I/O	FT	PC7	-	TXEV/TIM3_CH2/EXTIN7
-	-	39	65	PC8	I/O	FT	PC8	-	TXEV/TIM3_CH3/EXTIN8
-	-	40	66	PC9	I/O	FT	PC9	-	TXEV/TIM3_CH4/EXTIN9
29	29	41	67	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ RCC_MCO/EXTIN8	TXEV
30	30	42	68	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2/ EXTIN9	TXEV
31	31	43	69	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3/ EXTIN10	TXEV
32	32	44	70	PA11	I/O	FT	PA11	USART1_CTS/USB_DM/ CAN1_RX/TIM1_CH4/ EXTIN11	TXEV
33	33	45	71	PA12	I/O	FT	PA12	USART1_RTS/USB_DP/ CAN1_TX/TIM1_ETR/ EXTIN12	TXEV
34	34	46	72	PA13/JTMS-SWDIO	I/O	FT	JTMS-SWDIO	-	TXEV/PA13
-	-	-	73	NC	-	-	-	-	-
35	35	47	74	VSS_2	S		VSS_2	-	-
36	36	48	75	VDD_2	S		VDD_2	-	-
37	37	49	76	PA14/JTCK-SWCLK	I/O	FT	JTCK-SWCLK	EXTIN14	TXEV/PA14
38	38	50	77	PA15/JTDI	I/O	FT	JTDI	EXTIN15	TXEV/PA15/TIM2_CH1_ETR /SPI1_NSS
-	-	51	78	PC10	I/O	-	PC10	-	TXEV/USART3_TX/EXTIN10
-	-	52	79	PC11	I/O	-	PC11	-	TXEV/USART3_RX/EXTIN11

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LQFP48	QFN48	LQFP64	LQFP100	Pin Name	Type(1)	5 V-tolerant (2)	Main Function	Alternate Function	Additional Function
-	-	53	80	PC12	I/O	-	PC12	-	TXEV/USART3_CK/EXTIN12
-	-	-	81	PD0	I/O	FT	PD0	-	TXEV/CAN1_RX/EXTIN0
-	-	-	82	PD1	I/O	FT	PD1	-	TXEV/CAN1_TX/EXTIN1
-	-	54	83	PD2	I/O	-	PD2	TIM3_ETR	TXEV/EXTIN2
-	-	-	84	PD3	I/O	FT	PD3	-	TXEV/USART2_CTS/EXTIN3
-	-	-	85	PD4	I/O	FT	PD4	-	TXEV/USART2_RTS/EXTIN4
-	-	-	86	PD5	I/O	FT	PD5	-	TXEV/USART2_TX/EXTIN5
-	-	-	87	PD6	I/O	FT	PD6	-	TXEV/USART2_RX/EXTIN6
-	-	-	88	PD7	I/O	FT	PD7	-	TXEV/USART2_CK/EXTIN7
39	39	55	89	PB3	I/O	-	JTDO	TRACESWO	TXEV/PB3/TIM2_CH2/ SPI1_SCK/EXTIN3
40	40	56	90	PB4	I/O	-	NJTRST	-	TXEV/PB4/TIM3_CH1/SPI1 _MISO/EXTIN4
41	41	57	91	PB5	I/O	-	PB5	I2C1_SMBA	TXEV/TIM3_CH2/SPI1_MO SI/EXTIN5
42	42	58	92	PB6	I/O	-	PB6	I2C1_SCL/TIM4_CH 1	TXEV/USART1_TX/EXTIN6
43	43	59	93	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH 2	TXEV/USART1_RX/EXTIN7
44	44	60	94	BOOT0(4)	I	-	BOOT0	-	-
45	45	61	95	PB8	I/O	-	PB8	TIM4_CH3	TXEV/I2C1_SCL/CAN1_RX/ EXTIN8
46	46	62	96	PB9	I/O	-	PB9	TIM4_CH4	TXEV/I2C1_SDA/CAN1_TX/ EXTIN9
-	-	-	97	PE0	I/O	FT	PE0	TIM4_ETR	TXEV/EXTIN0
-	-	-	98	PE1	I/O	FT	PE1	-	TXEV/EXTIN1
47	47	63	99	VSS_3	S	-	VSS_3	-	-
48	48	64	100	VDD_3	S	-	VDD_3	-	-

(1). I = input, O = output, I/O = input/output, S = supply.

(2). FT: 5 V tolerant.

(3). Except for these I/O pins, the other I/O pins have the Schmitt function and can be configured via registers.

(4). BOOT0/BOOT1 pin is connected to an internal weak pull-down resistor.

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6 Packages

6.1 Package outlines

6.1.1 QFN48

QFN48 is a 7 mm × 7 mm, 0.5 mm pitch package.

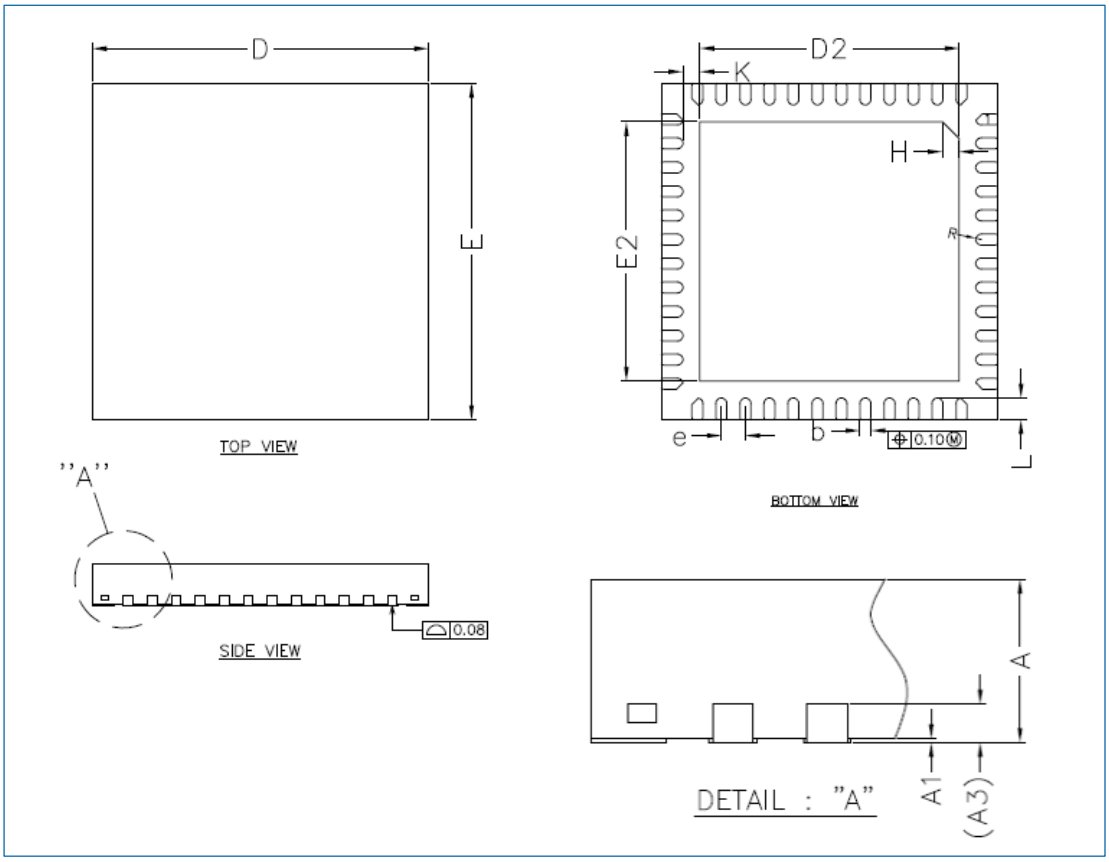

Figure 6-1 QFN48 package outline

Table 6-1 QFN48 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.23	0.28
D	6.924	7.000	7.076
E	6.924	7.000	7.076
D2	5.30	5.40	5.50
E2	5.30	5.40	5.50
e		0.50 BSC	
L	0.350	0.450	0.550
K	0.20	-	-
R	0.09	-	-

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6.1.2 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

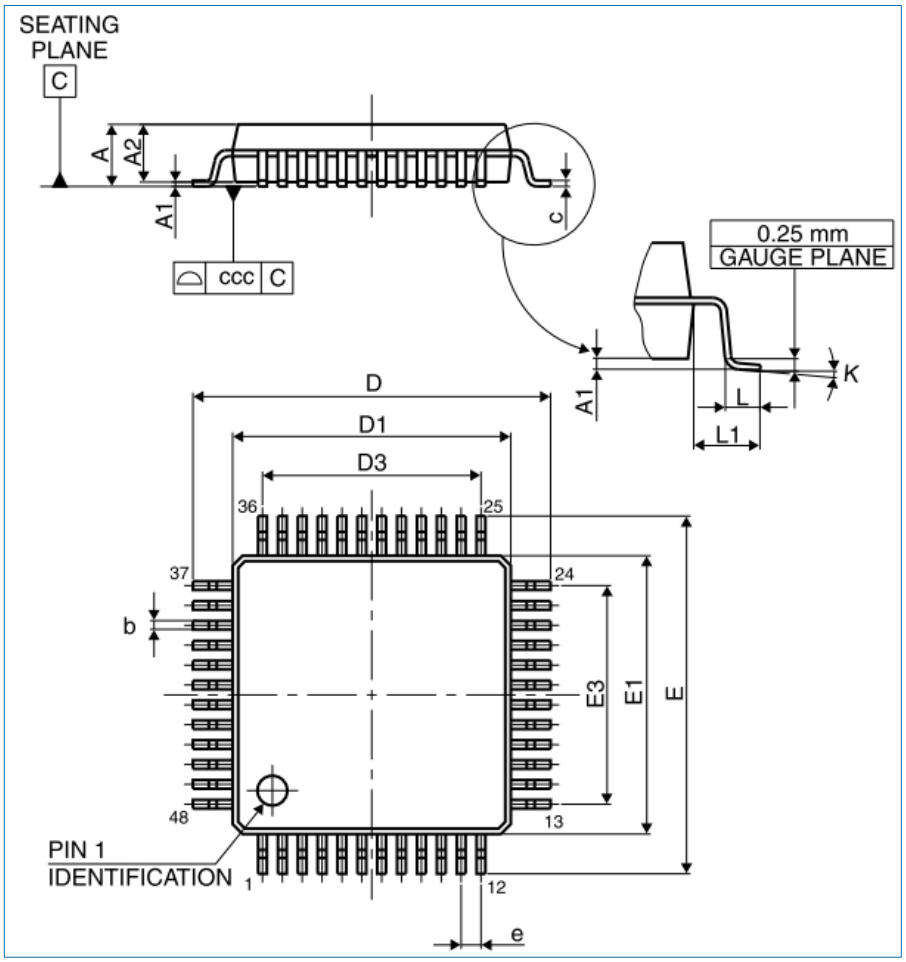

Figure 6-2 LQFP48 package outline

Table 6-2 LQFP48 package parameters

Symbol	Unit: mm			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

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6.1.3 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch package.

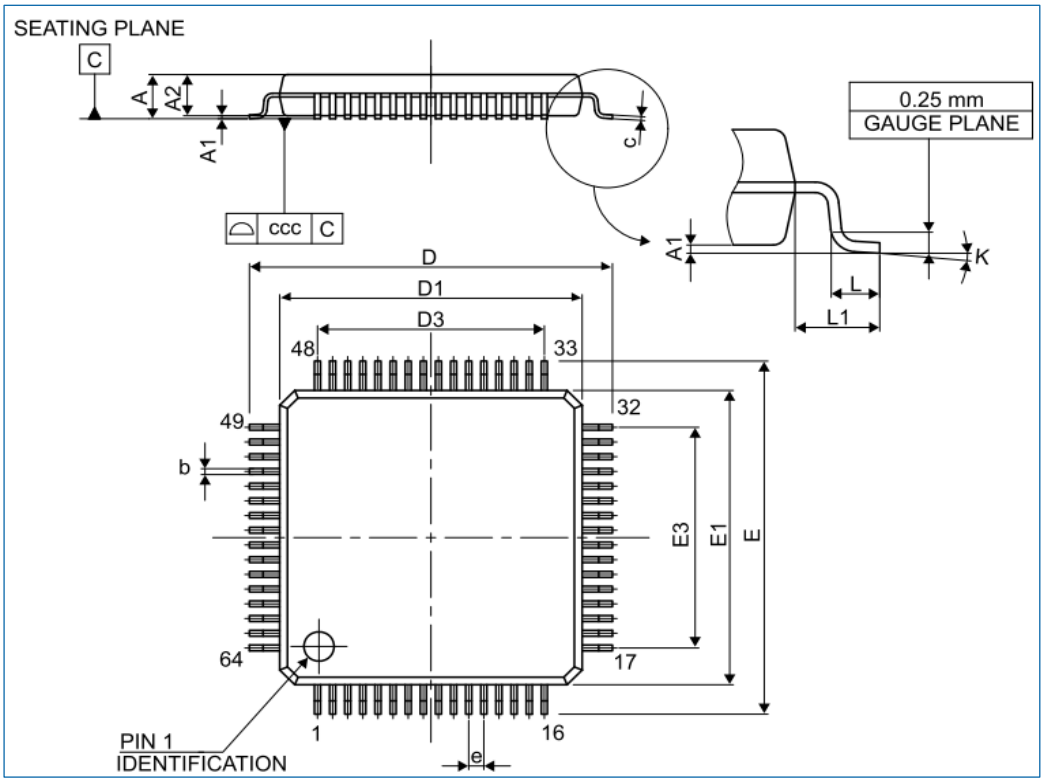

Figure 6-3 LQFP64 package outline

Table 6-3 LQFP64 package parameters

Symbol	Unit: mm			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D		12.000			0.4724	
D1		10.000			0.3937	
D3		7.500	-	-	0.2953	-
E		12.000			0.4724	
E1		10.000			0.3937	
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

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6.1.4 LQFP100

LQFP100 is a 14 mm × 14 mm, 0.5 mm pitch package.

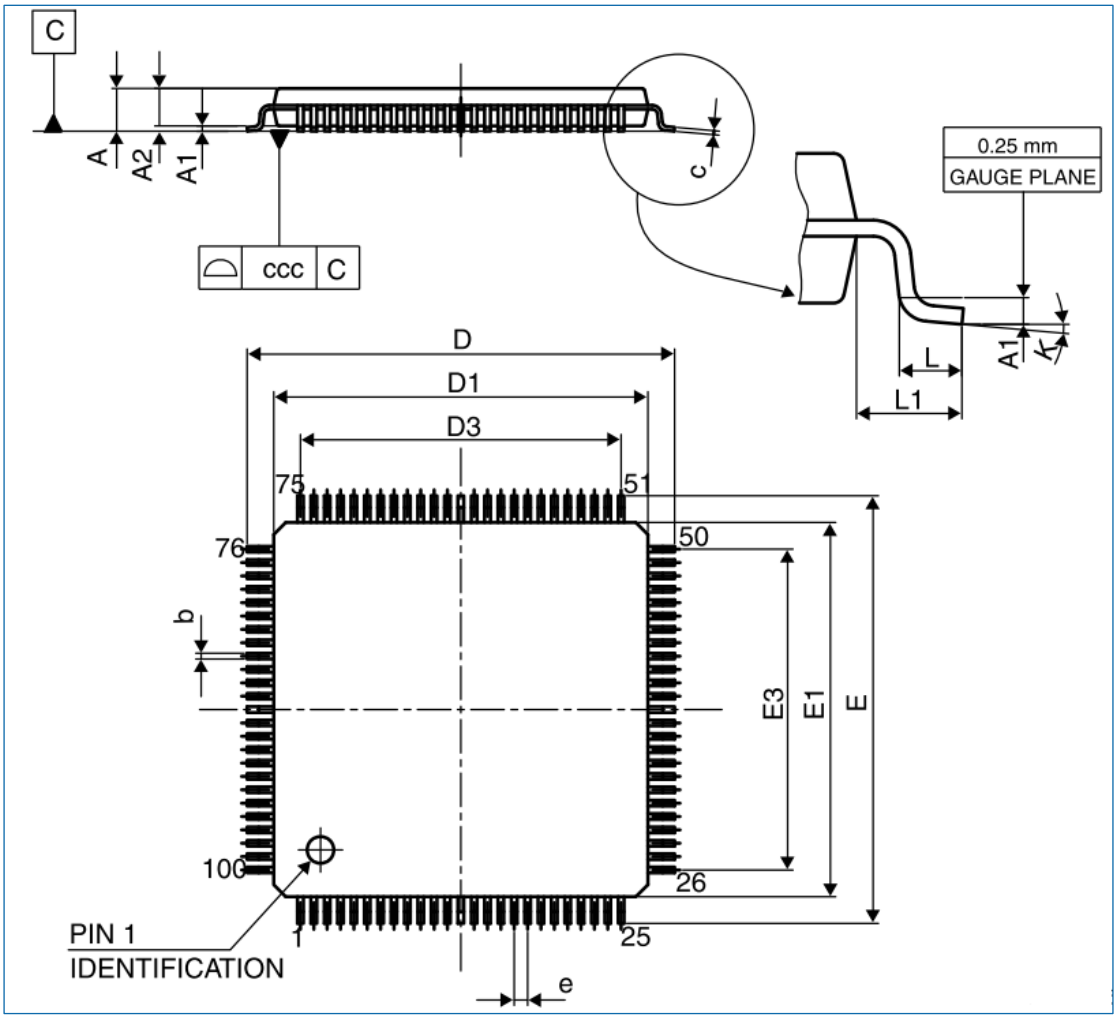

Figure 6-4 LQFP100 package outline

Table 6-4 LQFP100 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

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6.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 6-5 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

6.2.1 QFN48 marking

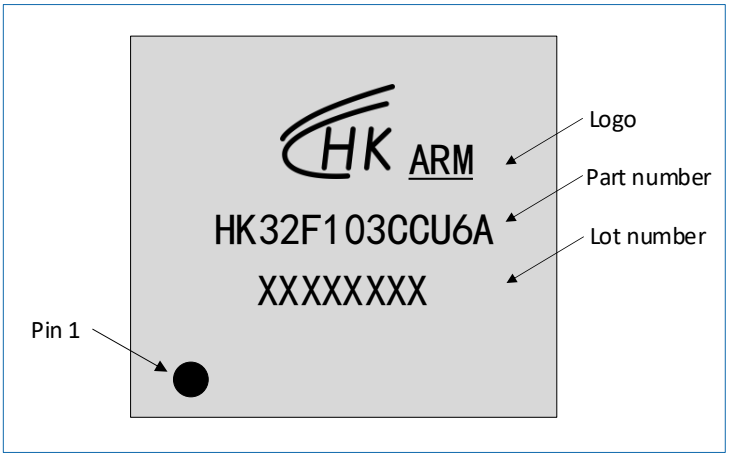

Figure 6-5 QFN48 HK32F103CCU6A marking example

6.2.2 LQFP48 marking

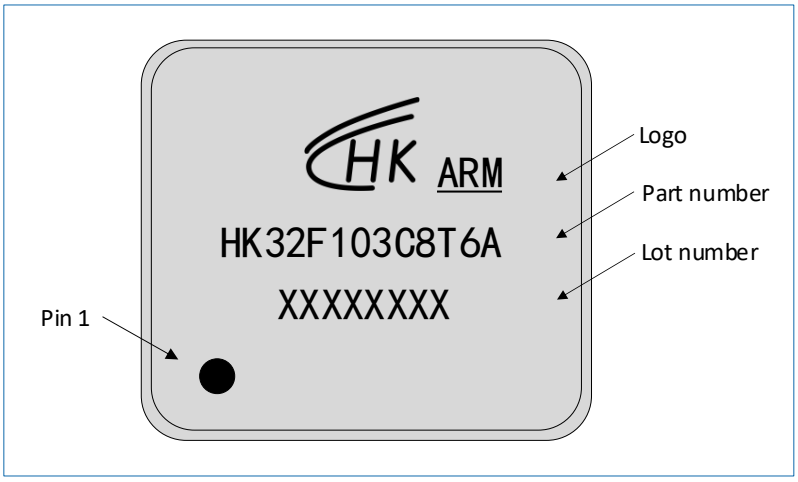

Figure 6-6 LQFP48 HK32F103C8T6A marking example

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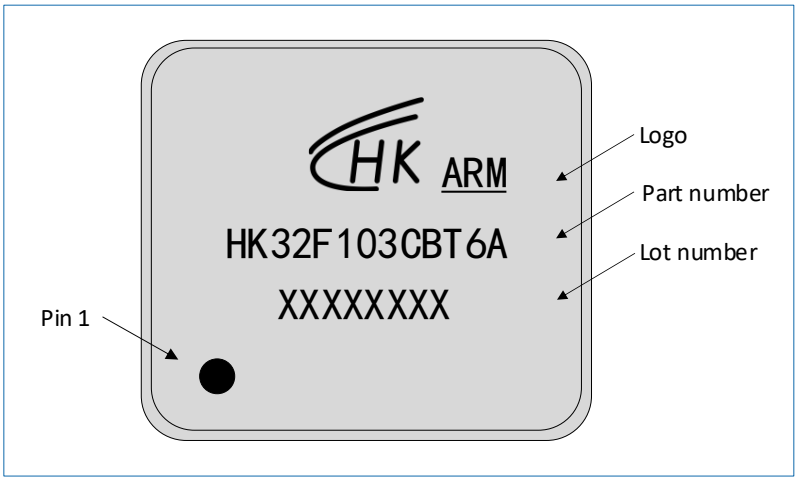

Figure 6-7 LQFP48 HK32F103CBT6A marking example

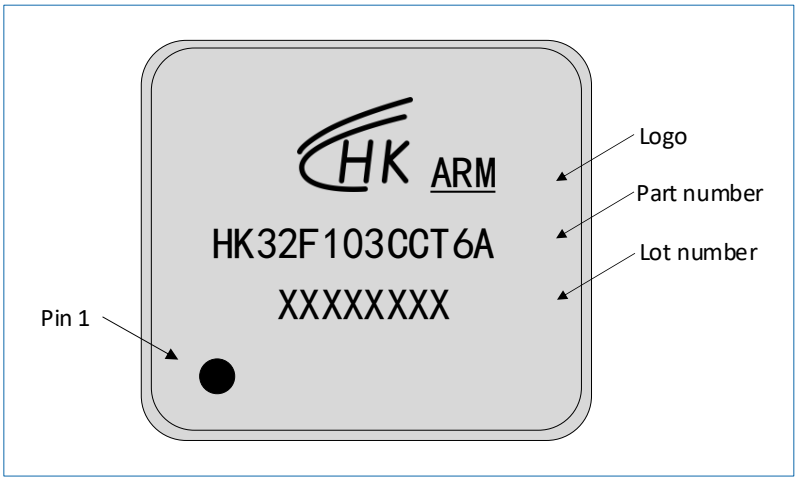

Figure 6-8 LQFP48 HK32F103CCT6A marking example

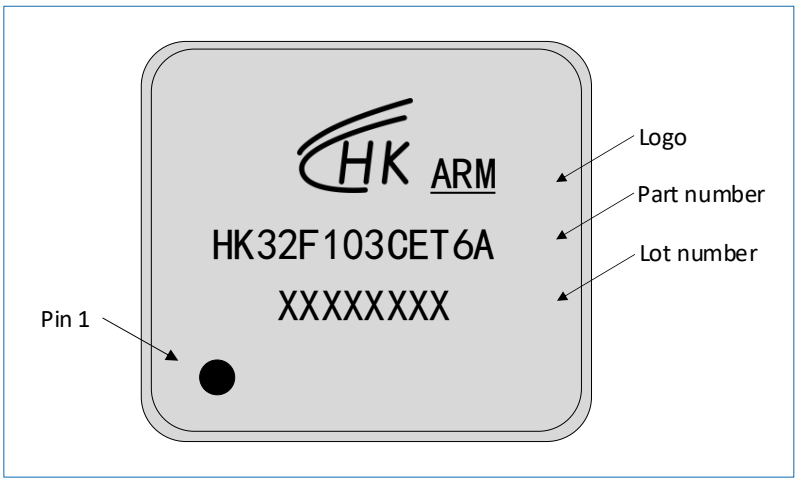

Figure 6-9 LQFP48 HK32F103CET6A marking example

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6.2.3 LQFP64 marking

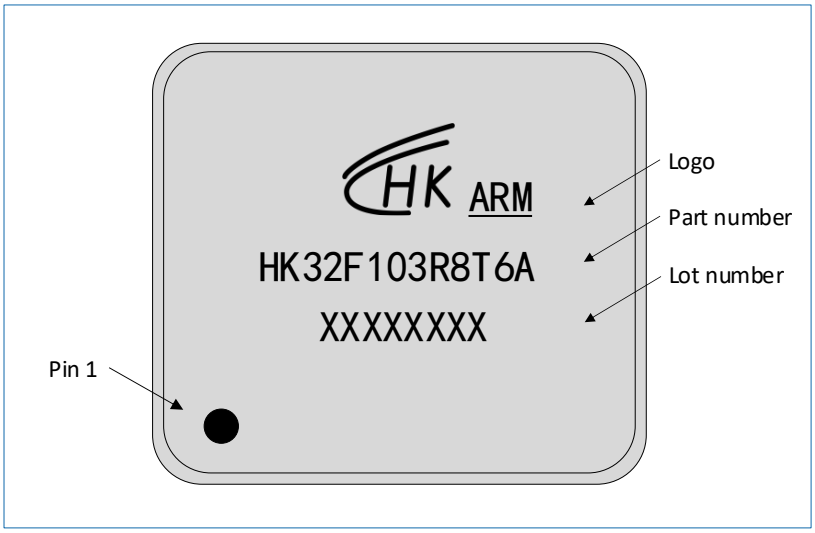

Figure 6-10 LQFP64 HK32F103R8T6A marking example

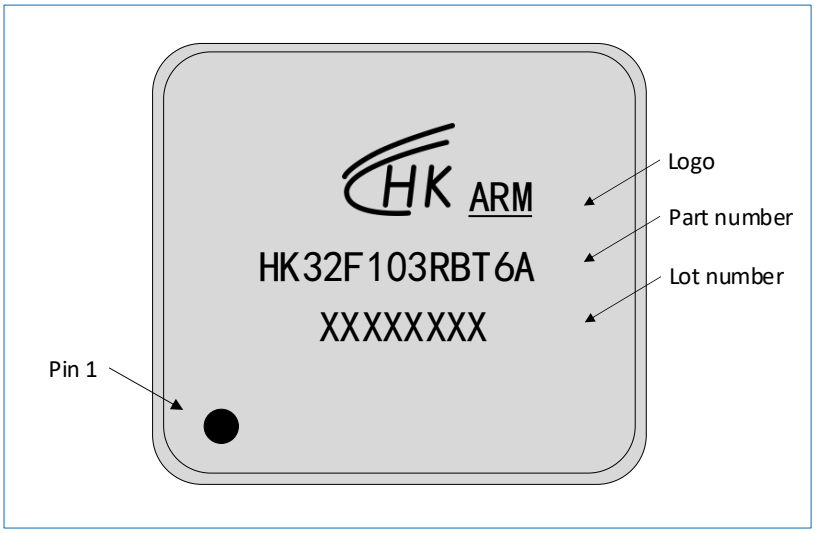

Figure 6-11 LQFP64 HK32F103RBT6A marking example

6.2.4 LQFP100 marking

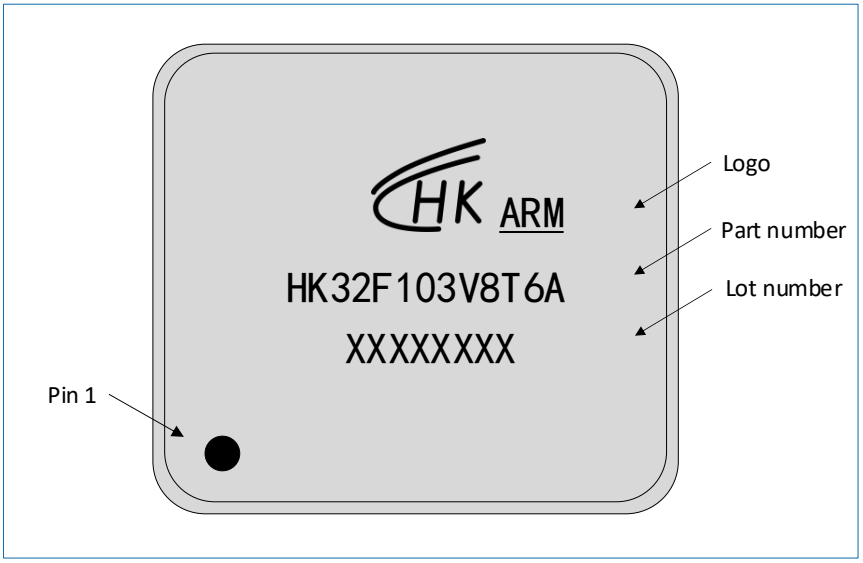

Figure 6-12 LQFP100 HK32F103V8T6A marking example

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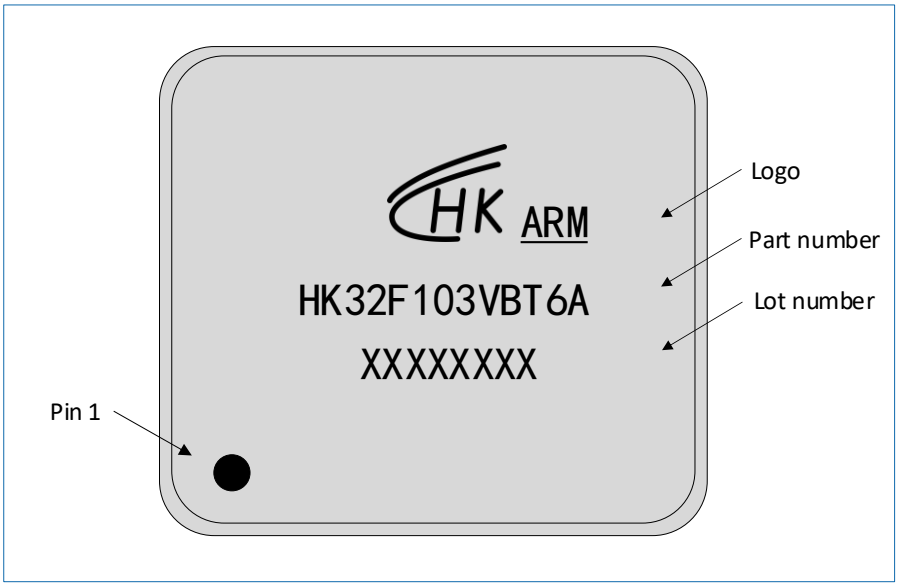

Figure 6-13 LQFP100 HK32F103VBT6A marking example

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7 Ordering information

7.1 Device numbering conventions

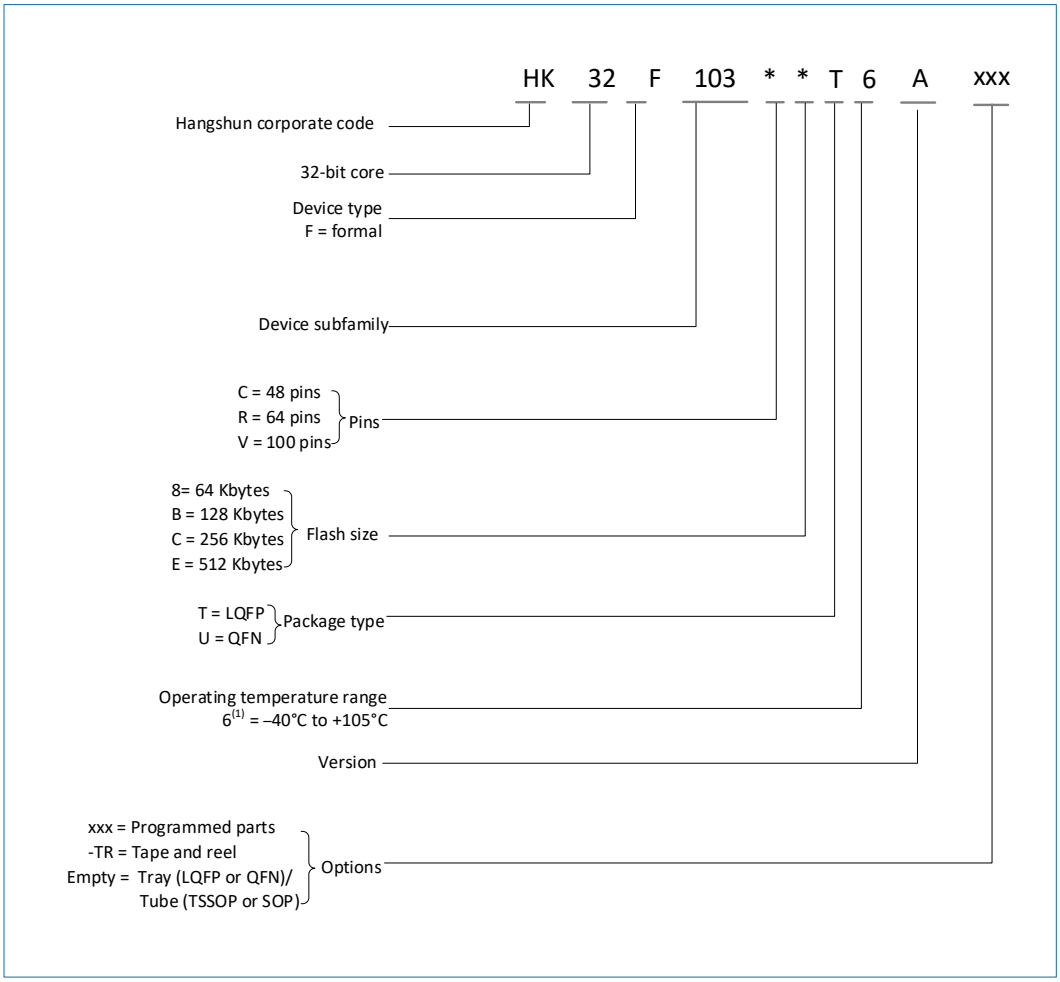

Figure 7-1 Device numbering conventions

(1). The HK32F103x8xBT6A series was first released in earlier times, so its device numbering is based on *Hangshun Product Naming Conventions V0.9*, which is slightly different from the latest naming conventions.

7.2 Packaging information

Table 7-1 HK32F103x8xBT6A packaging information

Package	Part Number	Shipping Option	Remarks
QFN48	HK32F103CCU6A	Tray	
QFN48	HK32F103CCU6A-TR	Tape and reel	
LQFP48	HK32F103C8T6A	Tray	
LQFP48	HK32F103C8T6A-TR	Tape and reel	
LQFP48	HK32F103CBT6A	Tray	
LQFP48	HK32F103CBT6A-TR	Tape and reel	
LQFP48	HK32F103CCT6A	Tray	
LQFP48	HK32F103CCT6A-TR	Tape and reel	
LQFP48	HK32F103CET6A	Tray	
LQFP48	HK32F103CET6A-TR	Tape and reel	
LQFP64	HK32F103R8T6A	Tray	
LQFP64	HK32F103R8T6A-TR	Tape and reel	
LQFP64	HK32F103RBT6A	Tray	
LQFP64	HK32F103RBT6A-TR	Tape and reel	
LQFP100	HK32F103V8T6A	Tray	
LQFP100	HK32F103V8T6A-TR	Tape and reel	
LQFP100	HK32F103VBT6A	Tray	
LQFP100	HK32F103VBT6A-TR	Tape and reel	

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8 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
FM	Fast Mode
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSB	Least Significant Bit
LSE	Low-Speed External (clock signal)
LSI	Low-speed Internal (clock signal)
LVD	Low Voltage Detector
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PVD	Programmable Voltage Detector
PWM output	Pulse Width Modulation
RCC	Reset and Clock Control
RTC	Real-time Clock
SDIO	Secure Digital Input and Output
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

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