HK32F030MxxxxA/HK32F0301MxxxxA

Datasheet

Version: 1.6

Release Date: 2024-01-12

Shenzhen Hangshun Chip Technology R&D Co., Ltd.

http://www.hsxp-hk.com

Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F030MxxxxA/HK32F0301MxxxxA series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32F030MxxxxA/HK32F0301MxxxxA.

Audience

This document is intended for:

- HK32F030MxxxxA/HK32F0301MxxxxA developers
- HK32F030MxxxxA/HK32F0301MxxxxA testers
- HK32F030MxxxxA/HK32F0301MxxxxA users

Release Notes

This document is applicable to HK32F030MxxxxA/HK32F0301MxxxxA series MCUs.

Revision History

Version	Date	Description
0.99	2022/03/01	The alpha version release.
1.0	2022/10/14	The initial release
1.1	2022/11/04	1. Corrected grammar errors in the whole document. 2. Updated section "3.17 Timers", 3. Changed the LSI frequency in Table 3-3 Clock sources from 114 kHz to 128 kHz. 4. Corrected the value of f_{ADC} in Table 4-20 ADC characteristics and the value in Table 4-21 Maximum input impedance values (f_{ADC} = 12 MHz).
1.2	2022/11/15	1. Updated section "4.2.4 Operating current". 2. Updated the maximum communication rate of I2C. 3. Updated section "2.2 Device overview".
1.3	2022/11/22	Updated section "6 Pinouts and pin descriptions".
1.4	2023/01/10	Updated all pinout figures in section "6 Pinouts and pin descriptions".
1.5	2023/02/16	1. Updated Table 2-1 HK32F030MxxxxA/HK32F0301MxxxxA features. 2. Updated section "6 Pinouts and pin descriptions".
1.6	2024/01/12	1. Updated the Flash size from 32 Kbytes to 16/32 Kbytes. 2. Updated Figure 3-3 Reset signal. 3. Changed the prescaler in section "3.19 IWDG" to 8-bit. 4. Updated section "4.2.3 Internal reference voltage". 5. Updated the operating current in low-power mode under 25°C in section "4.2.4 Operating current characteristics". 6. Updated the erase time in sections "4.2.8 EEPROM characteristics" and "4.2.9 Flash memory characteristics". 7. Updated Table 4-8 Operating current characteristics of HK32F030MxxxxA. 8. Corrected section "6.7 TSSOP16": exchanged pins 15 and 16 in the package pinout figure. 9. Corrected section "6.5 TSSOP24": changed pin 21 from PD0 to PC7. 10. Synchronized the above two changes to sections "6.9 Pin descriptions" and "6.10.1 IOMUX of the TSSOP16 package". 11. Updated sections "6.3 QFN20", "6.2 QFN24", and "6.1 QFN28": added the description

Version	Date	Description
		that the thermal pad on the bottom is used as the VSS pin. 12. Updated section "6.9 Pin descriptions": added the description that pin 0 is used as VSS in QFN packages. 13. Added sections "7.2 Device marking" and "8.1 Device numbering conventions". 14. Updated Figure 8-1 HK32F030MxxxxA device numbering conventions.

Contents

1 Introduction 1
2 Product overview 3
2.1 Features 3
2.2 Device overview 5
3 Function description 7
3.1 Block diagram 7
3.2 Memory mapping 7
3.3 Memory 8
3.3.1 Flash 8
3.3.2 SRAM 8
3.3.3 EEPROM 8
3.4 CRC calculation unit 8
3.5 Power supply scheme 9
3.6 Power supply monitor 9
3.7 Low-power modes 9
3.8 I/O retention 9
3.9 STBAWU timer 9
3.10 Resets 9
3.10.1 System reset 10
3.10.2 Power reset 10
3.11 Clocks and clock tree 10
3.12 SYSCFG 12
3.13 GPIO 12
3.14 IOMUX 12
3.15 Interrupts and events 13
3.15.1 NVIC 13
3.15.2 SysTick timer 13
3.15.3 EXTI 13
3.16 ADC 14
3.16.1 AWD wakeup function 14
3.17 Timers 14
3.17.1 Advanced timer 15
3.17.2 General-purpose timer 15
3.17.3 Basic timer 15
3.18 AWUT 15
3.19 IWDG 15

3.20 WWDG 15
3.21 I2C bus 16
3.22 USART/UART 16
3.23 SPI/I2S 16
3.24 Beeper 17
3.25 64-bit UID 17
3.26 Debug port 17
4 Electrical characteristics 18
4.1 Absolute maximum values 18
4.1.1 Voltage characteristics 18
4.1.2 Current characteristics 18
4.1.3 Temperature characteristics 18
4.2 Operating conditions 18
4.2.1 Recommended operating conditions 18
4.2.2 POR/PDR characteristics 19
4.2.3 Internal reference voltage 19
4.2.4 Operating current characteristics 19
4.2.5 HSI clock characteristics 20
4.2.6 LSI clock characteristics 21
4.2.7 GPIO external input clock characteristics 21
4.2.8 EEPROM characteristics 21
4.2.9 Flash memory characteristics 21
4.2.10 I/O pin input characteristics 22
4.2.11 I/O pin output characteristics 22
4.2.12 NRST pin characteristics 22
4.2.13 TIM characteristics 22
4.2.14 ADC characteristics 22
5 Typical circuitry 25
6 Pinouts and pin descriptions 26
6.1 QFN28 26
6.2 QFN24 27
6.3 QFN20 28
6.4 TSSOP28 29
6.5 TSSOP24 30
6.6 TSSOP20 31
6.7 TSSOP16 32
6.8 SOP8 33
6.9 Pin descriptions 33

6.10 IOMUX 36
6.10.1 IOMUX of the TSSOP16 package 37
6.10.2 IOMUX of the SOP8 package 38
6.11 Alternate function table 40
7 Packages 41
7.1 Package outlines 41
7.1.1 QFN28 41
7.1.2 QFN24 42
7.1.3 QFN20 43
7.1.4 TSSOP28 45
7.1.5 TSSOP24 46
7.1.6 TSSOP20 47
7.1.7 TSSOP16 48
7.1.8 SOP8 49
7.2 Device marking 50
7.2.1 QFN28 marking 50
7.2.2 QFN24 marking 51
7.2.3 QFN20 marking (4 mm × 4 mm package) 51
7.2.4 QFN20 marking (3 mm × 3 mm package) 52
7.2.5 TSSOP28 marking 53
7.2.6 TSSOP24 marking 54
7.2.7 TSSOP20 marking 55
7.2.8 TSSOP16 marking 55
7.2.9 SOP8 marking 56
8 Ordering information 58
8.1 Device numbering conventions 58
8.2 Packaging information 59
9 Acronyms 61
10 Legal and contact information 62

1 Introduction

This document is the datasheet for HK32F030MxxxxA/HK32F0301MxxxxA series MCUs. HK32F030MxxxxA/HK32F0301MxxxxA is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun) for a wide range of purposes. This MCU family includes:

- HK32F030MxxxxA:
  - HK32F030MGxU7A (QFN28 package)
    - HK32F030MG6U7A
    - HK32F030MG4U7A
  - HK32F030MExU7A (QFN24 package)
    - HK32F030ME6U7A
    - HK32F030ME4U7A
  - HK32F030MFxU7A/HK32F030MFxN7A (QFN20 package)
    - HK32F030MF6U7A
    - HK32F030MF4U7A
    - HK32F030MF4N7A
    - HK32F030MF6N7A
  - HK32F030MGxP7A (TSSOP28 package)
    - HK32F030MG6P7A
    - HK32F030MG4P7A
  - HK32F030MExP7A (TSSOP24 package)
    - HK32F030ME4P7A
    - HK32F030ME6P7A
  - HK32F030MFxP7A (TSSOP20 package)
    - HK32F030MF6P7A
    - HK32F030MF4P7A
  - HK32F030MDxP7A (TSSOP16 package)
    - HK32F030MD6P7A
    - HK32F030MD4P7A
  - HK32F030MJxM7A (SOP8 package)
    - HK32F030MJ6M7A
    - HK32F030MJ4M7A
- HK32F0301MxxxxA:
  - HK32F0301MGxU7A (QFN28 package)
    - HK32F0301MG6U7A
    - HK32F0301MG4U7A
  - HK32F0301MExU7A (QFN24 package)
    - HK32F0301ME6U7A
    - HK32F0301ME4U7A

- HK32F0301MFxU7A//HK32F0301MFxN7A (QFN20 package)
  - HK32F0301MF6U7A
  - HK32F0301MF4U7A
  - HK32F0301MF4N7A
  - HK32F0301MF6N7A
- HK32F0301MGxP7A (TSSOP28 package)
  - HK32F0301MG6P7A
  - HK32F0301MG4P7A
- HK32F0301MExP7A (TSSOP24 package)
  - HK32F0301ME4P7A
  - HK32F0301ME6P7A
- HK32F0301MFxP7A (TSSOP20 package)
  - HK32F0301MF6P7A
  - HK32F0301MF4P7A
- HK32F0301MDxP7A (TSSOP16 package)
  - HK32F0301MD6P7A
  - HK32F0301MD4P7A
- HK32F0301MJxM7A (SOP8 package)
  - HK32F0301MJ6M7A
  - HK32F0301MJ4M7A

For more details of HK32F030MxxxxA/HK32F0301MxxxxA, see *HK32F030MxxxxA/HK32F0301MxxxxA User Manual*.

2 Product overview

HK32F030MxxxxA/HK32F0301MxxxxA adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 32/48 MHz. Each HK32F030MxxxxA/HK32F0301MxxxxA MCU has 16/32 Kbytes of Flash, 432 bytes of EEPROM, and four Kbytes of SRAM. You can configure the Flash control register to remap interrupt vectors in the 32-Kbyte space.

Except for the power pins and ground pins, all the other pins of HK32F030MxxxxA/HK32F0301MxxxxA can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32F030MxxxxA/HK32F0301MxxxxA incorporates a wide selection of communication interfaces:

- 1 × high-speed USART of up to 6 Mbit/s

  The universal synchronous asynchronous receiver/transmitter (USART) supports synchronous and asynchronous full-duplex or half-duplex communication, multimaster communication, LIN protocol, Smart Card protocol, and IrDA SIR ENDEC. The RX and TX pin functions can be exchanged by using the software. The USART can wake up the MCU from Stop mode when receiving data.
- 3 × high-speed UARTs of up to 6 Mbit/s
- 1 × high-speed SPI/I2S of up to 18 Mbit/s

  The SPI/I2S supports the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, automatic cyclic redundancy check (CRC), and I2S protocol.
- 1 × high-speed I2C of up to 400 kbit/s

  The I2C supports the 400 kbit/s and 100 kbit/s transmission rates, master/slave mode, multimaster mode, 7-bit/10-bit addressing, and SMBus protocol. The I2C can wake up the MCU from Stop mode when receiving data.

HK32F030MxxxxA/HK32F0301MxxxxA embeds a 16-bit advanced PWM timer (four PWM outputs in total, three of which have programmable inserted dead-times), a 16-bit general-purpose PWM timer (four PWM outputs in total), and a 16-bit basic timer (for periodic outputs of CPU interrupts).

HK32F030MxxxxA/HK32F0301MxxxxA also incorporates the analog circuitry: a 12-bit ADC (1 MSPS), a power-on reset (POR)/power-down reset (PDR) circuitry, and an internal reference voltage (sampled by on-chip ADC).

HK32F030MxxxxA/HK32F0301MxxxxA supports multiple power consumption modes. In low-power modes, HK32F030MxxxxA/HK32F0301MxxxxA MCUs can be automatically woken up by the internal low-power timer.

HK32F030MxxxxA/HK32F0301MxxxxA can operate in the –40°C to +105°C temperature range, from a 1.8 V to 3.6 V power supply. It meets the environmental requirements of most applications.

With its diversified peripheral interfaces, HK32F030MxxxxA/HK32F0301MxxxxA is suitable for a wide range of applications:

- Programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- CPU core

- ARM® Cortex™-M0
- Maximum frequency: 32 MHz (HK32F030MxxxxA)/48 MHz (HK32F0301MxxxxA)
- 24-bit SysTick timer
- Supports the remapping of interrupt vectors (by configuring the Flash control register)

- Operating voltage range: 1.8 V to 3.6 V
- Operating temperature range: –40°C to +105°C
- Typical operating current
  - HK32F030MxxxxA
    - Run mode: 5.2 mA@32 MHz@3.3 V
    - Sleep mode: 2.0 mA@32 MHz@3.3 V
    - Stop mode: 565 µA@3.3 V
    - Low-power Stop mode: 298 µA@3.3 V
  - HK32F0301MxxxxA
    - Run mode: 5.1 mA@48 MHz@3.3 V
    - Sleep mode: 2.1 mA@48 MHz@3.3 V
    - Stop mode: 565 µA@3.3 V
    - Low-power Stop mode: 298 µA@3.3 V
    - Standby mode: 0.03 µA@3.3 V
- Up to 32 Kbytes of Flash (256 pages, 128 bytes per page; 32-bit reading, 16-bit writing)
  - Separate read and write protection for Flash data
  - 432-byte EEPROM (programmed by byte: 20 µs)
  - 4-Kbyte SRAM
- Cyclic redundancy check (CRC) hardware implementation unit
- Clock
  - High-speed internal clock (HSI): 32 MHz (HK32F030MxxxxA)/48 MHz (HK32F0301MxxxxA)
  - Low-speed internal clock (LSI): 128 kHz
  - GPIO external input clock: 32 MHz (maximum value)
- Reset
  - Low level on the NRST pin (external reset)
  - Window watchdog reset (WWDG reset)
  - Independent watchdog reset (IWDG reset)
  - Power reset
  - Software reset (SW reset)
  - Low-power management reset
- GPIO
  - Up to 24 (HK32F030MxxxxA)/26 (HK32F0301MxxxxA) GPIOs
  - Each can be used for external interrupt inputs
  - Built-in pull-up/pull-down resistors that can be turned on or off
  - Support open-drain output
  - Output drive capacity configurable

- Pin multiplexing controller IOMUX
  - In small packages like SOP8 and TSSOP16, the mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX.
- Data communication interface
  - 1 × high-speed USART of up to 6 Mbit/s: can wake up the MCU from Stop mode when receiving data
  - 3 × high-speed UARTs of up to 6 Mbit/s
  - 1 × high-speed I2C of up to 400 kbit/s: can wake up the MCU from Stop mode when receiving data
  - 1 × high-speed SPI/I2S of up to 18 Mbit/s
- Timer and PWM generator
  - 1 × 16-bit advanced PWM timer: four PWM outputs in total, three of which are complementary outputs with programmable inserted dead-times
  - 1 × 16-bit general-purpose PWM timer (four PWM outputs in total)
  - 1 × 16-bit basic timer (supports CPU interrupts)
  - 1 × auto-wakeup unit timer (AWUT) working in Stop mode
- Beeper
  - 1 × beeper, which can output 1 kHz, 2 kHz, 4 kHz, or 8 kHz pulses
  - In Stop mode, the beeper keeps operating and can trigger ADC sampling periodically.
- On-chip analog circuitry
  - 1 × 12-bit ADC (1 MSPS, up to five external analog input channels and one internal channel, differential pair input supported)
  - 1 × POR/PDR circuitry
  - 1 × 0.8 V internal reference voltage (sampled by ADC on chip)
- CPU trace and debug
  - Serial wire debug (SWD) interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- UID
  - 64-bit unique ID (UID) for each HK32F030MxxxxA/HK32F0301MxxxxA MCU
- Reliability
  - Passes HBM3000V/CDM1750V/LU800mA level tests.

2.2 Device overview

Table 2-1 HK32F030MxxxxA/HK32F0301MxxxxA series features

Feature	HK32F030 MJxM7A/ HK32F0301 MJxM7A	HK32F030 MDxP7A/ HK32F0301 MDxP7A	HK32F030 MFxP7A/ HK32F0301 MFxP7A	HK32F030 MExP7A/ HK32F0301 MExP7A	HK32F030 MGxP7A/ HK32F0301 MGxP7A	HK32F030 MFxU7A/Fx N7A HK32F0301 MFxU7A/Fx N7A	HK32F030 MExU7A/ HK32F0301 MExU7A	HK32F030 MGxU7A/ HK32F0301 MGxU7A
GPIO	6	14	16/18	20/22	24/26	16/18	20/22	24/26
Package	SOP8	TSSOP16	TSSOP20	TSSOP24	TSSOP28	QFN20	QFN24	QFN28
Operating voltage	1.8 V – 3.6 V							
Operating temperature	–40°C to +105°C							

Feature		HK32F030 MJxM7A/ HK32F0301 MJxM7A	HK32F030 MDxP7A/ HK32F0301 MDxP7A	HK32F030 MFxP7A/ HK32F0301 MFxP7A	HK32F030 MExP7A/ HK32F0301 MExP7A	HK32F030 MGxP7A/ HK32F0301 MGxP7A	HK32F030 MFxU7A/Fx N7A HK32F0301 MFxU7A/Fx N7A	HK32F030 MExU7A/ HK32F0301 MExU7A	HK32F030 MGxU7A/ HK32F0301 MGxU7A
Memory	Flash (Kbyte)	16/32	16/32	16/32	16/32	16/32	16/32	16/32	16/32
	SRAM (Kbyte)	4							
	EEPROM (byte)	432							
CPU	Core	Cortex®-M0							
	Frequency	HK32F030MxxxxA: 32 MHz (maximum value) HK32F0301MxxxxA: 48 MHz (maximum value)							
Clock	LSI	128 kHz							
	HSI	HK32F030MxxxxA: 32 MHz HK32F0301MxxxxA: 48 MHz							
	GPIO external input clock	32 MHz (maximum value)							
Timer	Advanced timer	1 (16-bit): TIM1							
	General-purpose timer	1 (16-bit): TIM2							
	Basic timer	1 (16-bit): TIM6							
	SysTick timer	1							
	Auto-wakeup unit timer (AWUT)	1							
	IWDG	1							
	WWDG	1							
Peripheral comm.	USART	1							
	UART	0	3						
	I2C	1							
	SPI/I2S	1							
ADC	ADC (external channels)	1 (3 external channels)	1 (4 external channels)	1 (5 external channels)					
	Reference selection	Internal reference voltage							
	ADC sampling rate	1 MSPS							
	ADC accuracy	12-bit							
Beeper		1							
CRC		1							
64-bit UID		1							

3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor that provides an MCU platform featuring low cost and low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With the ARM Cortex®-M0 core embedded, the HK32F030MxxxxA/HK32F0301MxxxxA family is compatible with ARM tools and software.

The following figure shows the block diagram of HK32F030MxxxxA/HK32F0301MxxxxA MCUs:

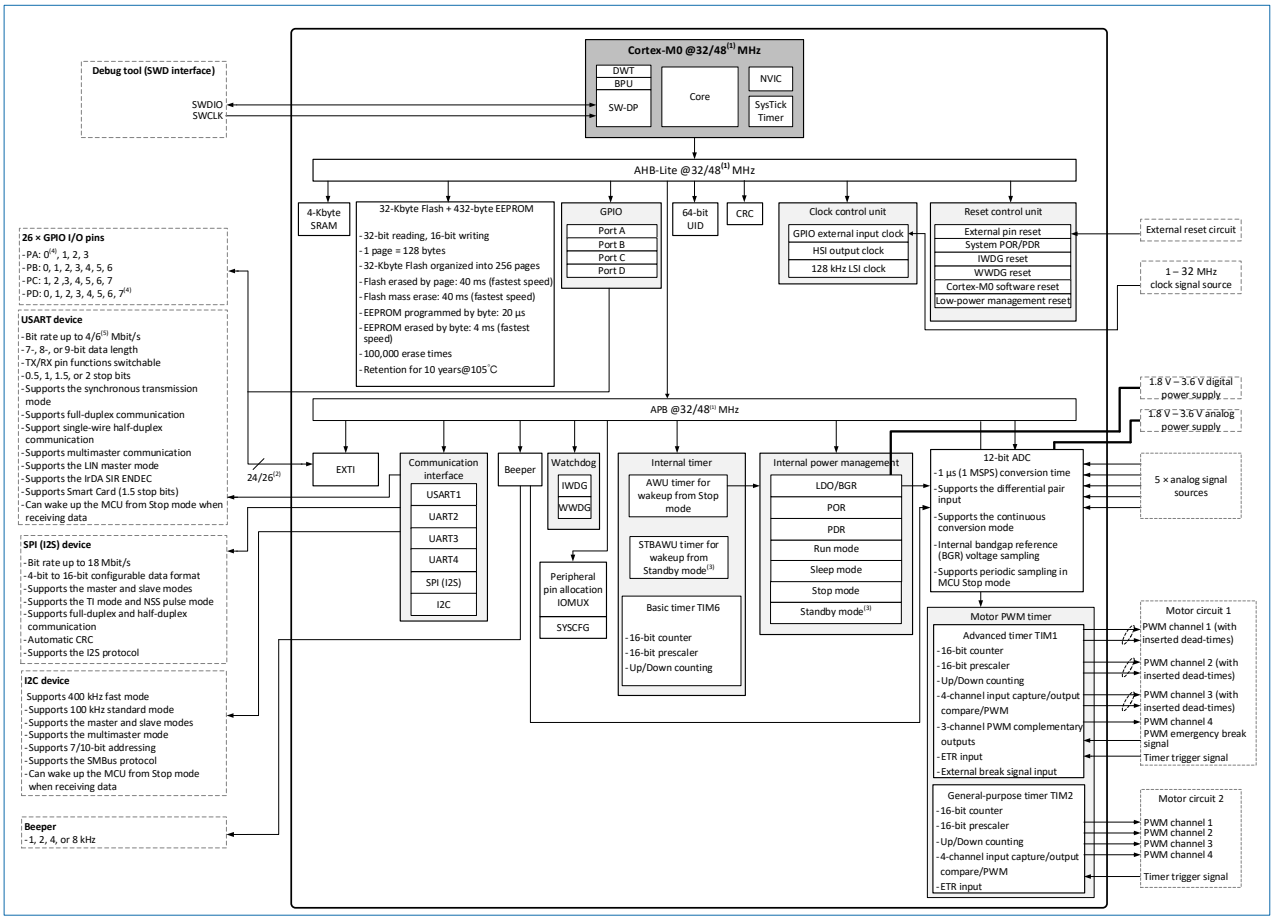


Figure 3-1 HK32F030MxxxxA/HK32F0301MxxxxA block diagram

Note:

(1). The maximum frequency of HK32F030MxxxxA and HK32F0301MxxxxA are 32MHz and 48 MHz respectively.

(2). HK32F030MxxxxA and HK32F0301MxxxxA have 24 and 26 GPIOs respectively for the connection of EXTI lines.

(3). Only HK32F0301MxxxxA supports the Standby mode.

(4). Some packages of HK32F030MxxxxA have PA0 and PD7 pins. All packages of HK32F0301MxxxxA have PA0 and PD7 pins. For details, see section "6 Pinouts and pin descriptions".

(5). The maximum USART transmission rates of HK32F030MxxxxA and HK32F0301MxxxxA are 4 Mbit/s and 6 Mbit/s respectively.

3.2 Memory mapping

The following figure shows the memory mapping of HK32F030MxxxxA/HK32F0301MxxxxA MCUs:

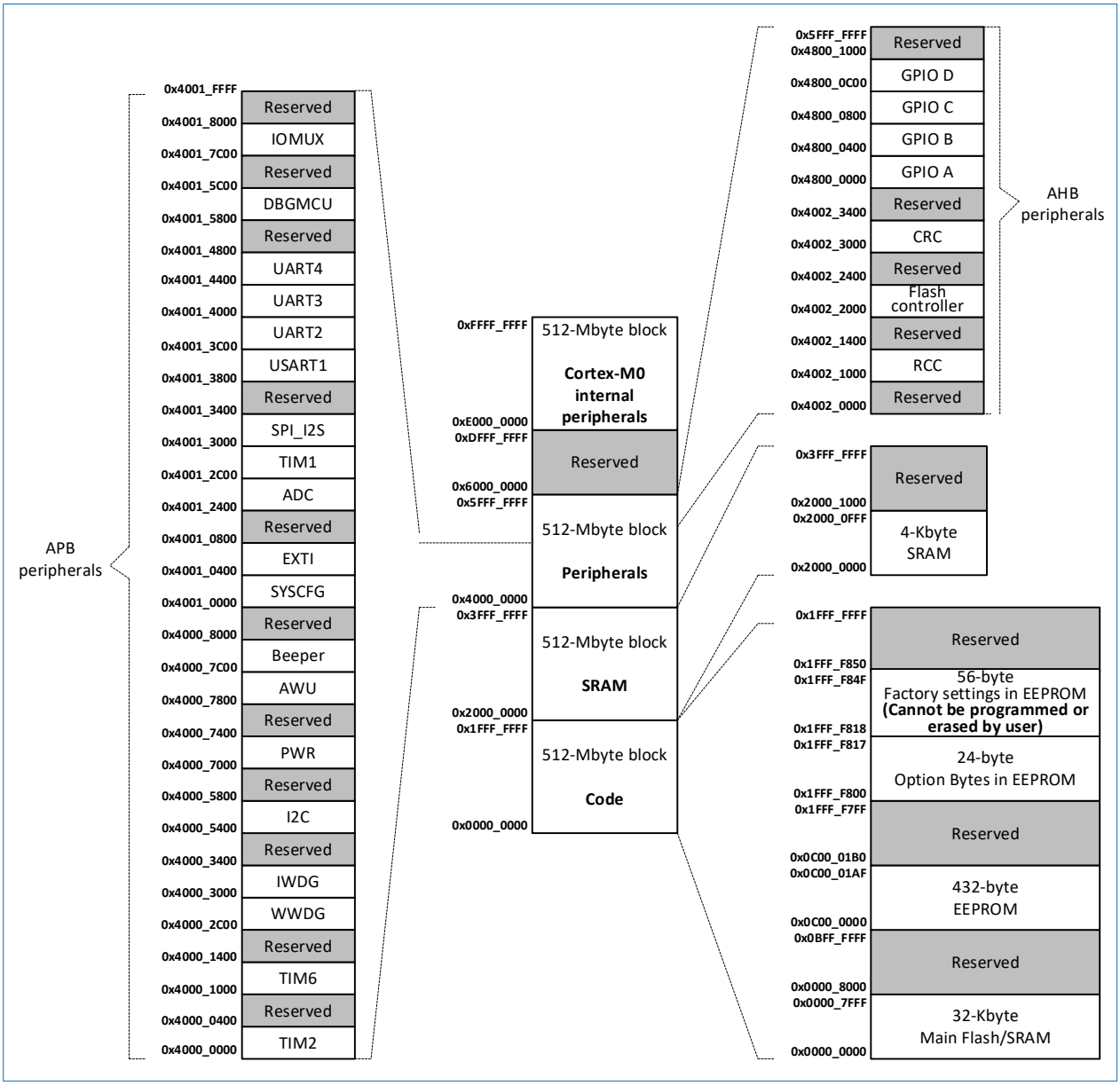


Figure 3-2 HK32F030MxxxxA/HK32F0301MxxxxA memory mapping

3.3 Memory

3.3.1 Flash

HK32F030MxxxxA/HK32F0301MxxxxA integrates a Flash memory of up to 32 Kbytes to store programs and data.

You can configure the Flash control register to remap interrupt vectors.

3.3.2 SRAM

HK32F030MxxxxA/HK32F0301MxxxxA integrates a 4-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.3.3 EEPROM

HK32F030MxxxxA/HK32F0301MxxxxA has 432 bytes of EEPROM.

3.4 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32F030MxxxxA/HK32F0301MxxxxA integrates a CRC calculation unit to reduce application processing burden and accelerate processing.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with the reference signature that is generated at link time and stored at a specified memory location.

3.5 Power supply scheme

HK32F030MxxxxA/HK32F0301MxxxxA has a single power supply. V_{DD} and V_{DDA} supply power to the digital circuitry and analog circuitry of the MCU via the same pin.

V_{DD}/V_{DDA} = 1.8 V – 3.6 V

3.6 Power supply monitor

HK32F030MxxxxA/HK32F0301MxxxxA embeds the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply is over the 1.8 V threshold. When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuits are required.

3.7 Low-power modes

HK32F030MxxxxA/HK32F0301MxxxxA supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain and the HSI oscillator are disabled. MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any external I/O pin.

- Standby mode

  In Standby mode, MCUs achieve the lowest power consumption. The internal LDO is off, so the entire 1.2 V domain is powered off. The HSI crystal oscillator is disabled. The SRAM content and register content are lost while the register content in the backup domain is retained. The Standby circuitry works as normal.

  The MCU exits from Standby mode when an external reset signal on the NRST pin, an independent watchdog (IWDG) reset, a rising edge on the WKUP pin, or an STBAWU alarm occurs. HK32F030MxxxxA/HK32F0301MxxxxA embeds four bytes of backup domain registers (PWR_SBKP0/PWR_SBKP1) that are used to store critical data in Standby mode.

Note: Only HK32F0301MxxxxA MCUs can operate in Standby mode. HK32F030MxxxxA MCUs cannot operate in Standby mode.

3.8 I/O retention

The three I/O pins PC6, PC3, and PD6 have the I/O retention function. They can be separately configured to retain the state before entering Standby mode. In the I/O retention state, all output control of the I/O is retained, including the output level, enable, pull-up/pull-down, and drive capacity. When the MCU exits the Standby mode and 0 is written to the configuration bit, the I/O retention state is released and the I/O can work normally.

3.9 STBAWU timer

HK32F030MxxxxA/HK32F0301MxxxxA integrates a standby auto-wakeup unit (STBAWU) timer. The STBAWU timer can count and generate a wakeup event to wake up the MCU from Standby mode. STBAWU is based on a 16-bit counter and uses LSI as the operating clock. The wakeup interval can be set to a value from 8 ms to 524.28s.

3.10 Resets

HK32F030MxxxxA/HK32F0301MxxxxA supports the system reset and power reset.

3.10.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain.

You can identify the reset source by checking reset status flags in the RCC_CSR register.

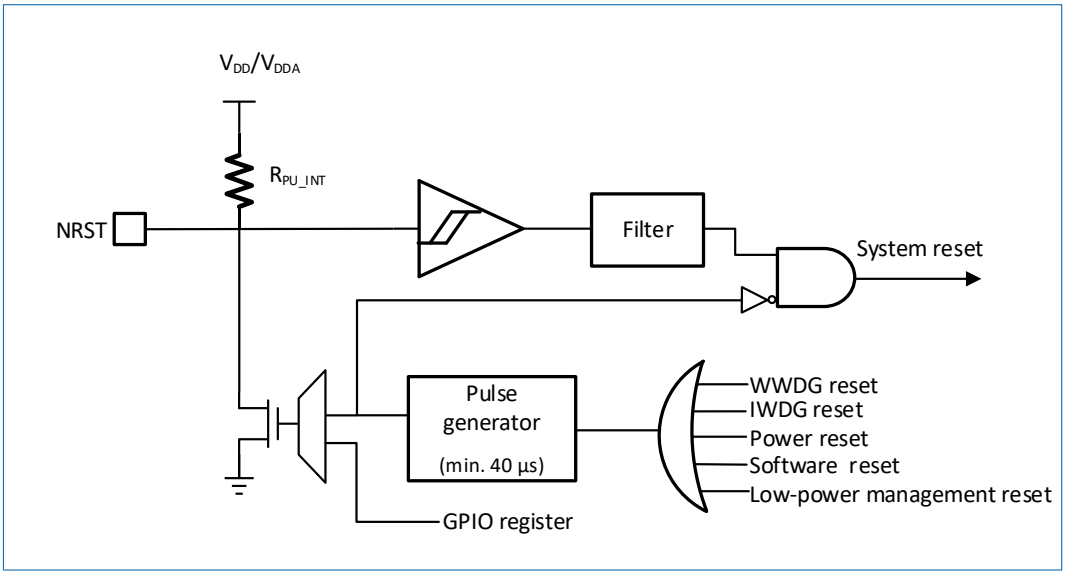


Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Power reset
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004. The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.10.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Exit from Standby mode (only HK32F0301MxxxxA)

HK32F030MxxxxA/HK32F0301MxxxxA MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the 1.8 V threshold. When V_{DD} is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

3.11 Clocks and clock tree

The following figure shows the clock tree of HK32F030MxxxxA/HK32F0301MxxxxA.

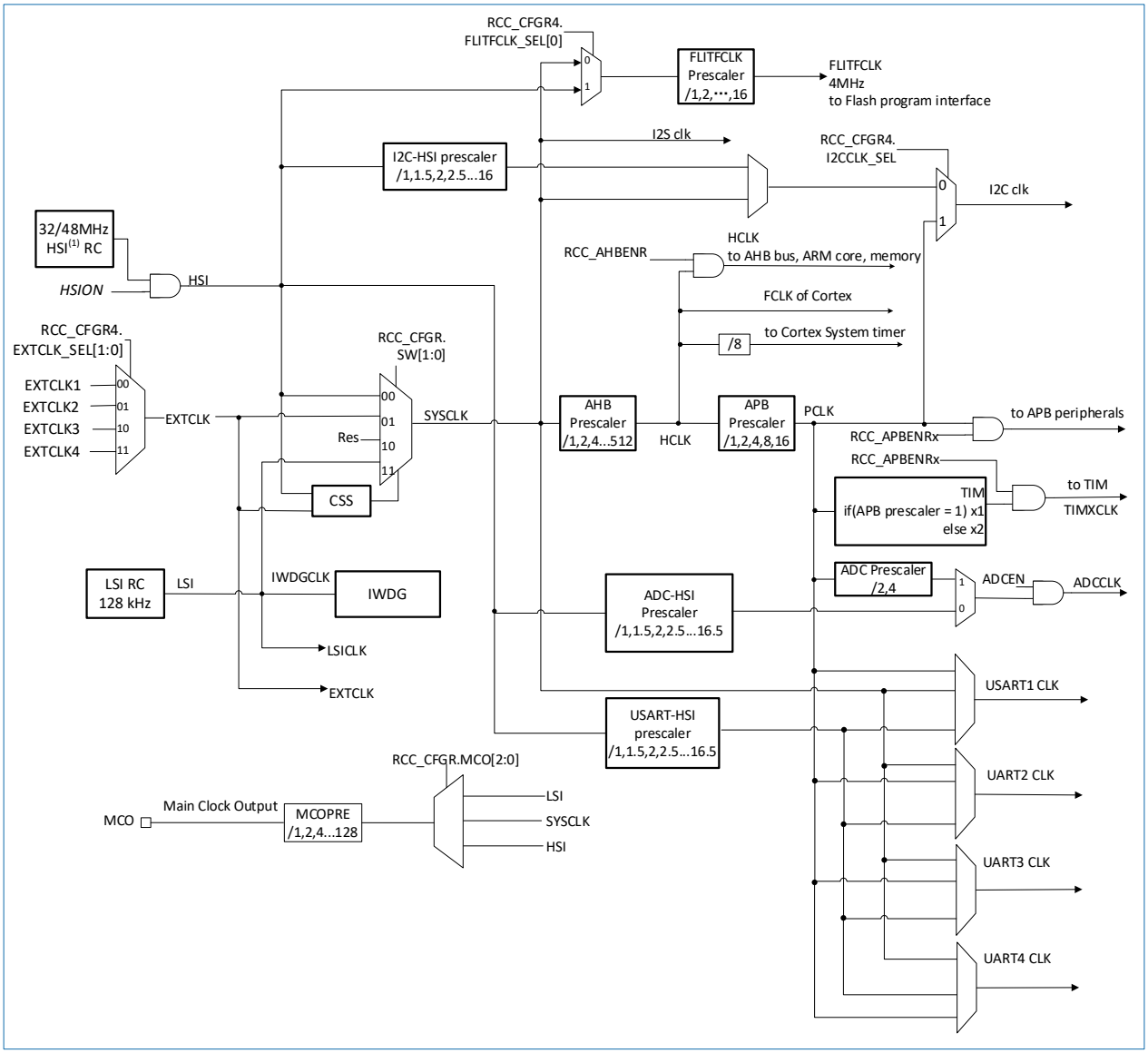


Figure 3-4 Clock tree of HK32F030MxxxxA/HK32F0301MxxxxA

Note:

(1). The HSI of HK32F030MxxxxA is 32 MHz, and the HSI of HK32F0301MxxxxA is 48 MHz.

As Figure 3-4 shows, HK32F030MxxxxA/HK32F0301MxxxxA supports the following clock sources:

- High-speed internal clock (HSI):
  - HK32F030MxxxxA: 32 MHz
  - HK32F0301MxxxxA: 48 MHz
- Low-speed internal clock (LSI): 128 kHz
- GPIO external input clock: 32 MHz (maximum value)

Each clock source can be enabled and disabled individually. The clock source not in use can be disabled to reduce power consumption. Multiple prescalers are available for the configuration of AHB and APB clock domains. The maximum clock frequency of AHB and APB clock domains is 32/48 MHz (32 MHz on HK32F030MxxxxA and 48 MHz on HK32F0301MxxxxA). The AHB clock (HCLK) divided by eight can drive the Cortex system timer (by configuring the Cortex SysTick configuration bit).

All peripheral clocks are driven by the clock (HCLK or PCLK) of the bus to which the peripheral is connected. However, there are some exceptions:

- The Flash programming interface clock (FLITFCLK) is driven by the HSI clock or SYSCLK (selected by using the software).

- I2S is driven by SYSCLK all the time.
- The clock source of I2C is one of the following (selected by using the software):
  - SYSCLK
  - 32/48 MHz HSI divided by the I2C-HSI prescaler
  - APB clock (PCLK)
- The FCLK of Cortex is provided by AHB clock (HCLK).
- AHB bus, ARM core, and memory are directly driven by AHB clock (HCLK).
- The clock source of ADC is one of the following (selected by using the software):
  - APB clock (PCLK) divided by 2 or 4 by the ADC prescaler
  - 32/48 MHz HSI divided by the ADC-HSI prescaler
- The clock source of USART1/UART2/UART3/UART4 is one of the following (selected by using the software):
  - PCLK
  - SYSCLK
  - 32/48 MHz HSI divided by the USART-HSI prescaler
- The APB clock (PCLK) or the APB clock (PCLK) multiplied by two provides the clock for timers. (The clock frequency is selected by using the software and implemented by hardware.)
- The reset and clock controller (RCC) uses the AHB clock (HCLK) divided by eight as the external clock of the Cortex SysTick timer. You can set the SysTick control/status register to select HCLK/8 as the SysTick timer clock.

3.12 SYSCFG

The HK32F030MxxxxA/HK32F0301MxxxxA MCU has a set of configuration registers that provide the following functions:

- Remap the memory areas.
- Manage the connections between external interrupts and GPIOs
- Manage the reliability feature of the system.

3.13 GPIO

Each general-purpose input/output (GPIO) pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by the digital and analog alternate functions. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.14 IOMUX

In small packages (such as SOP8 and TSSOP16), the mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX. The following example illustrates how to use IOMUX to remap functions to pins on a SOP8 package.

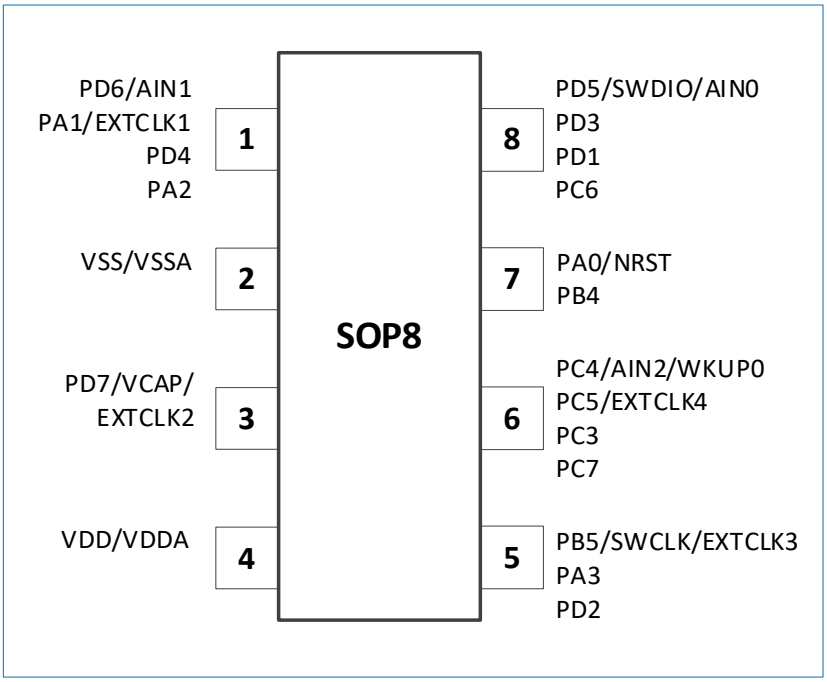


Figure 3-5 SOP8 package pinout

As Figure 3-5 shows, after the reset of the MCU, pin 8 is assigned with PD5 by default. You can configure the IOMUX register to remap pin 8 to PD3, PD1, or PC6.

By configuring IOMUX, you can use 18 GPIOs and all internal peripheral I/Os in SOP8 and TSSOP16 packages.

3.15 Interrupts and events

3.15.1 NVIC

HK32F030MxxxxA/HK32F0301MxxxxA incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 24 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities while maintaining the lowest interrupt latency.

- The NVIC closely coupled with the core interface ensures low latencies in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instructions needed.

3.15.2 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.15.3 EXTI

The extended interrupt/event controller (EXTI) manages 12 interrupt lines that are used to generate

interrupt/event requests and wake up the system through edge detection. The trigger event of each EXTI line can be configured and masked independently. The trigger event can be a rising edge, a falling edge, or both. The pending register stores the status of each interrupt request. EXTI can detect external interrupt line signals whose pulse width is shorter than the internal clock period. Among the 12 EXTI lines, up to eight are external EXTI lines.

The EXTI lines from EXTI 0 to EXTI 7 are connected to I/O pins. The connections of the other EXTI lines are as follows:

- EXTI line 8 connected to the ADC AWD event
- EXTI line 9 connected to the USART wakeup event
- EXTI line 10 connected to the I2C wakeup event
- EXTI line 11 connected to the AWU wakeup event

EXTI lines from 8 to 10 are connected to internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). EXTI lines from 8 to 10 can only detect the rising edge of events in Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system. The corresponding interrupt control bit and status bit are stored in the peripheral from which events are generated.

3.16 ADC

The ADC of HK32F030MxxxxA/HK32F0301MxxxxA has the following features:

- A total of six channels. AIN0 to AIN4 are external channels connected to I/Os. AIN5 is an internal channel connected to the internal reference voltage.
- Supports the differential pair input mode. AIN0-AIN1 and AIN2-AIN3 form two differential pairs. (When ADC is configured to the differential pair input mode, AIN4 and the ADC channel for the sampling of the internal BGR voltage are unavailable.)
- Supports only the 12-bit ADC sampling resolution.
- Supports the analog watchdog (AWD) wakeup function in Stop mode.

3.16.1 AWD wakeup function

In Stop mode, the beeper counts and sends a signal to the ADC. The ADC samples the signal and wakes up the ADC clock. Then the ADC clock triggers an ADC conversion and generates an AWD event according to the ADC conversion result. Then the AWD event is sent to an EXTI line to wake up the system.

To use the AWD wakeup function, you need to configure not only the related threshold and channel, but also the ADC_CR2.WAKE_EN register, beeper internal counting control register, and ADC wakeup enable register.

3.17 Timers

The HK32F030MxxxxA/HK32F0301MxxxxA MCU has an advanced timer, a general-purpose timer, and a basic timer. The following table describes the functions of timers.

Table 3-1 Features of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	1 to 65536	No	Yes	4	3
General-purpose timer	TIM2	16-bit	Up, down, up/down	1 to 65536	No	No	4	No
Basic timer	TIM6	16-bit	Up, down	1 to 65536	No	No	No	No

3.17.1 Advanced timer

HK32F030MxxxxA/HK32F0301MxxxxA integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of the advanced timer can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output
- Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). Many functions of TIM1 are the same as those of the general-purpose timer. Therefore, TIM1 can work together with the general-purpose timer through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

3.17.2 General-purpose timer

HK32F030MxxxxA/HK32F0301MxxxxA integrates a 4-channel general-purpose timer TIM2.

TIM2 can generate PWM outputs or serve as a simple time base. TIM2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. In debug mode, the counter can be frozen.

TIM2 can work with the advanced timer through the Timer Link feature for synchronization and event chaining. Additionally, TIM2 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors.

3.17.3 Basic timer

HK32F030MxxxxA/HK32F0301MxxxxA integrates a basic timer TIM6.

TIM6 embeds a 16-bit up/down counter and a 16-bit prescaler. It is used to generate periodic CPU interrupt requests. In debug mode, the counter can be frozen.

3.18 AWUT

HK32F030MxxxxA/HK32F0301MxxxxA provides an auto-wakeup timer (AWUT). The AWUT can count and generate an interrupt to wake up the MCU from Stop mode. An ultra-low-power 22-bit counter is embedded in the AWUT. The operating clock of AWUT can be the GPIO input clock or the low-speed internal (LSI) clock. The AWUT adopts the down-counting mode.

3.19 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent RC oscillator (LSI). The RC oscillator is independent of the main clock, so it can operate in Stop and Standby modes. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use IWDG in window mode.

3.20 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the

main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.21 I2C bus

The I2C bus interface can work as a master or slave and supports the standard and fast modes. The I2C bus interface supports the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interface embeds hardware CRC generation/verification and supports SMBus V2.0/PMBus.

Table 3-2 I2C features

I2C Feature	I2C
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast/Fast mode plus	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

3.22 USART/UART

One universal synchronous/asynchronous receiver/transmitter (USART1) and three universal asynchronous receivers/transmitters (UART2/3/4) are embedded in each HK32F030MxxxxA/HK32F0301MxxxxA MCU. They can communicate at up to 6 Mbit/s. USART/UARTs provide hardware management of multiprocessor communication mode, master synchronous communication, and single-wire half-duplex communication mode. This module also supports Smart Card communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability, and automatic baud rate detection. The USARTs have a clock domain independent of the CPU clock, so they can wake up the MCU from Stop mode.

Table 3-3 USART/UART features

USART Mode/Feature	USART1	UART2/UART3/UART4
Data word length	8/9-bit	7/8/9-bit
Multiprocessor communication	Supported	Supported
Synchronous mode	Supported	Not supported
Single-wire half-duplex communication	Supported	Supported
Dual clock domains and wakeup from Stop mode	Supported	Not supported
Automatic baud rate detection	Supported	Not supported
Modbus communication	Supported	Not supported
RS232 hardware flow control	Not supported	Not supported
RS485 driver enable	Not supported	Not supported
IrDA SIR ENDEC	Supported	Not supported
LIN mode	Supported	Not supported
Smart Card mode	Supported	Not supported

3.23 SPI/I2S

HK32F030MxxxxA/HK32F0301MxxxxA has a serial peripheral interface (SPI) communicating at up to 18 Mbit/s. The SPI interface can work as the master or slave and supports full-duplex and half-duplex communication. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4-bit to 16-bit. The SPI interface supports the CRC and TI modes. The following table lists the features of the SPI interface.

Table 3-4 SPI features

SPI Feature	SPI1
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
I2S mode	Supported
TI mode	Supported

The standard I2S interface (with SPI multiplexed) provides four types of audio standards and supports half-duplex communication in master or slave mode. The I2S interface has dedicated signals for data synchronization. The data format can be 16-bit, 24-bit, or 32-bit and the I2S interface can operate with 16- or 32-bit resolution. The I2S interface can be set to an audio sampling frequency from 8 kHz to 192 kHz by the 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components. The I2S interface supports the half-duplex communication and master/slave mode. The following table lists the features of the I2S interface.

Table 3-5 I2S features

I2S Feature	I2S1
Half-duplex mode	Supported
Master/Slave mode configurable	Supported
8-bit programmable linear prescaler	Supported
Data format programmable	Supported
Clock polarity programmable	Supported
I2S protocol	Supported
Driving external audio components	Supported

3.24 Beeper

An ultra-low-power 7-bit timer is embedded in the beeper. The operating clock of the timer can be the GPIO external input clock or the 128 kHz low-speed internal (LSI) clock. The timer adopts the down-counting mode and can output 1 kHz, 2 kHz, 4 kHz, or 8 kHz pulses.

In Stop mode, the beeper keeps operating and can trigger ADC sampling periodically. The frequency at which ADC sampling is triggered is 1/1024 of the frequency of the pulse output by the beeper. For example, if the beeper outputs 1 kHz pulses, ADC sampling is triggered at a frequency of 1 kHz/1024 ≈ 0.98 Hz (at an interval of about 1.02s).

3.25 64-bit UID

The 64-bit unique identifier (UID) provides a reference number for each HK32F030MxxxxA/HK32F0301MxxxxA MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 64-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) as needed. The 64-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process that has a security mechanism.

3.26 Debug port

Based on the ARM SWJ-DP embedded in HK32F030MxxxxA/HK32F0301MxxxxA, SWDIO and SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	3.8	V
V_{IN}	Input voltage on pins	–0.3	3.8	
$\|V_{SSX} – V_{SS}\|$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	105	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	40	
	Output current sourced by any I/O and control pin	40	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–45	130	°C
T_J	Maximum junction temperature	–45	130	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions of HK32F030MxxxxA

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	32	
V_{DD}	Standard operating voltage	1.8	3.6	V
V_{DDA}(1)	Analog operating voltage	1.8	3.6	V
T_A	Operating temperature	–40	105	°C

Table 4-5 Recommended operating conditions of HK32F0301MxxxxA

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	48	
V_{DD}	Standard operating voltage	1.8	3.6	V
V_{DDA}(1)	Analog operating voltage	1.8	3.6	V
T_A	Operating temperature	–40	105	°C

(1). V_{DDA} is connected to V_{DD} on the chip.

4.2.2 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge	1.58	1.67	1.78	V
		Rising edge	1.7	1.76	1.88	V
$V_{PDRhyst}$	PDR hysteresis	-	22	92	185	mV
$t_{RSTTEMPO}$(2)	Reset duration	-	-	2	-	ms

(1). PDR and POR are based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.3 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ(2)	Max	Unit
V_{REFINT}(1)	Internal reference voltage	–40°C to 105°C V_{DD} or V_{DDA} = 3.3 V	0.75	0.8	0.87	V
$Ripple_{REFINT}$(3)	Fluctuation of reference voltage in full temperature range	–40°C to 105°C V_{DD} or V_{DDA} = 3.3 V	0.096	-	3.188	%

(1). The actual test results of multiple samples after trimming.

(2). The target trimming value.

(3). The actual test results of multiple samples when the temperature is 20°C.

4.2.4 Operating current characteristics

Table 4-8 Operating current characteristics of HK32F030MxxxxA

Mode	Condition	V_{DD} = 3.3 V			Unit
		–40°C	25°C	105°C	
Run mode	HCLK = HSI (32 MHz); All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled**; Two wait states to access Flash.	5.036	5.111	5.631	mA
Sleep mode	HCLK = 32 MHz; AHB/APB disabled; Clocks in the core domain disabled; All I/Os configured in high impedance; SRAM and Flash data retained, other peripherals disabled.	1.993	2.089	2.566	mA
Stop mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO operating in low-power mode; All I/Os configured in high impedance; AWU **enabled**, other peripherals disabled.	500	565	951	μA
Low-power Stop mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO operating in low-power mode;	231	298(1)/ 30(2)	638	μA

Mode	Condition	V_{DD} = 3.3 V			Unit
		–40°C	25°C	105°C	
	All I/Os configured in high impedance; AWU **disabled**, all the other peripherals disabled.				

(1). When the rising edge on the NRST pin is shorter than 800 µs, the test result in low-power Stop mode is about 298 µA.

(2). When the rising edge on the NRST pin is longer than 800 µs, the test result in low-power Stop mode is about 30 µA.

Table 4-9 Operating current characteristics of HK32F0301MxxxxA

Mode	Condition	V_{DD} = 3.3 V			Unit
		–40°C	25°C	105°C	
Run mode	SYSCLK = HSI (48 MHz); All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled**; Two wait states to access Flash.	5.037	5.111	5.632	mA
Sleep mode	SYSCLK = 48 MHz; AHB/APB disabled; Clocks in the core domain disabled; All I/Os configured in high impedance; SRAM and Flash data retained, other peripherals disabled.	1.993	2.089	2.566	mA
Stop mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO operating in low-power mode; All I/Os configured in high impedance; AWU **enabled**, other peripherals disabled.	500	565	951	µA
Low-power Stop mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO operating in low-power mode; All I/Os configured in high impedance; AWU **disabled**, all the other peripherals disabled.	231	298(1)/ 30(2)	638	µA
Standby mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO power supply disabled; PDR of Standby circuitry **disabled**; All I/Os configured in high impedance; Power supply to backup registers and Standby circuitry kept, all the other peripherals disabled, SRAM and register content lost.	0.02	0.03	1.14	µA

(1). When the rising edge on the NRST pin is shorter than 800 µs, the test result in low-power Stop mode is about 298 µA.

(2). When the rising edge on the NRST pin is longer than 800 µs, the test result in low-power Stop mode is about 30 µA.

4.2.5 HSI clock characteristics

Table 4-10 HSI clock characteristics of HK32F030MxxxxA

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-		-	32	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-		45	-	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user		-	1	-	%
		Factory calibrated	T_A = –40°C to +105°C	–0.5	-	1.5	
$T_{su\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		-	6	-	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	32 MHz, V_{DD} = 3.3 V		-	120	-	µA

Table 4-11 HSI clock characteristics of HK32F0301MxxxxA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	48	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-	45	-	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	-	1	-	%
		Factory calibrated T_A = –40°C to +105°C	–0.5	-	1.5	
$T_{su\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	6	-	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	48 MHz, V_{DD} = 3.3 V	-	120	-	µA

(1). The value is guaranteed in design.

4.2.6 LSI clock characteristics

Table 4-12 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	128	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	10	15	µs
$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	5	8	µA

(1). The value is guaranteed in design.

4.2.7 GPIO external input clock characteristics

Clocks can be input from PA1, PD7, PB5, and PC5. The following table lists the requirements for input clocks:

Table 4-13 Characteristics of the input clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ext_clk}	External clock source frequency	-	-	-	32	MHz
$DuCy_{(HSE)}$(1)	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.8 EEPROM characteristics

Table 4-14 EEPROM characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	Half word programming time	-	120	-	µs
T_{ERASE}	Byte erase time	-	8	-	ms
N_{END}	Endurance	Supports about 100,000 cycles of erase, read, and write operations, or a service life of 10 years. (The shorter one prevails.)			

4.2.9 Flash memory characteristics

Table 4-15 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	Half word programming time	-	120	-	µs
T_{ERASE}	Page erase time	60	80	100	ms
	Mass erase time	60	80	100	ms
I_{DDPROG}	Half word programming current	-	-	5	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	2	mA
I_{DDREAD}	Read current@24 MHz	-	2	3	mA
	Read current@1 MHz	-	0.25	0.4	mA
N_{END}	Erasure endurance	100	-	-	1k cycles
t_{RET}	Data retention	10	-	-	Years

4.2.10 I/O pin input characteristics

Table 4-16 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	0.65 × V_{DD}	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	1.8	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.6	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	200	-	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V; 0 < V_{IN} < 3.3 V	-	5	-	nA
		V_{DD} = 3.3 V; V_{IN} = 5 V	-	5	-	nA
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The value is guaranteed in design.

4.2.11 I/O pin output characteristics

Table 4-17 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	2.4	-	-	V
V_{OL}	Output low level voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4	V

4.2.12 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuits.

Table 4-18 NRST pin input characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{Noise}	Low level ignored duration	-	-	80	ns

4.2.13 TIM characteristics

Table 4-19 TIM characteristics (1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency	-	$f_{TIMxCLK}$/2	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 32 MHz (HK32F030MxxxxA)/48 MHz (HK32F0301MxxxxA).

4.2.14 ADC characteristics

Table 4-20 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when ADC is enabled	-	1.8	3.3	3.6	V
VREFP	Positive reference voltage	-	1.8	3.3	3.6	V
VREFN	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	16	32	MHz
f_S (1)	Sampling frequency	f_{ADC} = 12 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 12 MHz	-	-	823	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	VREFN	-	VREFP	V
R_{AIN} (1)	External input impedance	For details, see Table 4-21.				kΩ
R_{ADC} (1)	Sample switch resistance	-	-	-	1	kΩ
C_{ADC} (1)	Sample and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC	-	-	1	-	Cycles

Item	Description	Condition	Min	Typ	Max	Unit
	conversions					
t_S(1)	Sampling time	f_{ADC} = 12 MHz	-	1.5	-	Cycles
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz 12-bit resolution		14		Cycles

(1). The value is guaranteed in design.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-21 Maximum input impedance values (f_{ADC} = 12 MHz)

Sampling Cycles (Cycles)	Sampling Time tS (μs)	Maximum Input Impedance (kΩ)
1.5	0.13	1.58
7.5	0.63	11.88
13.5	1.13	22.19
28.5	2.38	47.95
41.5	3.46	70.28
55.5	4.63	94.32
71.5	5.96	121.80
239.5	19.96	410.34

Table 4-22 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	V_{DD} = V_{DDA} = 3.3 V f_{ADC} = 12 MHz Test after ADC calibration	-	8	LSB
EO	Offset error(2)		-	5	
EG	Gain error(3)		-	8	
ED	Differential linearity error(4)		-	2	
EL	Integral linearity error(5)		-	3	

(1). Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3). Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4). Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5). Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With the restricted V_{DDA}, frequency, and temperature range, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

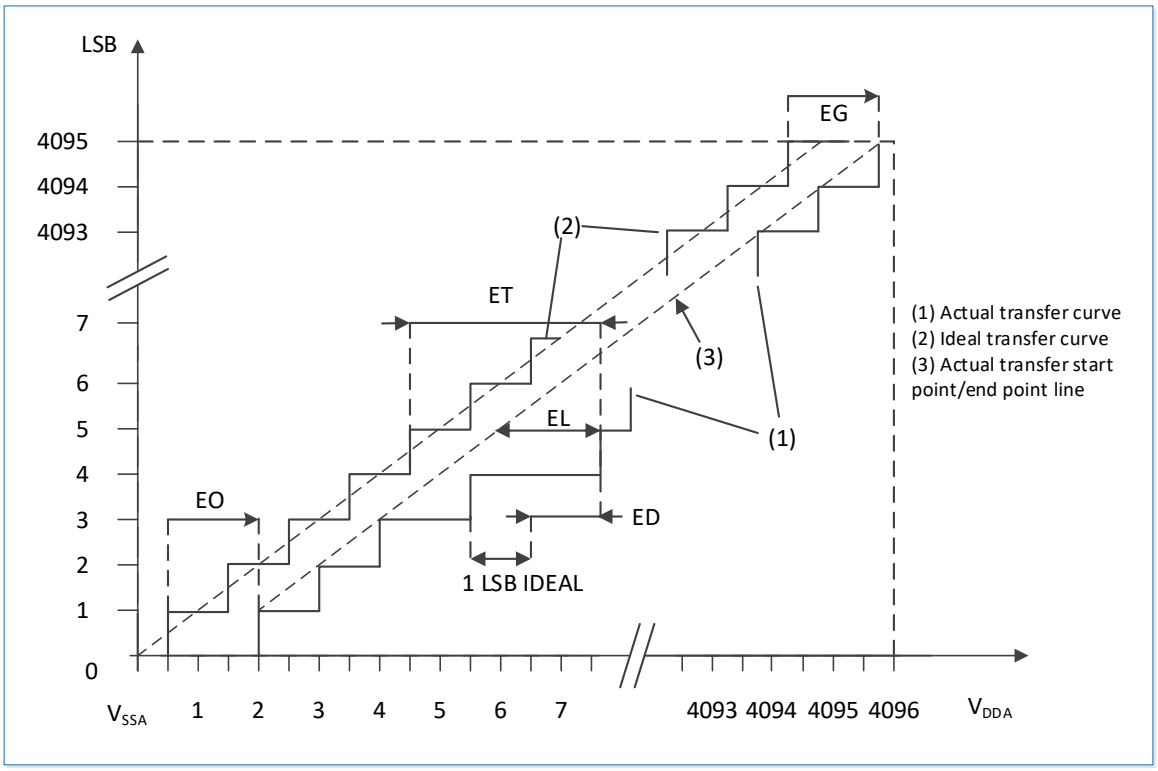


Figure 4-1 ADC accuracy characteristics

Note: For the explanations of EO, ET, EG, EL, and ED, see Table 4-22.

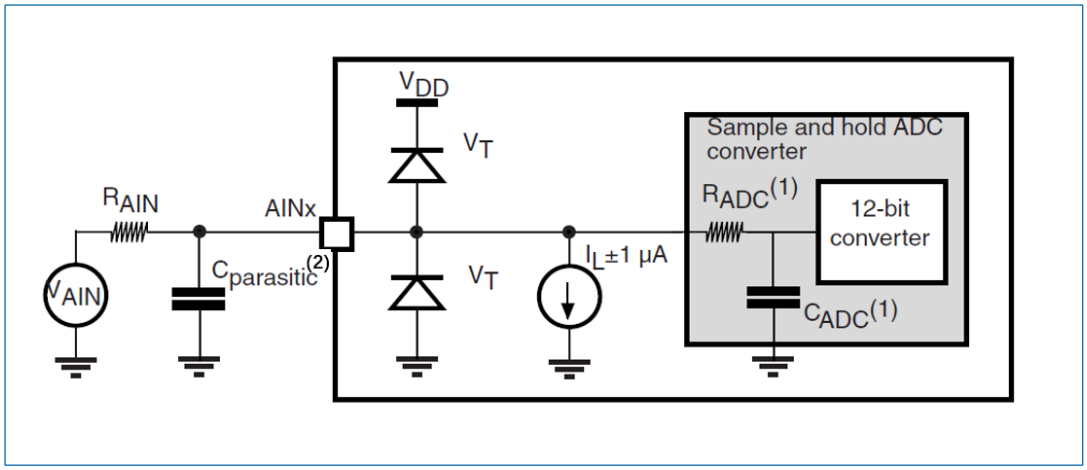


Figure 4-2 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-20.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

5 Typical circuitry

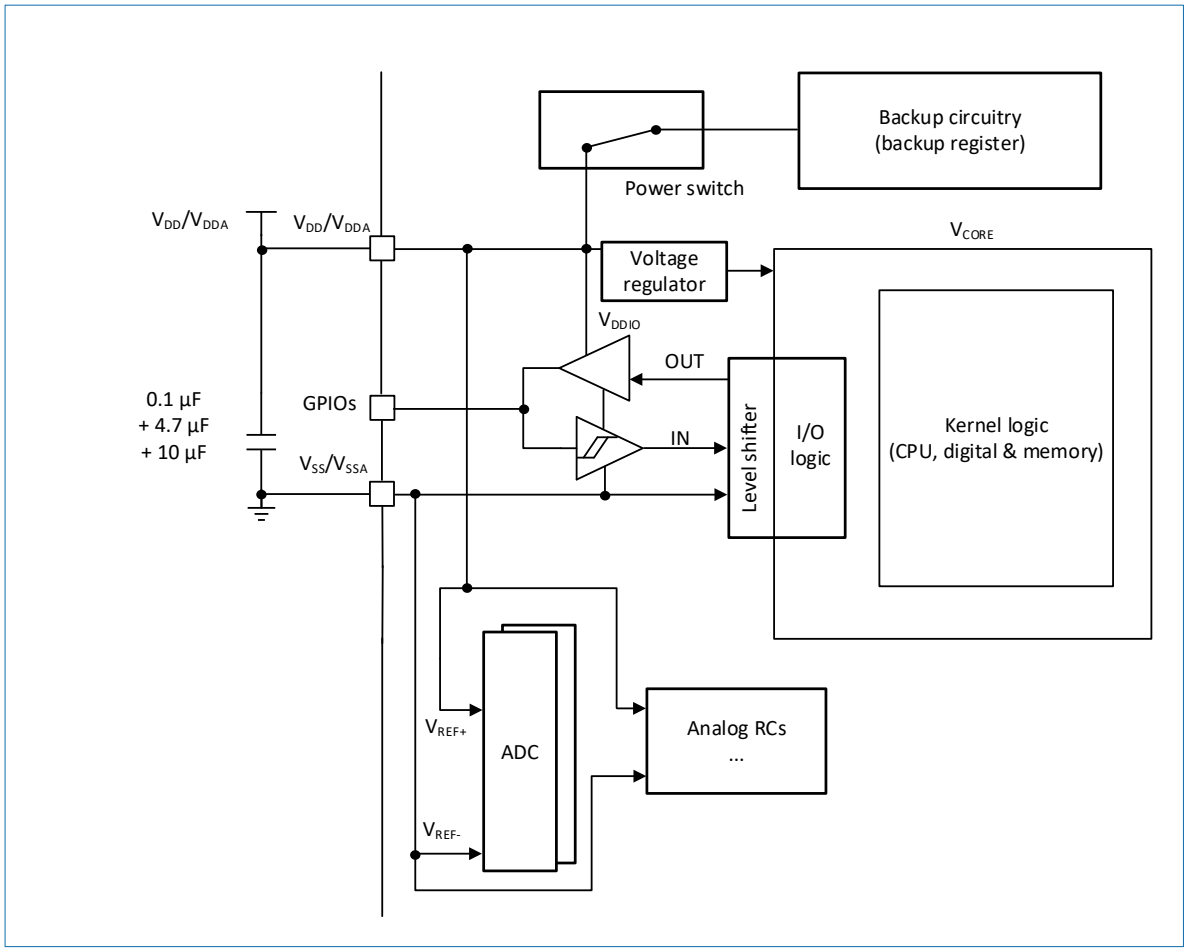
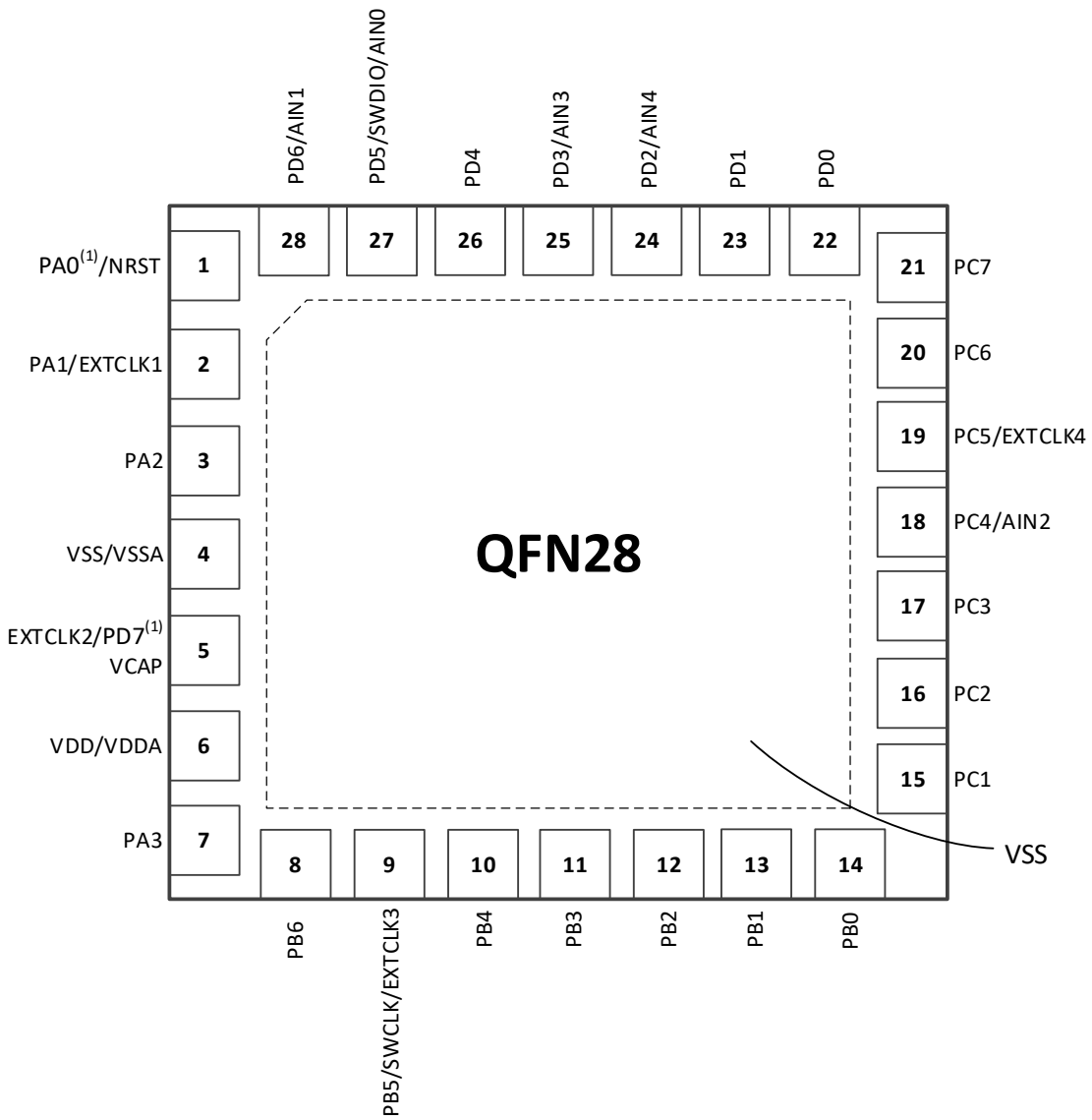


Figure 5-1 Power supply reference circuitry

6 Pinouts and pin descriptions

HK32F030MxxxxA/HK32F0301Mxxxx MCUs are delivered in QFN28, QFN24, QFN20, TSSOP28, TSSOP24, TSSOP20, TSSOP16, and SOP8 packages. This chapter describes the pinout and pin description of each package.

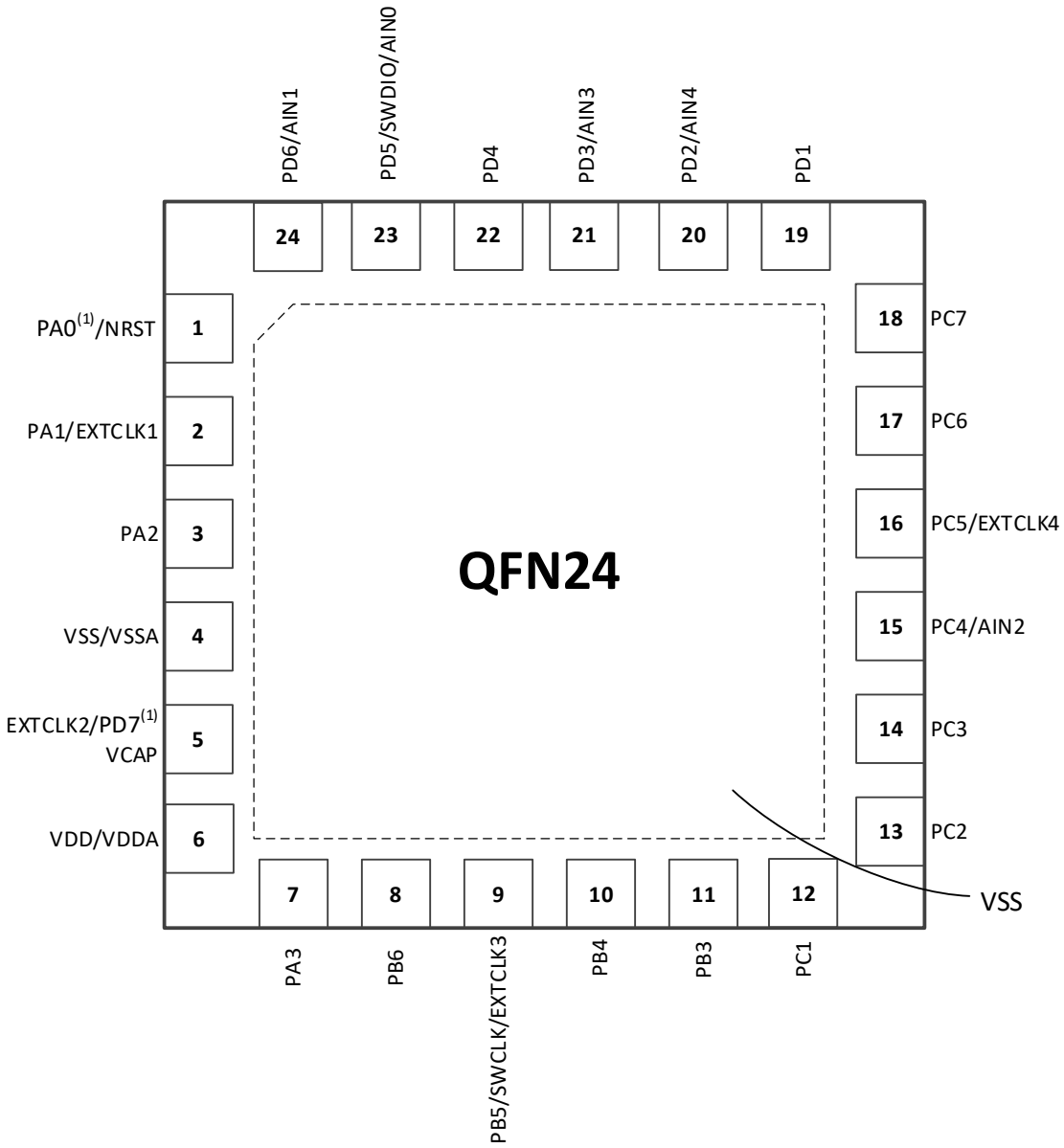
6.1 QFN28



(1). This package of HK32F030MxxxxA series does not have PD7 and PA0 pins.

Figure 6-1 QFN28 package pinout

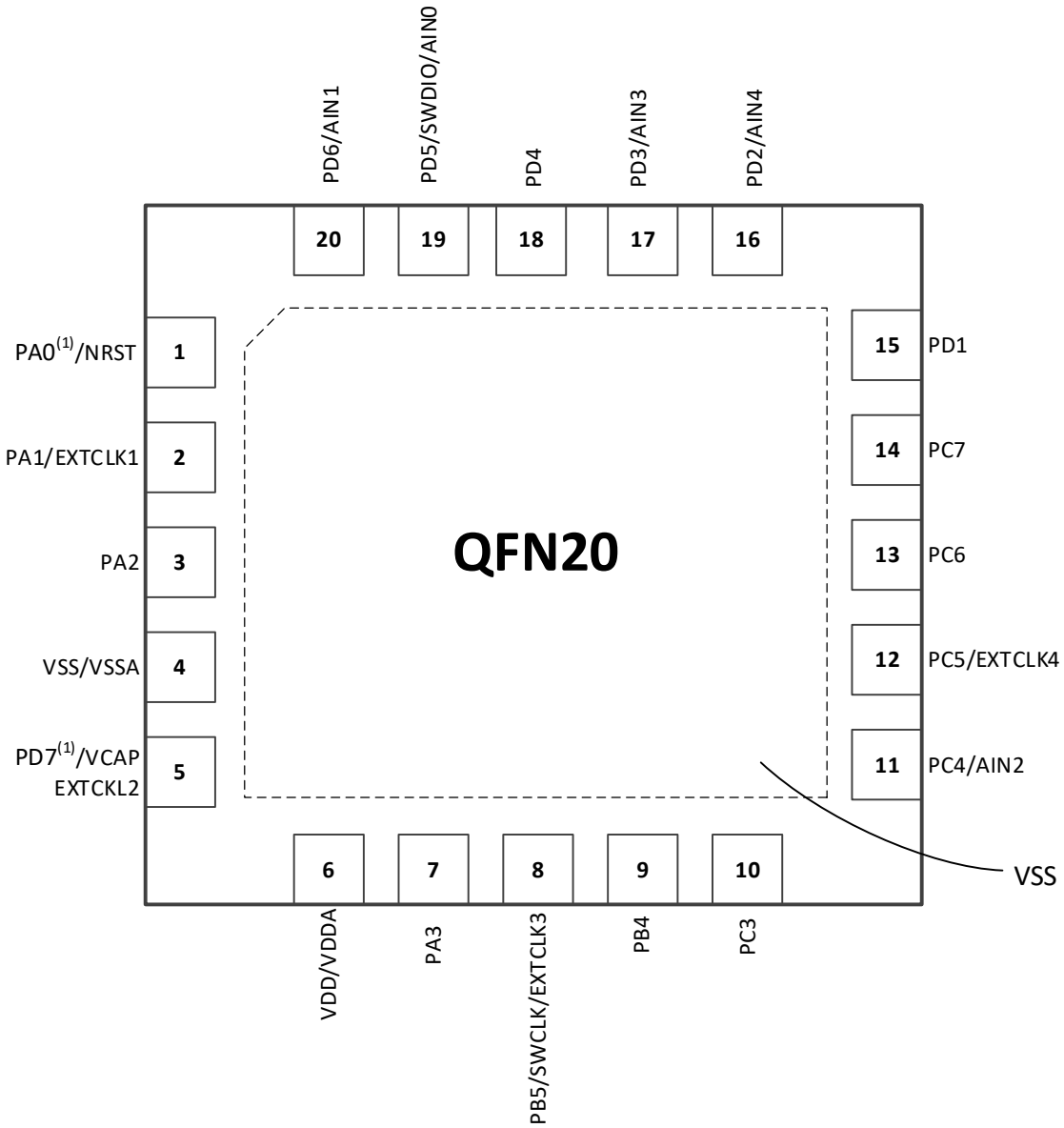
6.2 QFN24



(1). This package of HK32F030MxxxxA series does not have PD7 and PA0 pins.

Figure 6-2 QFN24 package pinout

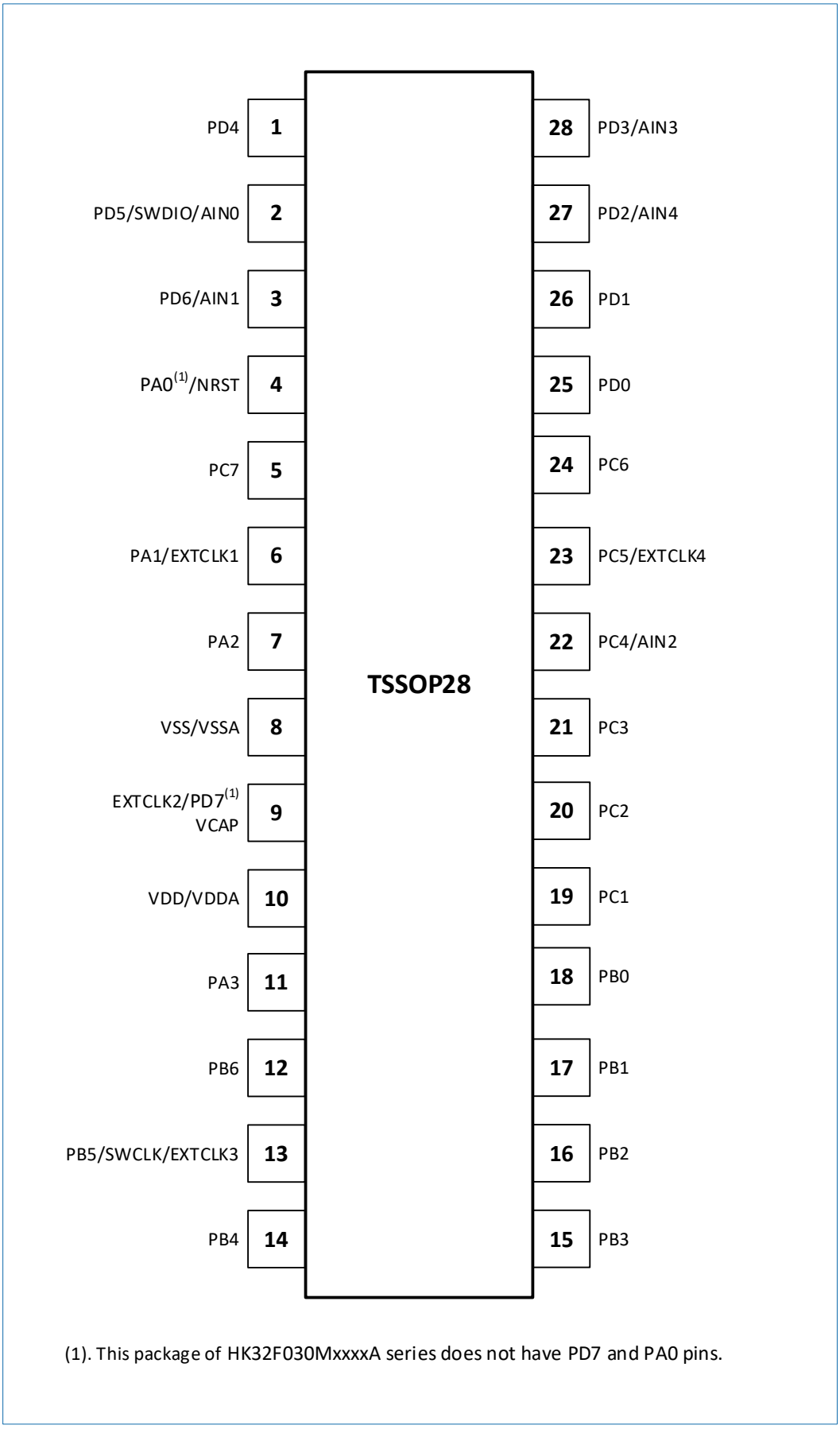
6.3 QFN20



(1). This package of HK32F030MxxxxA series does not have PD7 and PA0 pins.

Figure 6-3 QFN20 package pinout

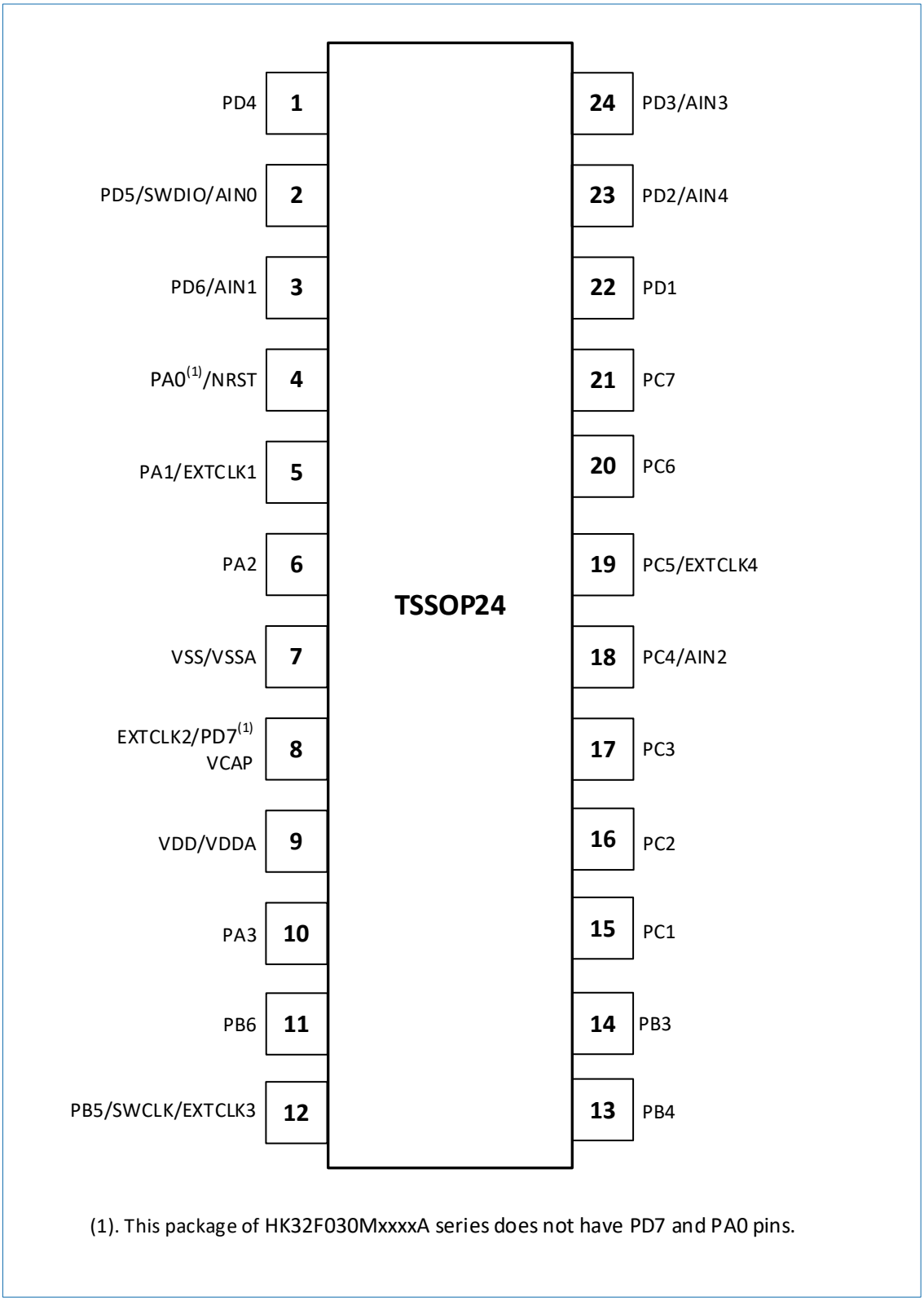
6.4 TSSOP28



(1). This package of HK32F030MxxxxA series does not have PD7 and PA0 pins.

Figure 6-4 TSSOP28 package pinout

6.5 TSSOP24



(1). This package of HK32F030MxxxxA series does not have PD7 and PA0 pins.

Figure 6-5 TSSOP24 package pinout

6.6 TSSOP20

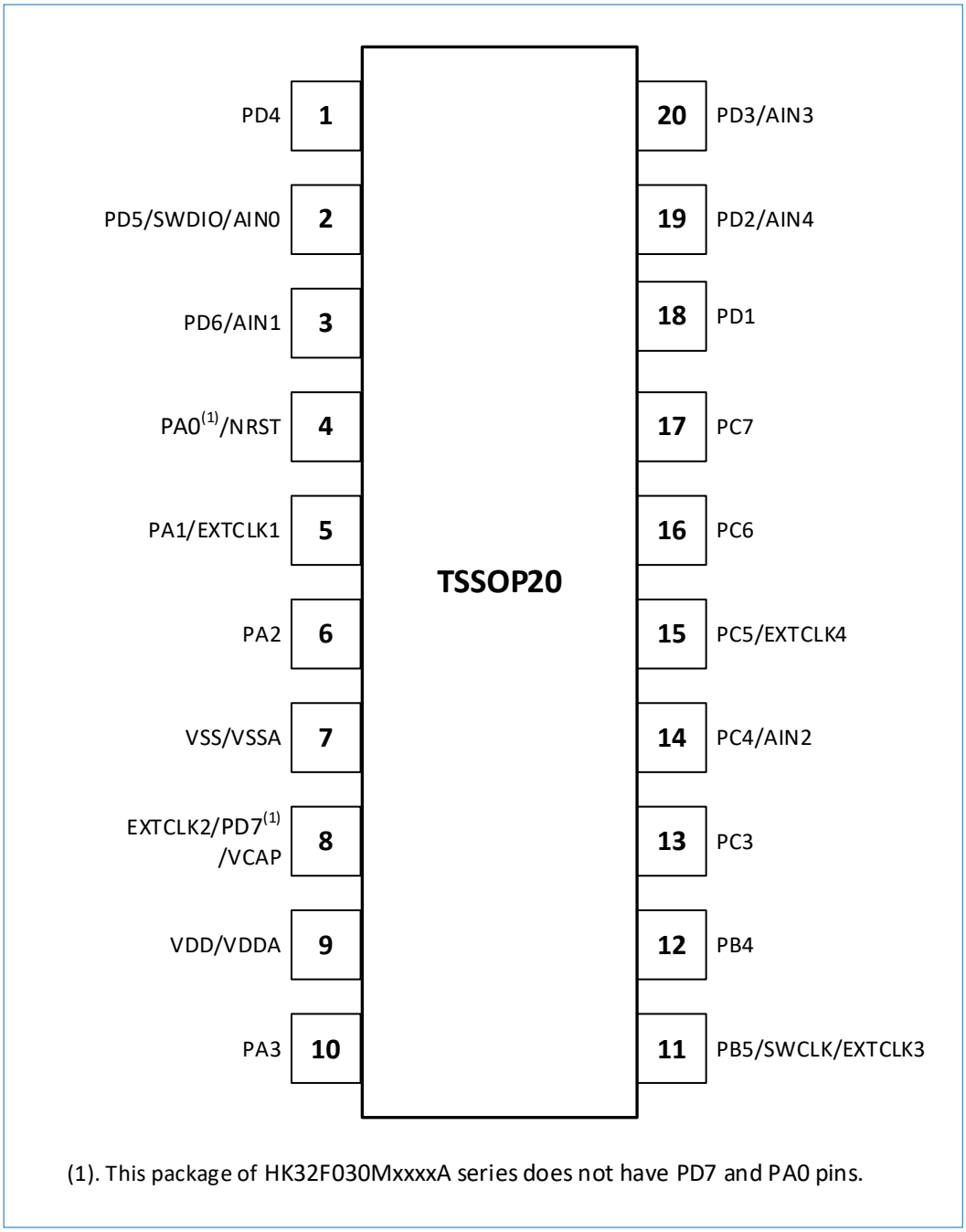


Figure 6-6 TSSOP20 package pinout

6.7 TSSOP16

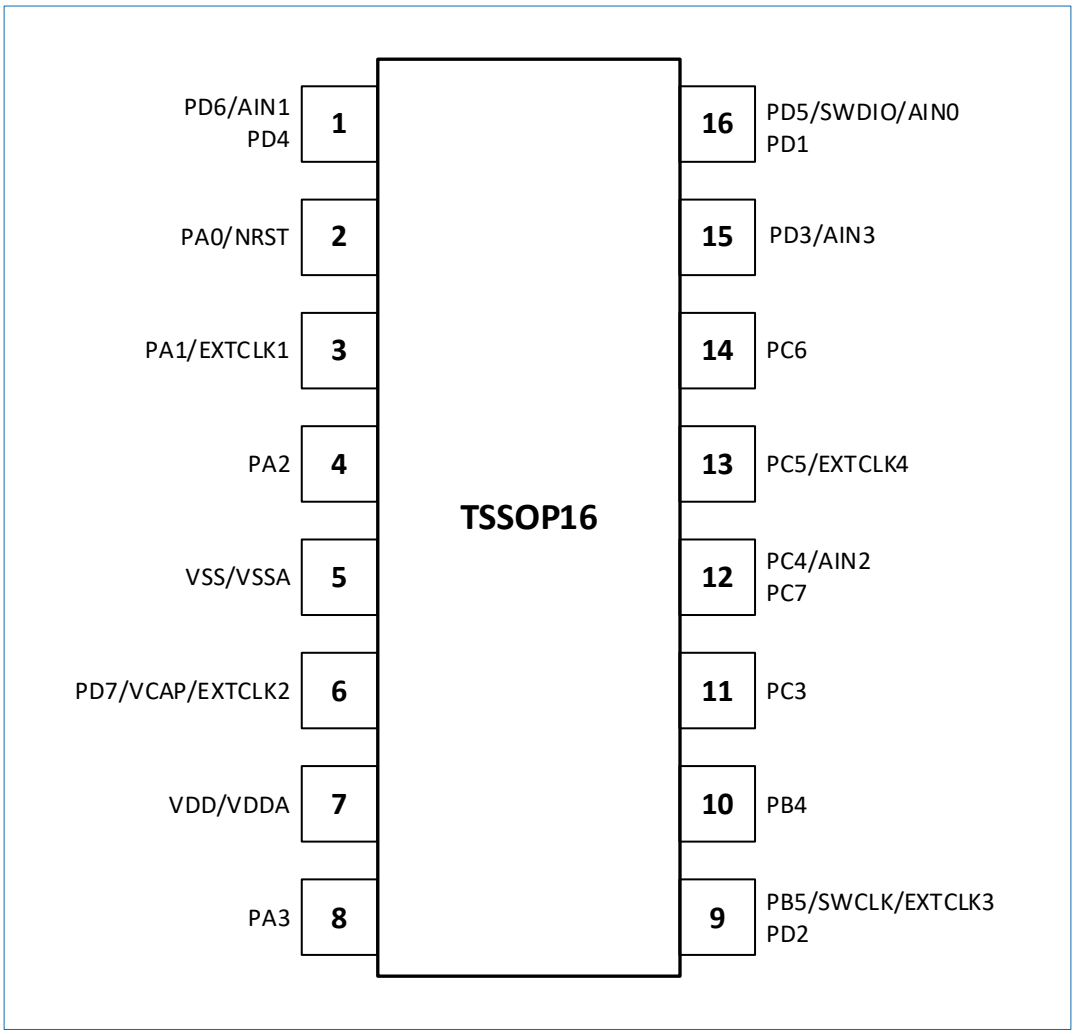


Figure 6-7 TSSOP16 package pinout

6.8 SOP8

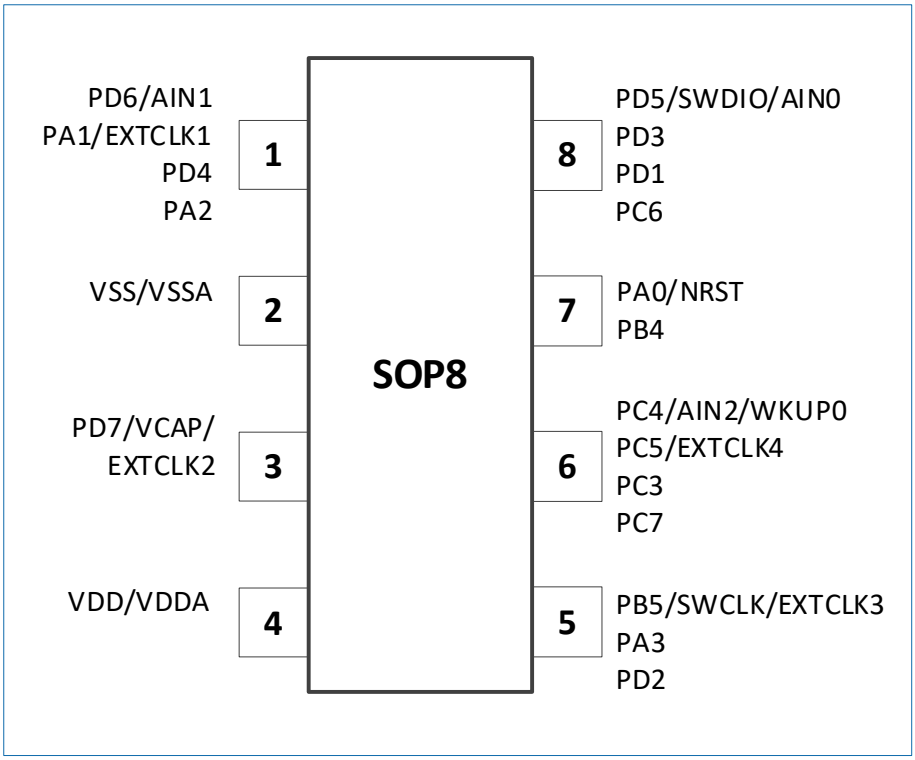


Figure 6-8 SOP8 package pinout

6.9 Pin descriptions

Table 6-1 Pin description of each package

Pin No.								Pin Name (Default Function After Resets)(1)	Pin Type(2)	5-V Tolerant	Pin Functions	
QFN28	QFN24	QFN20	TSSOP28	TSSOP24	TSSOP20	TSSOP16	SOP8				Alternate Function	Additional Function
0	0	0	-	-	-	-	-	VSS	S	-	Ground (Pin 0 is the thermal pad on the QFN package bottom.)	
1	1	1	4	4	4	2	7	NRST_PA0 (3) (NRST)	I/O	FT(6)	TIM1_BKIN TIM2_CH3 UART3_TX BEEP ADC_ETR	NRST EXTI0
2	2	2	6	5	5	3	1	PA1	I/O	FT	I2C_SCL TIM1_CH1N TIM2_ETR UART4_TX BEEP ADC_ETR	EXTCLK1 EXTI1
3	3	3	7	6	6	4	1	PA2	I/O	FT	I2C_SMBA SPI_SCK/I2S_CK TIM1_CH2N TIM2_CH4 UART4_RX BEEP ADC_ETR	EXTI2
4	4	4	8	7	7	5	2	VSS	S		Ground	
5	5	5	9	8	8	6	3	VCAP/PD7 (3) (PD7)	I/O	FT	I2C_SMBA USART1_RX SPI_NSS/I2S_WS TIM1_CH3 TIM2_CH1	EXTCLK2 EXTI7

Pin No.								Pin Name (Default Function After Resets)(1)	Pin Type(2)	5-V Tolerant	Pin Functions	
QFN28	QFN24	QFN20	TSSOP28	TSSOP24	TSSOP20	TSSOP16	SOP8				Alternate Function	Additional Function
											RCC_MCO BEEP ADC_ETR	
6	6	6	10	9	9	7	4	VDD	S		Power supply	
7	7	7	11	10	10	8	5	PA3	I/O	FT	USART1_TX SPI_NSS/I2S_WS TIM1_CH3N TIM2_CH3 RCC_MCO BEEP ADC_ETR	EXTI3
8	8	-	12	11	-	-	-	PB6	I/O	FT	I2C_SMBA SPI_SCK/I2S_CK TIM1_CH3 TIM2_CH1 UART2_RX BEEP ADC_ETR	EXTI6
9	9	8	13	12	11	9	5	PB5	I/O	FT	SWCLK I2C_SDA USART1_RX SPI_NSS/I2S_WS TIM1_BKIN TIM2_CH2 UART2_TX BEEP ADC_ETR	EXTCLK3 EXTI5
10	10	9	14	13	12	10	7	PB4	I/O	FT	I2C_SCL USART1_RX SPI_MISO/I2S_MCK TIM1_CH2N TIM2_ETR UART2_RX BEEP ADC_ETR	EXTI4
11	11	-	15	14	-	-	-	PB3	I/O	FT	I2C_SCL SPI_NSS/I2S_WS TIM1_CH2N TIM2_CH4 UART2_TX BEEP ADC_ETR	EXTI3
12	-	-	16	-	-	-	-	PB2	I/O	FT	I2C_SDA SPI_MISO/I2S_MCK TIM1_CH1N TIM2_CH3 UART4_RX BEEP ADC_ETR	EXTI2
13	-	-	17	-	-	-	-	PB1	I/O	FT	I2C_SCL SPI_NSS/I2S_WS TIM1_CH2 TIM2_CH4 UART4_TX BEEP ADC_ETR	EXTI1
14	-	-	18	-	-	-	-	PB0	I/O	FT	I2C_SDA USART1_RX SPI_MISO/I2S_MCK TIM1_CH1 TIM2_CH3	EXTI0

Pin No.								Pin Name (Default Function After Resets)(1)	Pin Type(2)	5-V Tolerant	Pin Functions	
QFN28	QFN24	QFN20	TSSOP28	TSSOP24	TSSOP20	TSSOP16	SOP8				Alternate Function	Additional Function
											RCC_MCO BEEP ADC_ETR	
15	12	-	19	15	-	-	-	PC1	I/O	FT	I2C_SMBA SPI_SCK/I2S_CK TIM1_CH3N TIM2_CH1 UART3_TX BEEP ADC_ETR	EXTI1
16	13	-	20	16	-	-	-	PC2	I/O	FT	SPI_MOSI/I2S_SD TIM1_CH4 TIM2_CH2 UART3_RX BEEP ADC_ETR	EXTI2
17	14	10	21	17	13	11	6	PC3	I/O	FT	USART1_CK SPI_MOSI/I2S_SD TIM1_CH3/TIM1_CH1N TIM2_CH1 RCC_MCO BEEP ADC_ETR	EXTI3
18	15	11	22	18	14	12	6	PC4	I/O	-	SPI_MISO/I2S_MCK TIM1_CH4 TIM1_CH2N TIM2_CH4 UART3_RX BEEP ADC_ETR	WKUP0 EXTI4 ADC_AIN2
19	16	12	23	19	15	13	6	PC5	I/O	FT	I2C_SDA SPI_SCK/I2S_CK TIM1_ETR TIM2_CH1 UART2_TX BEEP ADC_ETR	EXTCLK4 EXTI5
20	17	13	24	20	16	14	8	PC6	I/O	FT	I2C_SCL SPI_MOSI/I2S_SD TIM1_CH1 TIM2_CH3 UART2_RX BEEP ADC_ETR	EXTI6
21	18	14	5	21	17	12	6	PC7	I/O	FT	SPI_MISO/I2S_MCK TIM1_CH2 TIM2_ETR UART4_RX BEEP ADC_ETR	EXTI7
22	-	-	25	-	-	-	-	PD0	I/O	FT	USART1_TX SPI_MOSI/I2S_SD TIM1_BKIN TIM2_CH2 RCC_MCO BEEP ADC_ETR	EXTI0
23	19	15	26	22	18	16	8	PD1	I/O	FT	I2C_SMBA USART1_TX TIM1_CH1 TIM2_CH4	EXTI1

Pin No.								Pin Name (Default Function After Resets)(1)	Pin Type(2)	5-V Tolerant	Pin Functions	
QFN28	QFN24	QFN20	TSSOP28	TSSOP24	TSSOP20	TSSOP16	SOP8				Alternate Function	Additional Function
											UART4_TX BEEP ADC_ETR	
24	20	16	27	23	19	9	5	PD2	I/O	-	SPI_MOSI/I2S_SD TIM1_CH2 TIM2_CH3 UART3_TX BEEP ADC_ETR	EXTI2 ADC_AIN4(4)(5)
25	21	17	28	24	20	15	8	PD3	I/O	-	SPI_SCK/I2S_CK TIM1_CH3 TIM2_CH2 UART3_RX BEEP ADC_ETR	EXTI3 ADC_AIN3(4)
26	22	18	1	1	1	1	1	PD4	I/O	FT	I2C_SMBA USART1_CK SPI_MOSI/I2S_SD TIM1_CH4 TIM2_CH1 RCC_MCO BEEP ADC_ETR	EXTI4
27	23	19	2	2	2	16	8	PD5	I/O	-	SWDIO USART1_TX TIM1_ETR TIM2_ETR RCC_MCO BEEP ADC_ETR	EXTI5 ADC_AIN0
28	24	20	3	3	3	1	1	PD6	I/O	-	USART1_RX SPI_MISO/I2S_MCK TIM1_CH2 TIM2_CH2 RCC_MCO BEEP ADC_ETR	EXTI6 ADC_AIN1

(1). The default pin function after resets, except for pins in SOP8 and TSSOP16 packages. If IOMUX is configured for SOP8 and TSSOP16 packages, see Table 6-2 and Table 6-3 for default pin functions.

(2). I = input, O = output, I/O = input/output, S = power supply.

(3). In the HK32F030MxxxxA series, PD7 and PA0 are only available in SOP8 and TSSOP16 packages. In the HK32F0301MxxxxA series, PD7 and PA0 are available in all packages.

(4). This function is not supported in the SOP8 package.

(5). This function is not supported in the TSSOP16 package.

(6). FT = 5 V tolerant.

Note:

- Unless otherwise specified, all I/Os are configured in input floating mode during and after resets.

6.10 IOMUX

In small packages (SOP8 and TSSOP16) of HK32F030MxxxxA/HK32F0301MxxxxA, the mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX.

6.10.1 IOMUX of the TSSOP16 package

Table 6-2 TSSOP16 IOMUX table

Pin No.	Map To	Pin Type	5 V-Tolerant	Pin Functions	
				Alternate Function	Additional Function
1	PD6 (default)	I/O	-	USART1_RX SPI_MISO/I2S_MCK TIM1_CH2 TIM2_CH2 RCC_MCO BEEP ADC_ETR	EXTI6 ADC_AIN1
	PD4	I/O	FT(1)	I2C_SMBA USART1_CK SPI_MOSI/I2S_SD TIM1_CH4 TIM2_CH1 RCC_MCO BEEP ADC_ETR	EXTI4
9	PB5 (default)	I/O	FT	SWCLK I2C_SDA USART1_RX SPI_NSS/I2S_WS TIM1_BKIN TIM2_CH2 UART2_TX BEEP ADC_ETR	EXTCLK3 EXTI5
	PD2	I/O	-	SPI_MOSI/I2S_SD TIM1_CH2 TIM2_CH3 UART3_TX BEEP ADC_ETR	EXTI2
12	PC4 (default)	I/O	-	SPI_MISO/I2S_MCK TIM1_CH4 TIM1_CH2N TIM2_CH4 UART3_RX BEEP ADC_ETR	WKUP0 EXTI4 ADC_AIN2
	PC7	I/O	FT	SPI_MISO/I2S_MCK TIM1_CH2 TIM2_ETR UART4_RX BEEP ADC_ETR	EXTI7
16	PD5 (default)	I/O	-	SWDIO USART1_TX TIM1_ETR TIM2_ETR RCC_MCO BEEP ADC_ETR	EXTI5 ADC_AIN0
	PD1	I/O	FT	I2C_SMBA USART1_TX TIM1_CH1 TIM2_CH4 UART4_TX BEEP ADC_ETR	EXTI1

(1). FT = 5 V tolerant.

6.10.2 IOMUX of the SOP8 package

Table 6-3 SOP8 IOMUX table

Pin No.	Map To	Pin Type	5 V-Tolerant	Pin Functions	
				Alternate Function	Additional Function
1	PD6 (default)	I/O	-	USART1_RX SPI_MISO/I2S_MCK TIM1_CH2 TIM2_CH2 RCC_MCO BEEP ADC_ETR	EXTI6 ADC_AIN1
	PA1	I/O	FT(1)	I2C1_SCL TIM1_CH1N TIM2_ETR UART4_TX BEEP ADC1_ETR	EXTCLK1 EXTI1
	PD4	I/O	FT	I2C_SMBA USART1_CK SPI_MOSI/I2S_SD TIM1_CH4 TIM2_CH1 RCC_MCO BEEP ADC_ETR	EXTI4
	PA2	I/O	FT	I2C_SMBA SPI_SCK/I2S_CK TIM1_CH2N TIM2_CH4 UART4_RX BEEP ADC_ETR	EXTI2
5	PB5	I/O	FT	SWCLK I2C_SDA USART1_RX SPI_NSS/I2S_WS TIM1_BKIN TIM2_CH2 UART2_TX BEEP ADC_ETR	EXTCLK3 EXTI5
	PA3	I/O	FT	USART1_TX SPI_NSS/I2S_WS TIM1_CH3N TIM2_CH3 RCC_MCO BEEP ADC_ETR	EXTI3
	PD2	I/O	-	SPI_MOSI/I2S_SD TIM1_CH2 TIM2_CH3 UART3_TX BEEP ADC_ETR	EXTI2
6	PC4 (default)	I/O	-	SPI_MISO/I2S_MCK TIM1_CH4 TIM1_CH2N TIM2_CH4 UART3_RX BEEP ADC_ETR	WKUP0 EXTI4 ADC_AIN2
	PC3	I/O	FT	USART1_CK SPI1_MOSI TIM1_CH3_CH1N	EXTI3

Pin No.	Map To	Pin Type	5 V-Tolerant	Pin Functions	
				Alternate Function	Additional Function
				TIM2_CH1 RCC_MCO BEEP ADC1_ETR	
	PC5	I/O	FT	I2C1_SDA SPI1_SCK TIM1_ETR TIM2_CH1 UART2_TX BEEP ADC1_ETR	EXTCLK4 EXTI5
	PC7	I/O	FT	SPI_MISO/I2S_MCK TIM1_CH2 TIM2_ETR UART4_RX BEEP ADC_ETR	EXTI7
7	NRST_PA0 (default)	I/O	FT	TIM1_BKIN TIM2_CH3 UART3_TX BEEP ADC_ETR	NRST EXTI0
	PB4	I/O	FT	I2C_SCL USART1_RX SPI_MISO/I2S_MCK TIM1_CH2N TIM2_ETR UART2_RX BEEP ADC_ETR	EXTI4
8	PD5 (default)	I/O	-	SWDIO USART1_TX TIM1_ETR TIM2_ETR RCC_MCO BEEP ADC_ETR	EXTI5 ADC_AIN0
	PD3	I/O	-	SPI_SCK/I2S_CK TIM1_CH3 TIM2_CH2 UART3_RX BEEP ADC_ETR	EXTI3
	PD1	I/O	FT	I2C_SMBA USART1_TX TIM1_CH1 TIM2_CH4 UART4_TX BEEP ADC_ETR	EXTI1
	PC6	I/O	FT	I2C_SCL SPI_MOSI/I2S_SD TIM1_CH1 TIM2_CH3 UART2_RX BEEP ADC_ETR	EXTI6

(1). FT = 5 V tolerant.

6.11 Alternate function table

Table 6-4 Alternate function table

Pin Name	AF0 (I2C/SWD)	AF1 (USART1)	AF2 (SPI/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC/UART)	AF6 (Beeper)	AF7 (ADC)
PA0	-	-	-	TIM1_BKIN	TIM2_CH3	UART3_TX/ UART3_RX	BEEP	ADC_ETR
PA1	I2C_SCL	-	-	TIM1_CH1N	TIM2_ETR	UART4_TX/ UART4_RX	BEEP	ADC_ETR
PA2	I2C_SMBA	-	SPI_SCK	TIM1_CH2N	TIM2_CH4	UART4_RX/ UART4_TX	BEEP	ADC_ETR
PA3	-	USART1_TX/ USART1_RX	SPI_NSS	TIM1_CH3N	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PB0	I2C_SDA	USART1_RX /USART1_TX	SPI_MISO	TIM1_CH1	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PB1	I2C_SCL	-	SPI_NSS	TIM1_CH2	TIM2_CH4	UART4_TX/ UART4_RX	BEEP	ADC_ETR
PB2	I2C_SDA	-	SPI_MISO	TIM1_CH1N	TIM2_CH3	UART4_RX/ UART4_TX	BEEP	ADC_ETR
PB3	I2C_SCL	-	SPI_NSS	TIM1_CH2N	TIM2_CH4	UART2_TX/ UART2_RX	BEEP	ADC_ETR
PB4	I2C_SCL	USART1_RX /USART1_TX	SPI_MISO	TIM1_CH2N	TIM2_ETR	UART2_RX/ UART2_TX	BEEP	ADC_ETR
PB5	SWCLK/ I2C_SDA(1)	USART1_RX /USART1_TX	SPI_NSS	TIM1_BKIN	TIM2_CH2	UART2_TX/ UART2_RX	BEEP	ADC_ETR
PB6	I2C_SMBA	-	SPI_SCK	TIM1_CH3	TIM2_CH1	UART2_RX/ UART2_TX	BEEP	ADC_ETR
PC1	I2C_SMBA	-	SPI_SCK	TIM1_CH3N	TIM2_CH1	UART3_TX/ UART3_RX	BEEP	ADC_ETR
PC2	-	-	SPI_MOSI	TIM1_CH4	TIM2_CH2	UART3_RX/ UART3_TX	BEEP	ADC_ETR
PC3	-	USART1_CK	SPI_MOSI	TIM1_CH3/ TIM1_CH1N(1)	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC4	-	-	SPI_MISO	TIM1_CH4/ TIM1_CH2N(1)	TIM2_CH4	UART3_RX/ UART3_TX	BEEP	ADC_ETR
PC5	I2C_SDA	-	SPI_SCK	TIM1_ETR	TIM2_CH1	UART2_TX/ UART2_RX	BEEP	ADC_ETR
PC6	I2C_SCL	-	SPI_MOSI	TIM1_CH1	TIM2_CH3	UART2_RX/ UART2_TX	BEEP	ADC_ETR
PC7	-	-	SPI_MISO	TIM1_CH2	TIM2_ETR	UART4_RX/ UART4_TX	BEEP	ADC_ETR
PD0	-	USART1_TX/ USART1_RX	SPI_MOSI	TIM1_BKIN	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PD1	I2C_SMBA	USART1_TX/ USART1_RX	-	TIM1_CH1	TIM2_CH4	UART4_TX/ UART4_RX	BEEP	ADC_ETR
PD2	-	-	SPI_MOSI	TIM1_CH2	TIM2_CH3	UART3_TX/ UART3_RX	BEEP	ADC_ETR
PD3	-	-	SPI_SCK	TIM1_CH3	TIM2_CH2	UART3_RX/ UART3_TX	BEEP	ADC_ETR
PD4	I2C_SMBA	USART1_CK	SPI_MOSI	TIM1_CH4	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PD5	SWDIO	USART1_TX/ USART1_RX	-	TIM1_ETR	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PD6	-	USART1_RX /USART1_TX	SPI_MISO	TIM1_CH2	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PD7	I2C_SMBA	USART1_RX /USART1_TX	SPI_NSS	TIM1_CH3	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR

(1). Configure the IOMUX register to set the following alternate functions: PC3 as CH3 or CH1N of TIM1, PC4 as CH4 or CH2N of TIM1, PB5 as SWCLK or I2C_SDA.

7 Packages

7.1 Package outlines

7.1.1 QFN28

QFN28 is a 4 mm × 4 mm, 0.4 mm pitch package.

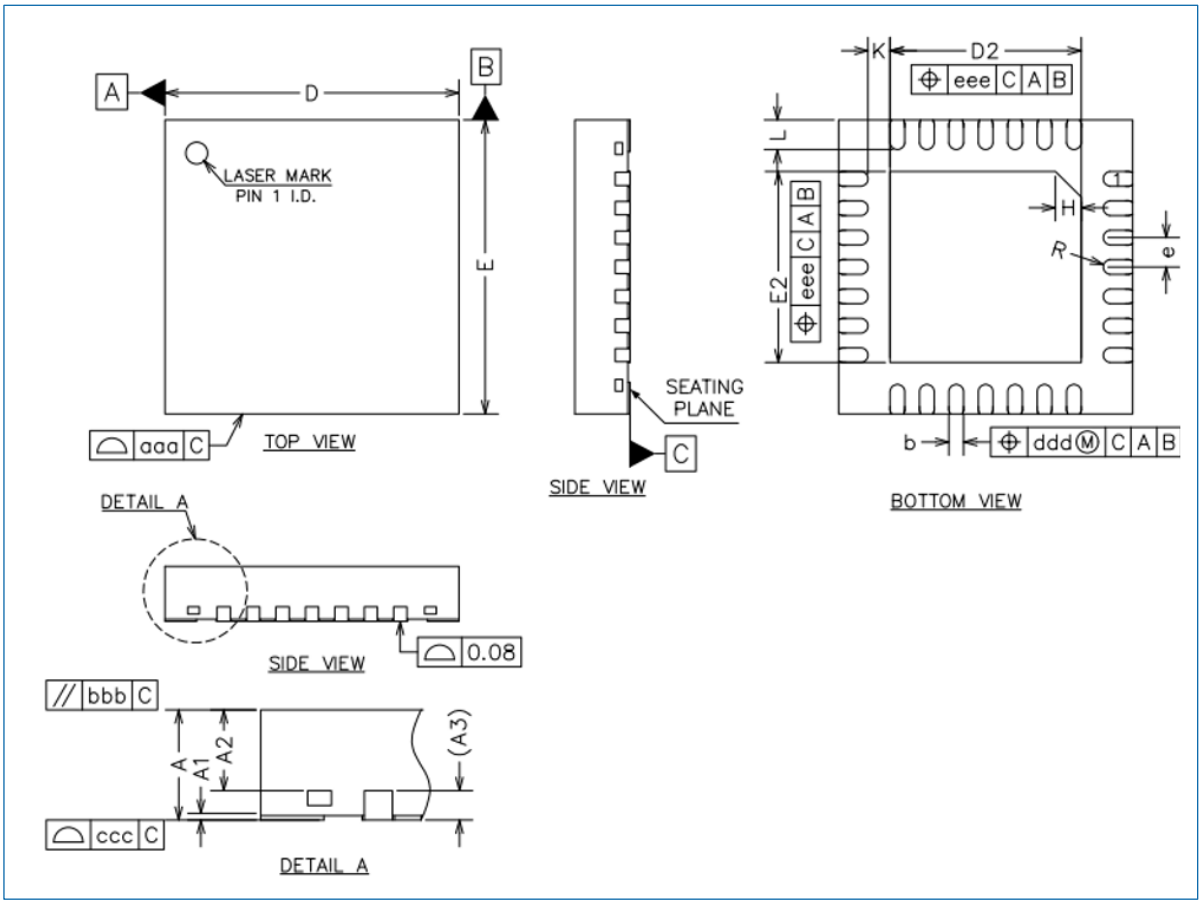


Figure 7-1 QNF28 package outline

Table 7-1 QFN28 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.8
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20 REF(1)		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.30	0.40	0.50
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
L	0.35	0.40	0.45
R	0.075	-	-
K	0.30 REF		
H	0.35 REF		
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
eee	0.10		

(1). REF indicates a reference value.

7.1.2 QFN24

QFN24 is a 3 mm × 3 mm, 0.35 mm pitch package.

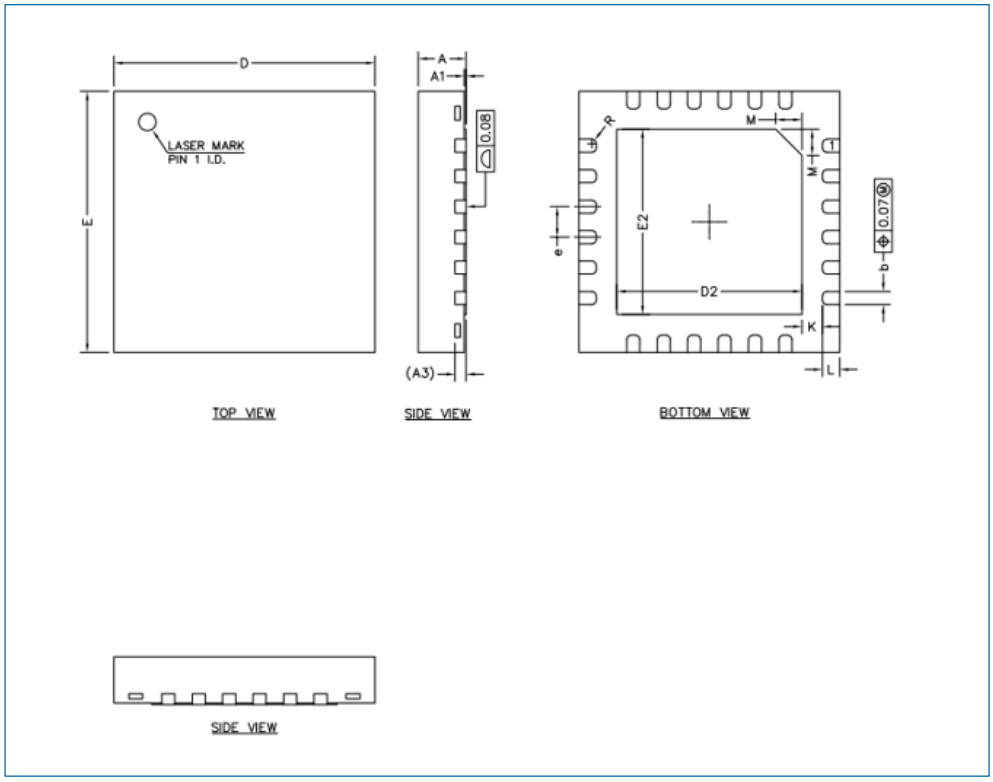


Figure 7-2 QFN24 package outline

Table 7-2 QFN24 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.127 REF(1)		
b	0.10	0.15	0.20
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.03	2.13	2.23
E2	2.03	2.13	2.23
e	0.30	0.35	0.40
K	0.235 REF		
L	0.15	0.20	0.25
M	0.30 REF		
R	0.05 REF		

(1). REF indicates a reference value.

7.1.3 QFN20

The QFN20 package has two types of outlines. One is the 3 mm × 3 mm, 0.4 mm pitch package, as shown in Figure 7-3. Another is the 4 mm × 4 mm, 0.5 mm pitch package, as shown in Figure 7-4.

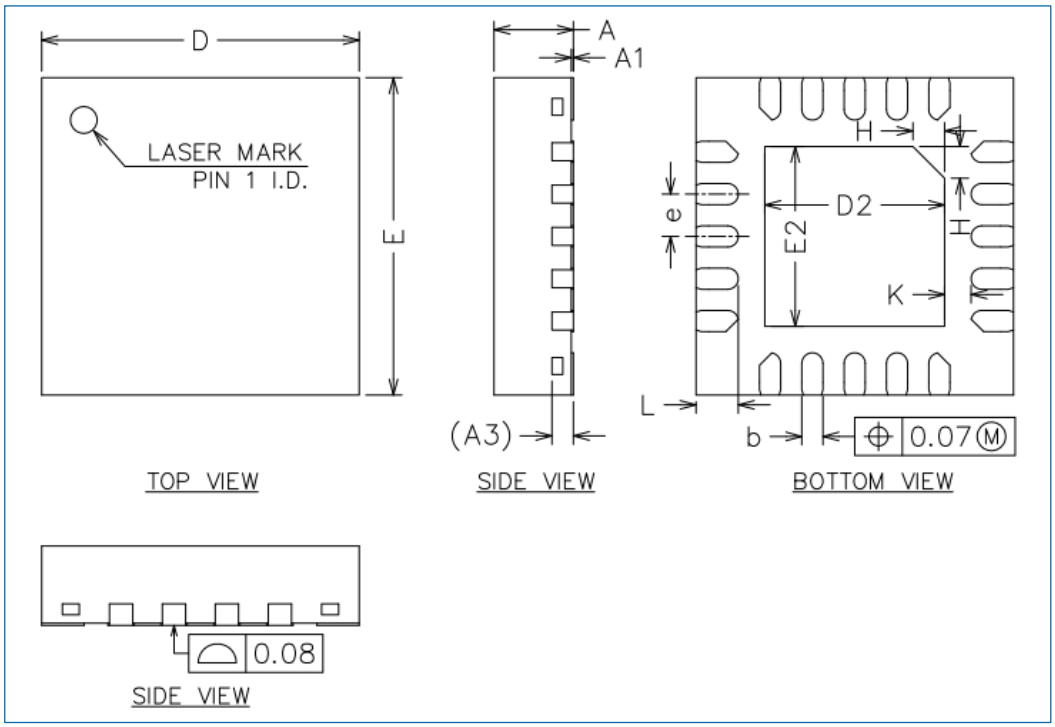


Figure 7-3 Outline of QFN20 package 1

Table 7-3 Parameters of QFN20 package 1

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF(1)		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75
e	0.30	0.40	0.50
H	0.30 REF		
K	0.15	-	-
L	0.35	0.40	0.45

(1). REF indicates a reference value.

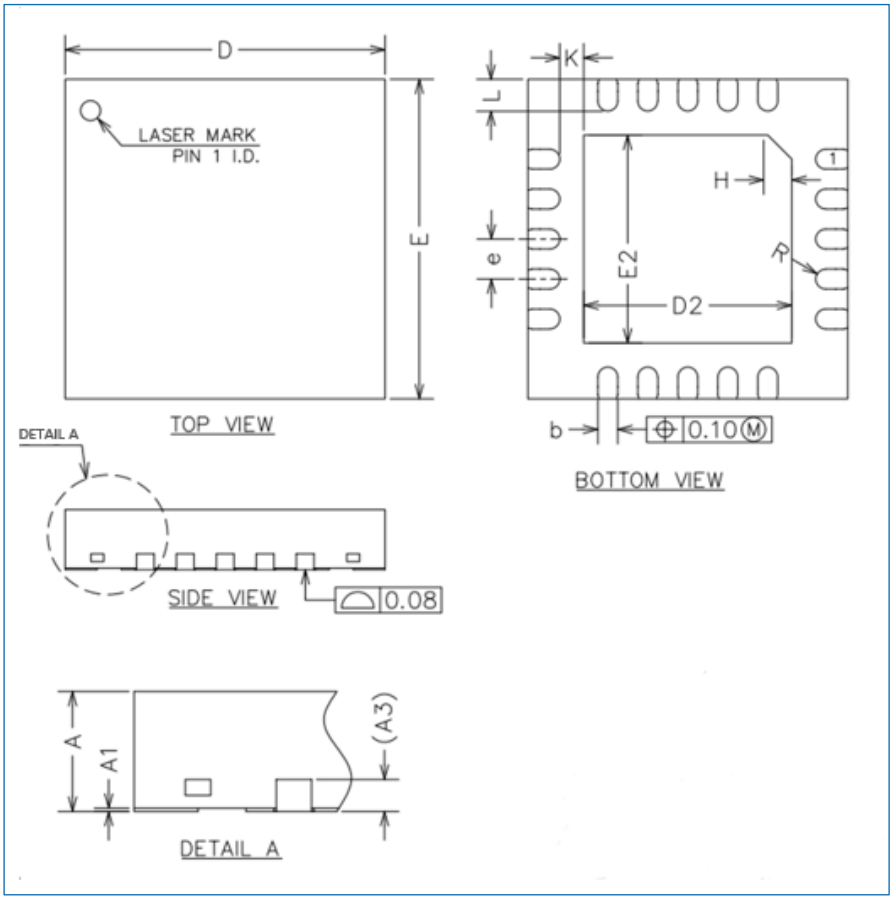


Figure 7-4 Outline of QFN20 package 2

Table 7-4 Parameters of QFN20 package 2

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF(1)		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
H	0.30 REF		
K	0.20	-	-
L	0.35	0.40	0.45
R	0.10	-	-

(1). REF indicates a reference value.

7.1.4 TSSOP28

TSSOP28 is a 9.70 mm × 4.40 mm, 0.65 mm pitch package.

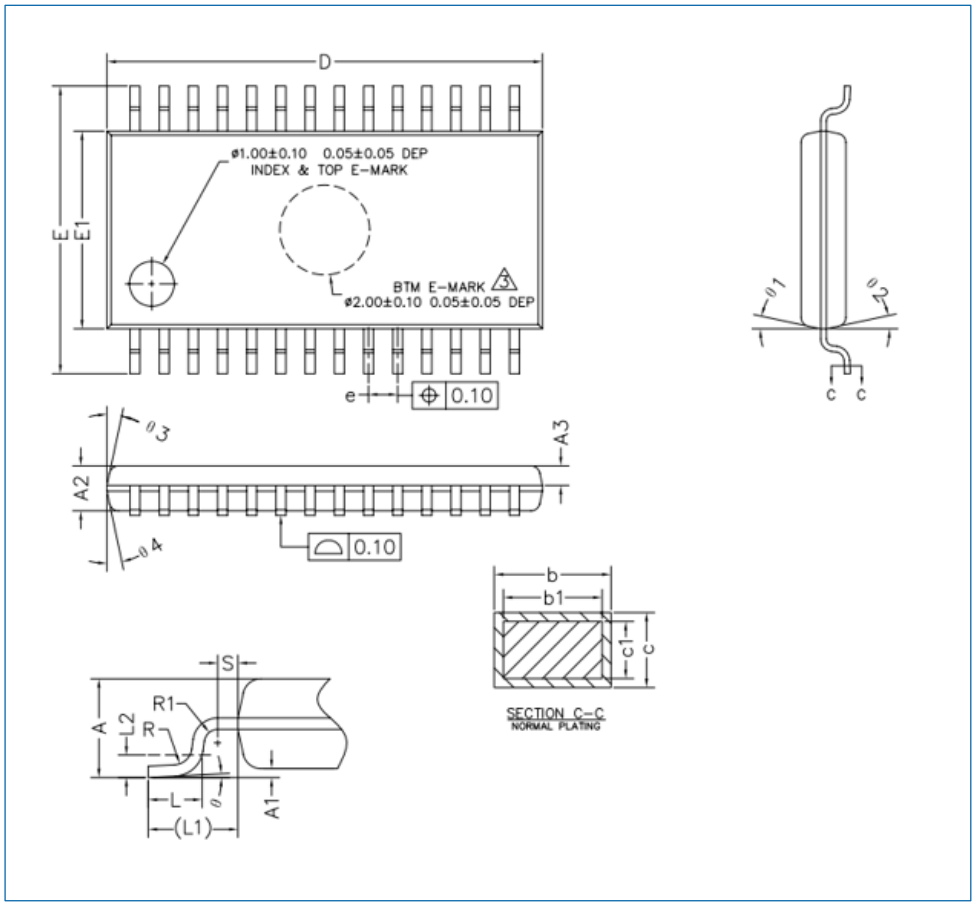


Figure 7-5 TSSOP28 package outline

Table 7-5 TSSOP28 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00 REF(1)		
L2	0.25 BSC(2)		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	--	8°
	10°	12°	14°
	10°	12°	14°
	10°	12°	14°
	10°	12°	14°

(1). REF indicates a reference value.

(2). BSC: basic spacing between centers.

7.1.5 TSSOP24

TSSOP24 is a 7.8 mm × 4.4 mm, 0.65 mm pitch package.

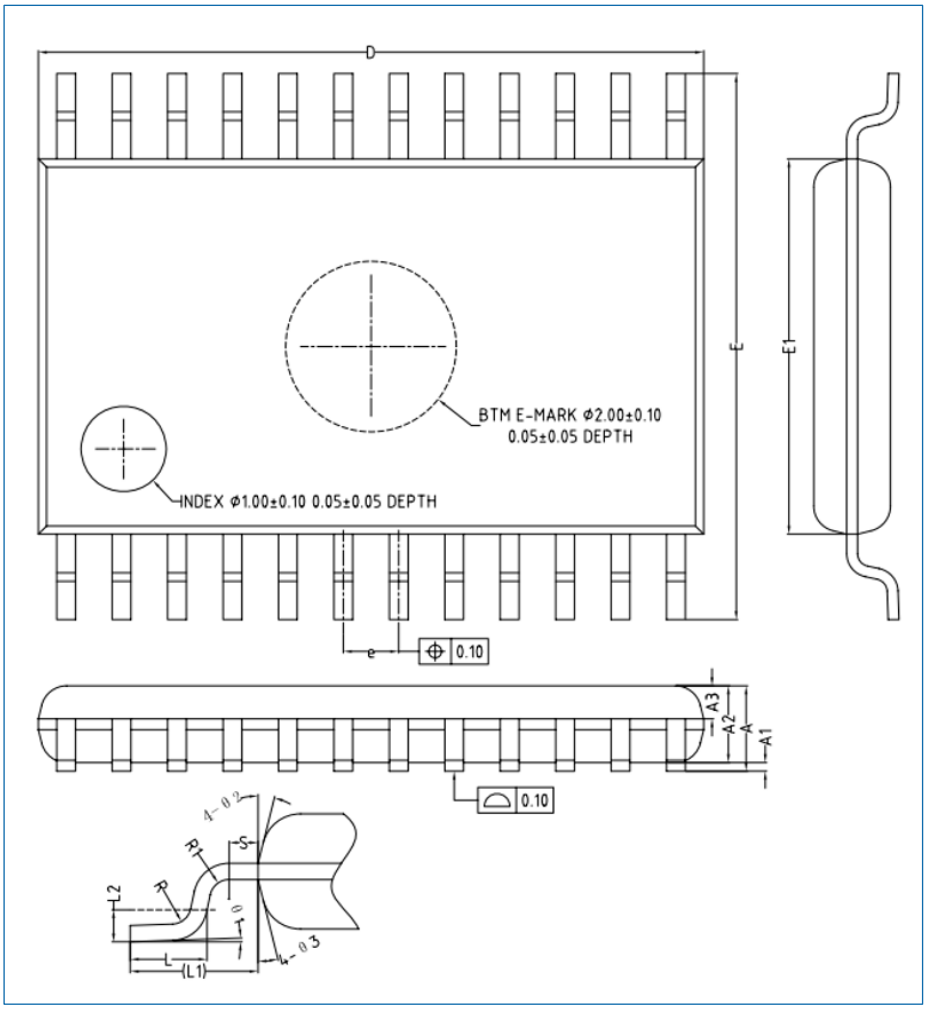


Figure 7-6 TSSOP24 package outline

Table 7-6 TSSOP24 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.00
A3	0.34	0.39	0.44
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00 REF(1)		
L2	0.25 BSC(2)		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	12°	14°	16°
θ3	12°	14°	16°

(1). REF indicates a reference value.

(2). BSC: basic spacing between centers.

7.1.6 TSSOP20

TSSOP20 is a 6.5 mm × 4.4 mm, 0.65 mm pitch package.

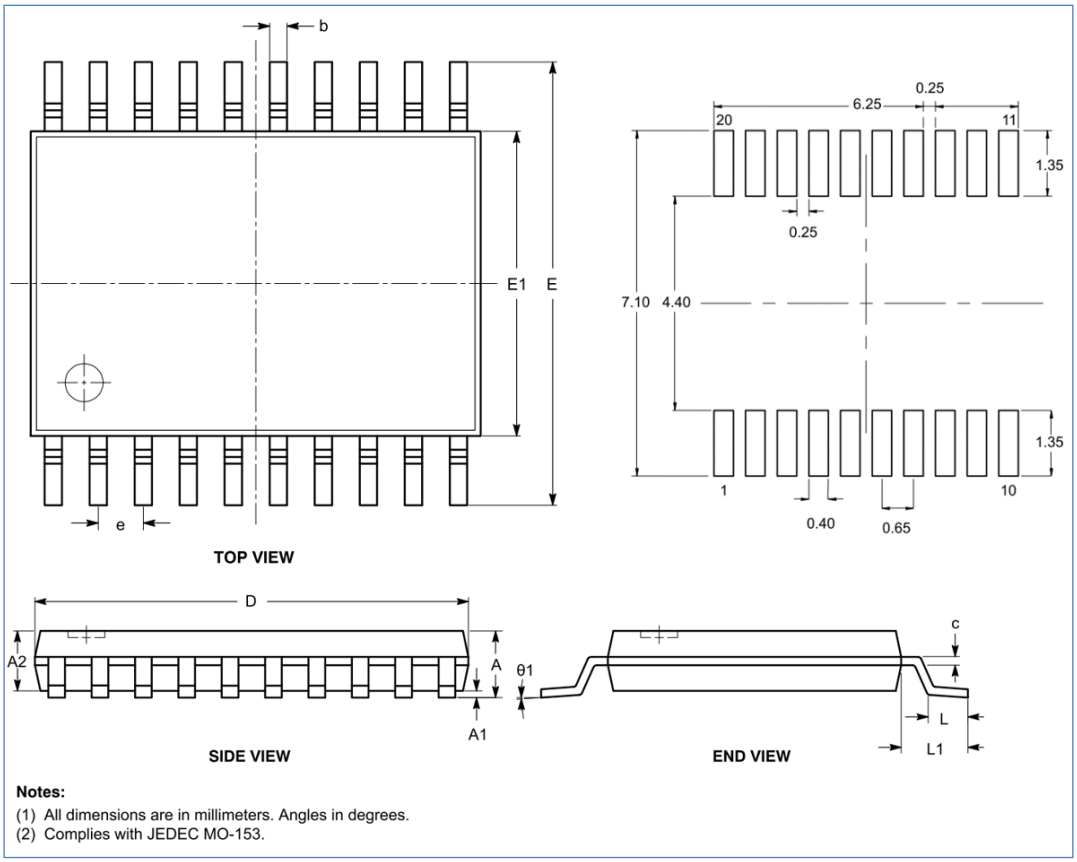


Figure 7-7 TSSOP20 package outline

Table 7-7 TSSOP20 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC(2)		
L	0.45	0.60	0.75
L1	1.00 REF(1)		
θ	0°	-	8°

(1). REF indicates a reference value.

(2). BSC: basic spacing between centers.

7.1.7 TSSOP16

TSSOP16 is a 5.0 mm × 4.4 mm, 0.65 mm pitch package.

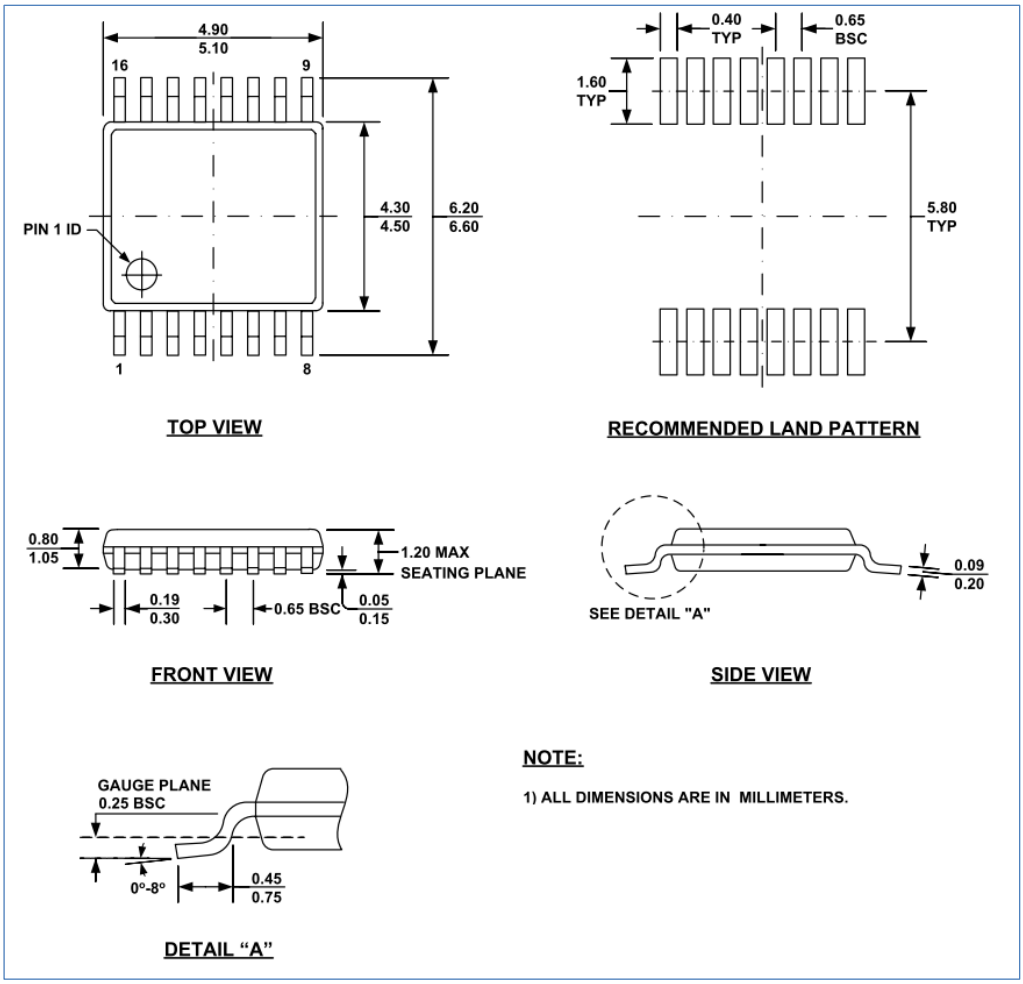


Figure 7-8 TSSOP16 package outline

Table 7-8 TSSOP16 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
b1	0.20	0.22	0.24
c	0.10	-	0.19
C1	0.10	0.13	0.15
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC(2)		
L	0.45	0.60	0.75
L1	1.00 REF(1)		
L2	0.25 BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

(1). REF indicates a reference value.

(2). BSC: basic spacing between centers.

7.1.8 SOP8

SOP8 is a 4.9 mm × 3.8 mm, 1.27 mm pitch package.

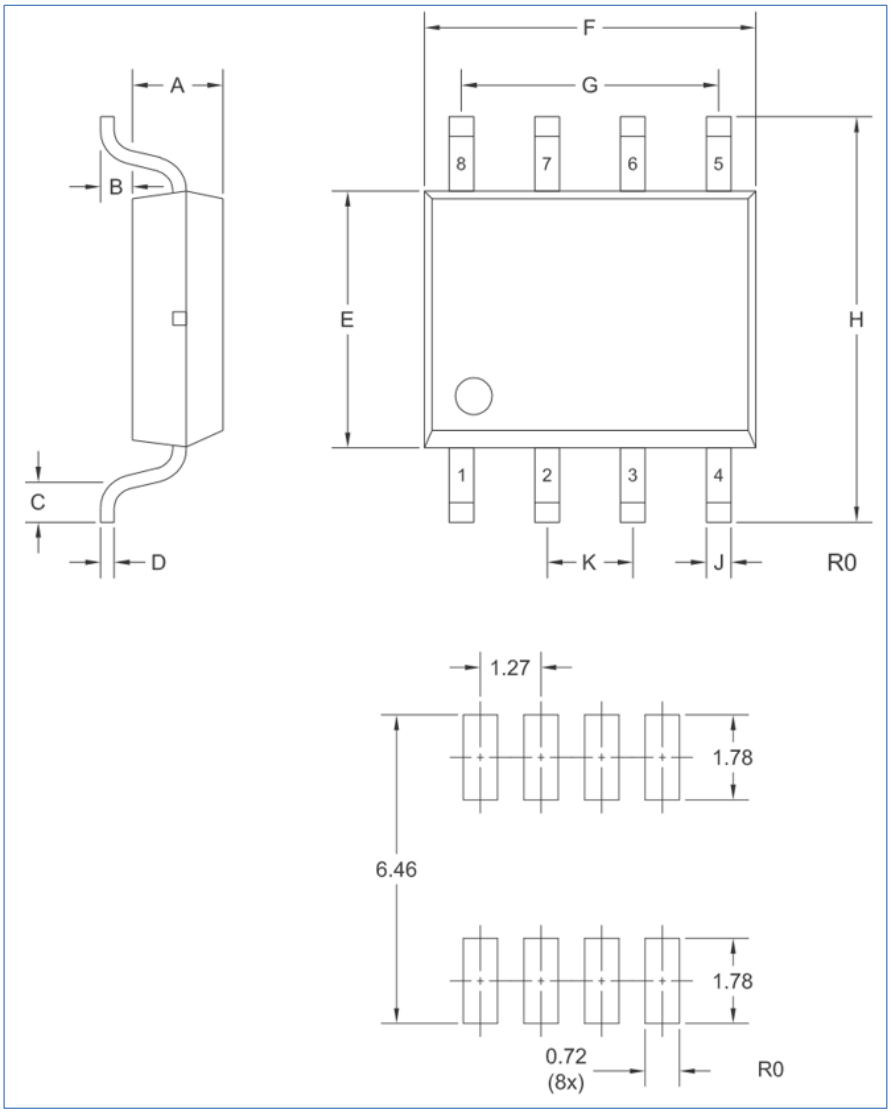


Figure 7-9 SOP8 package outline

Table 7-9 SOP8 package parameters

Symbol	Unit: mm		Unit: inches(1)	
	Min	Max	Min	Max
A	1.24	1.44	0.049	0.057
B	0.00	0.27	0.000	0.011
C	0.46	-	0.018	-
D	0.16	0.27	0.006	0.011
E	3.70	3.90	0.145	0.154
F	4.81	5.01	0.189	0.198
G	3.81		0.150	
H	5.88	6.18	0.231	0.244
J	0.35	0.52	0.013	0.021
K	1.27		0.050	

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-10 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 QFN28 marking

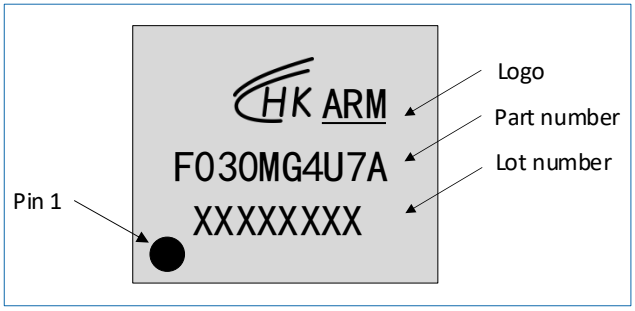


Figure 7-10 QFN28 HK32F030MG4U7A marking example

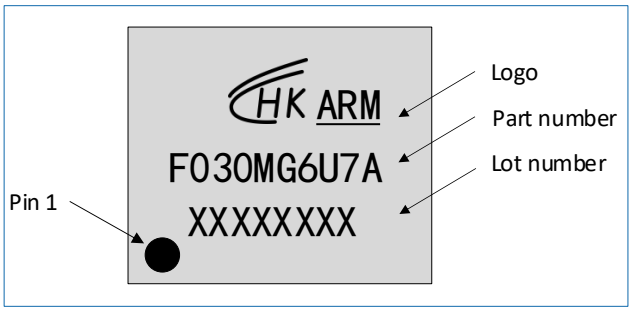


Figure 7-11 QFN28 HK32F030MG6U7A marking example

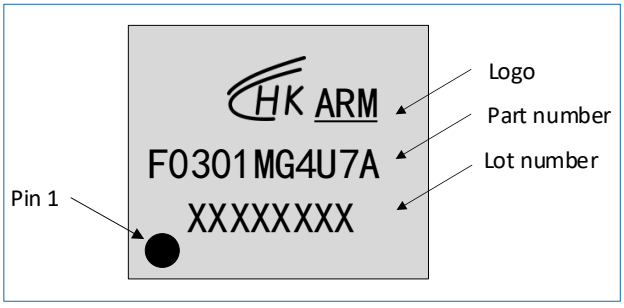


Figure 7-12 QFN28 HK32F0301MG4U7A marking example

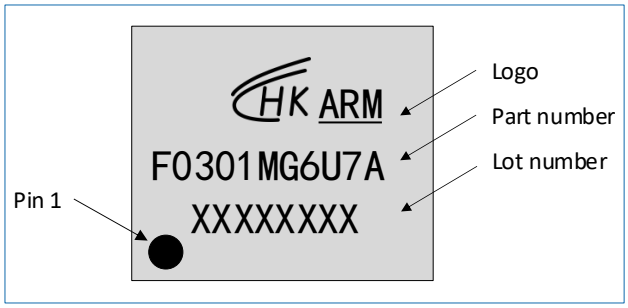


Figure 7-13 QFN28 HK32F0301MG6U7A marking example

7.2.2 QFN24 marking

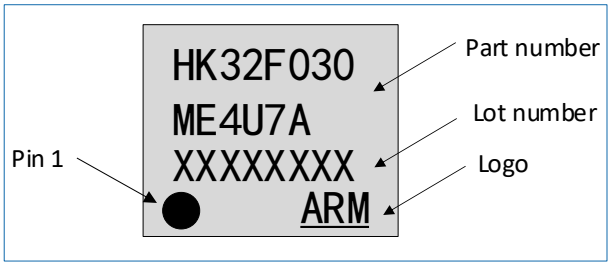


Figure 7-14 QFN24 HK32F030ME4U7A marking example

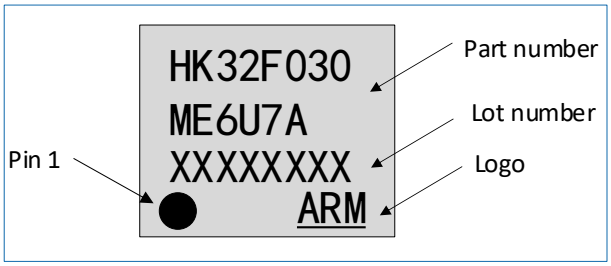


Figure 7-15 QFN24 HK32F030ME6U7A marking example

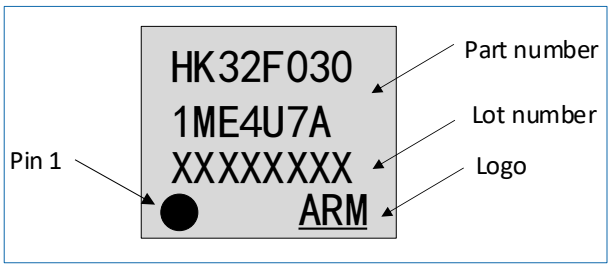


Figure 7-16 QFN24 HK32F0301ME4U7A marking example

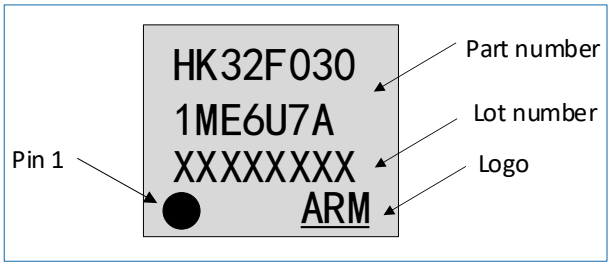


Figure 7-17 QFN24 HK32F0301ME6U7A marking example

7.2.3 QFN20 marking (4 mm × 4 mm package)

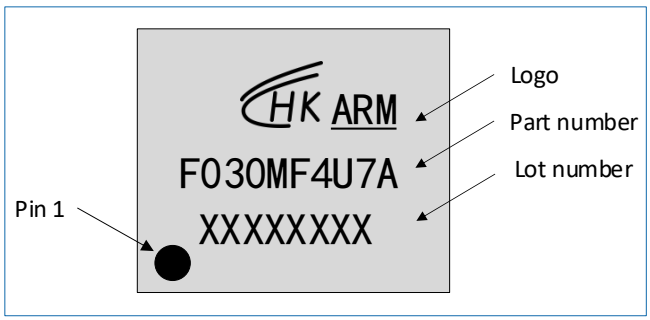


Figure 7-18 QFN20 HK32F030MF4U7A marking example (4 mm × 4 mm package)

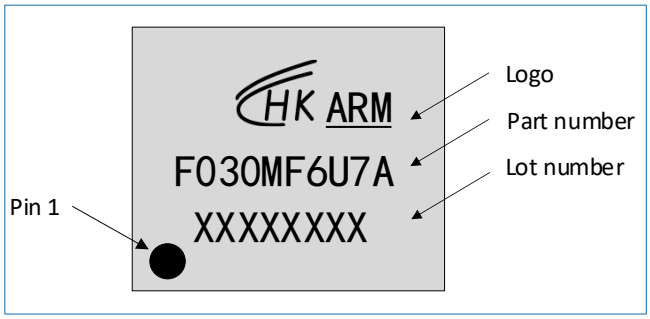


Figure 7-19 QFN20 HK32F030MF6U7A marking example (4 mm × 4 mm package)

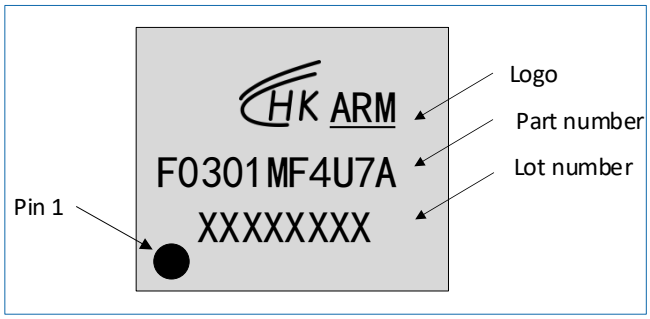


Figure 7-20 QFN20 HK32F0301MF4U7A marking example (4 mm × 4 mm package)

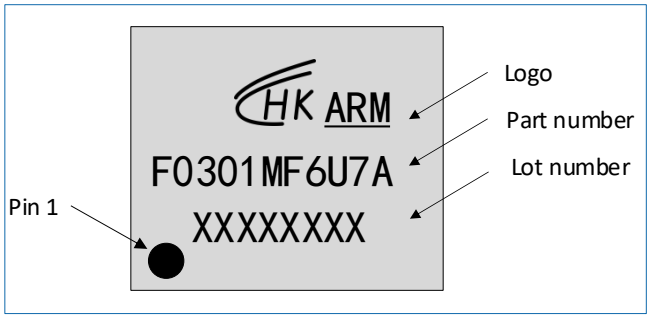


Figure 7-21 QFN20 HK32F0301MF6U7A marking example (4 mm × 4 mm package)

7.2.4 QFN20 marking (3 mm × 3 mm package)

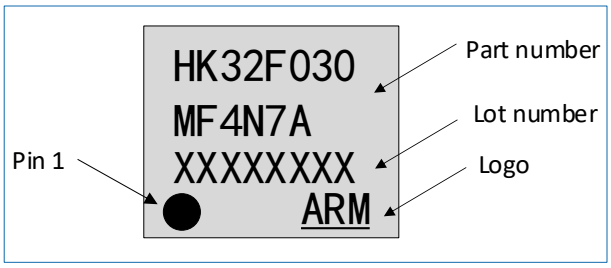


Figure 7-22 QFN20 HK32F030MF4N7A marking example (3 mm × 3 mm package)

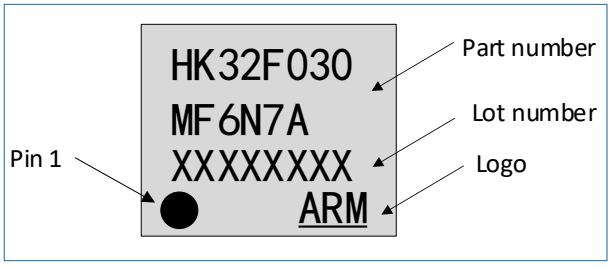


Figure 7-23 QFN20 HK32F030MF6N7A marking example (3 mm × 3 mm package)

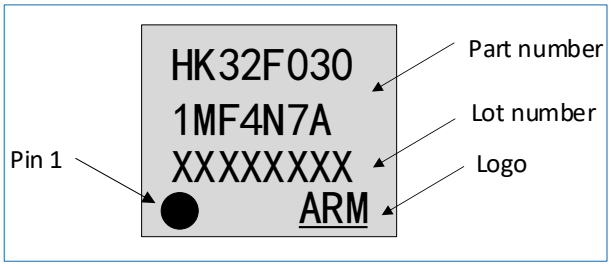


Figure 7-24 QFN20 HK32F0301MF4N7A marking example (3 mm × 3 mm package)

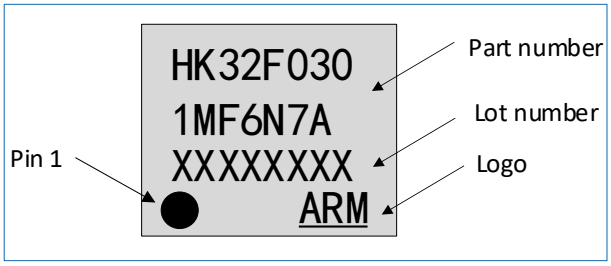


Figure 7-25 QFN20 HK32F0301MF6N7A marking example (3 mm × 3 mm package)

7.2.5 TSSOP28 marking

Figure 7-26 TSSOP28 HK32F030MG4P7A marking example

Figure 7-27 TSSOP28 HK32F030MG6P7A marking example

Figure 7-28 TSSOP28 HK32F0301MG4P7A marking example

Figure 7-29 TSSOP28 HK32F0301MG6P7A marking example

7.2.6 TSSOP24 marking

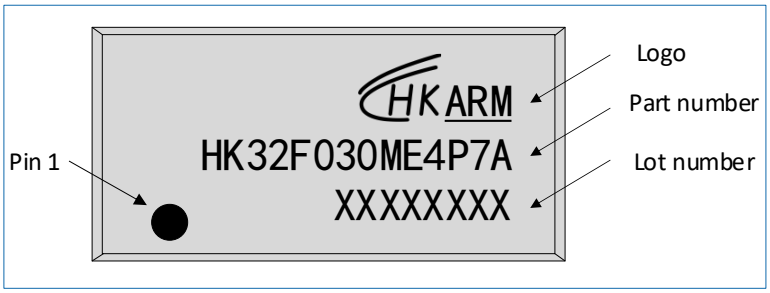


Figure 7-30 TSSOP24 HK32F030ME4P7A marking example

Figure 7-31 TSSOP24 HK32F030ME6P7A marking example

Figure 7-32 TSSOP24 HK32F0301ME4P7A marking example

Figure 7-33 TSSOP24 HK32F0301ME6P7A marking example

7.2.7 TSSOP20 marking

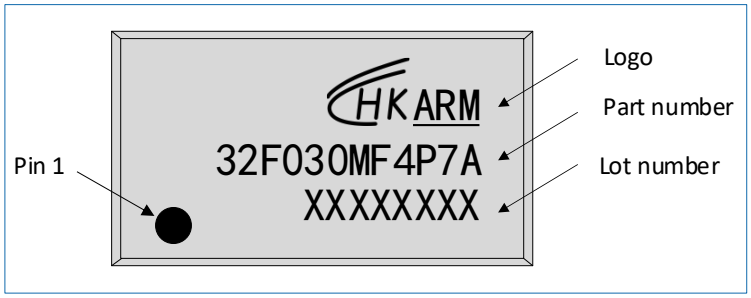


Figure 7-34 TSSOP20 HK32F030MF4P7A marking example

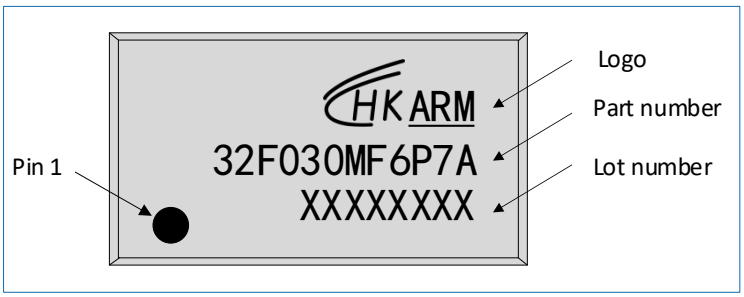


Figure 7-35 TSSOP20 HK32F030MF6P7A marking example

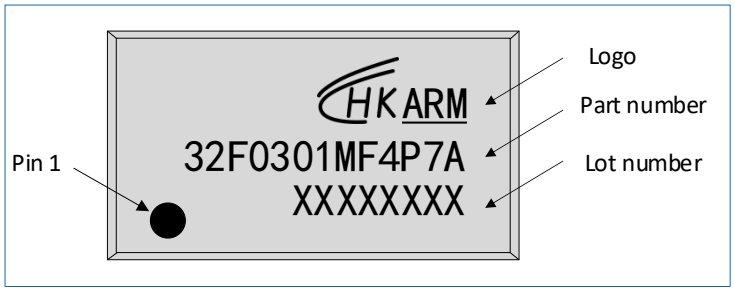


Figure 7-36 TSSOP20 HK32F0301MF4P7A marking example

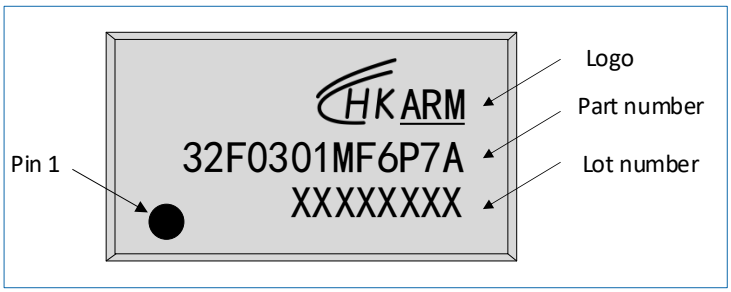


Figure 7-37 TSSOP20 HK32F0301MF6P7A marking example

7.2.8 TSSOP16 marking

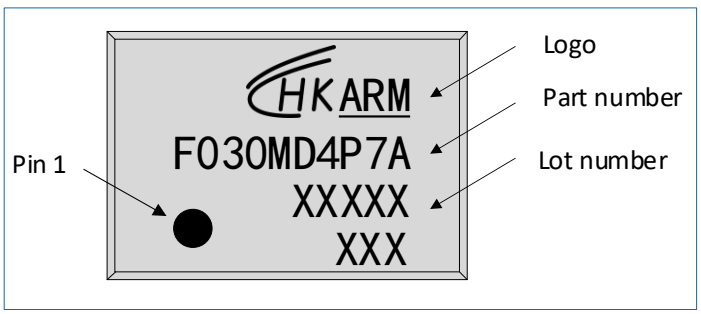


Figure 7-38 TSSOP16 HK32F030MD4P7A marking example

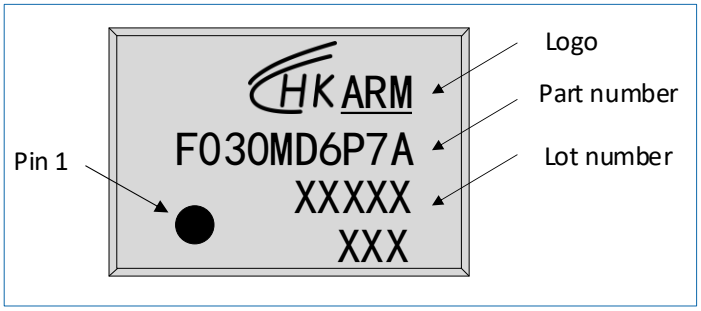


Figure 7-39 TSSOP16 HK32F030MD6P7A marking example

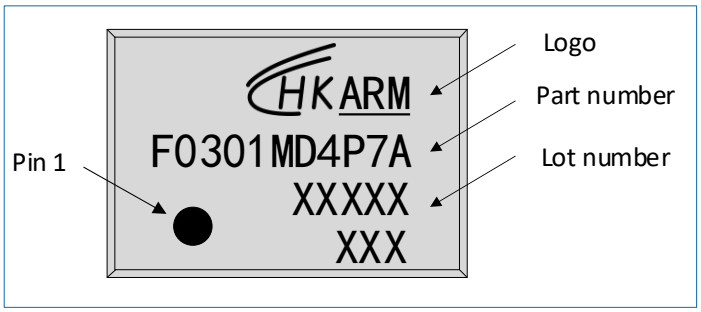


Figure 7-40 TSSOP16 HK32F0301MD4P7A marking example

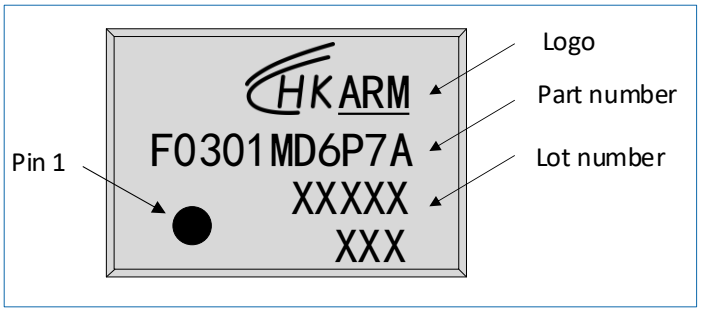


Figure 7-41 TSSOP16 HK32F0301MD6P7A marking example

7.2.9 SOP8 marking

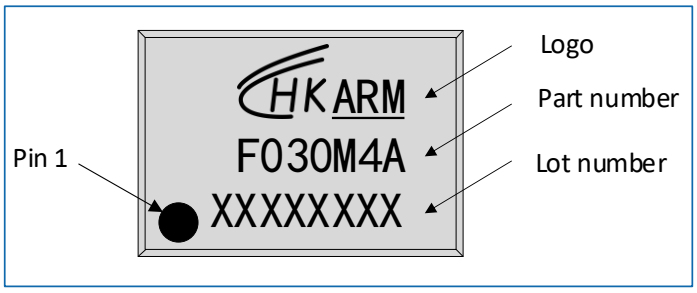


Figure 7-42 SOP8 HK32F030MJ4M7A marking example

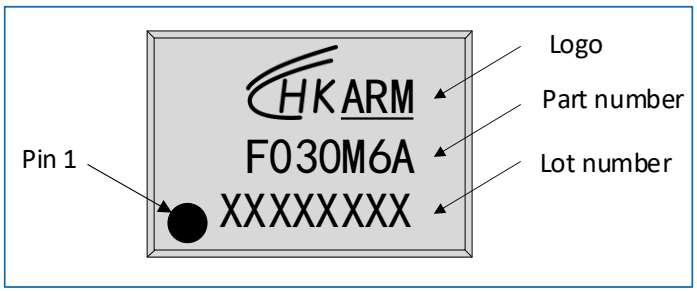


Figure 7-43 SOP8 HK32F030MJ6M7A marking example

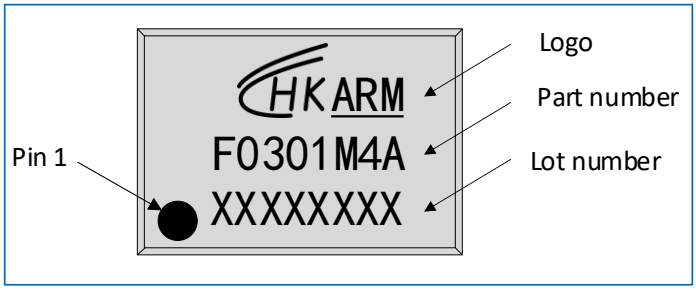


Figure 7-44 SOP8 HK32F0301MJ4M7A marking example

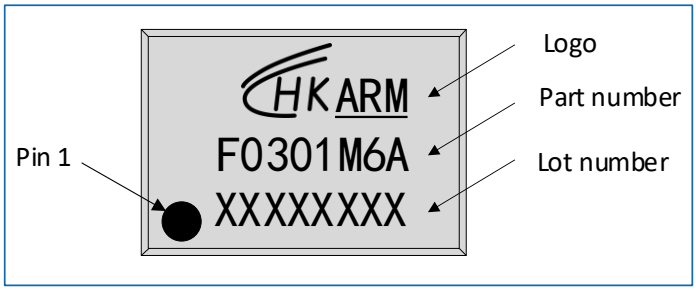


Figure 7-45 SOP8 HK32F0301MJ6M7A marking example

8 Ordering information

8.1 Device numbering conventions

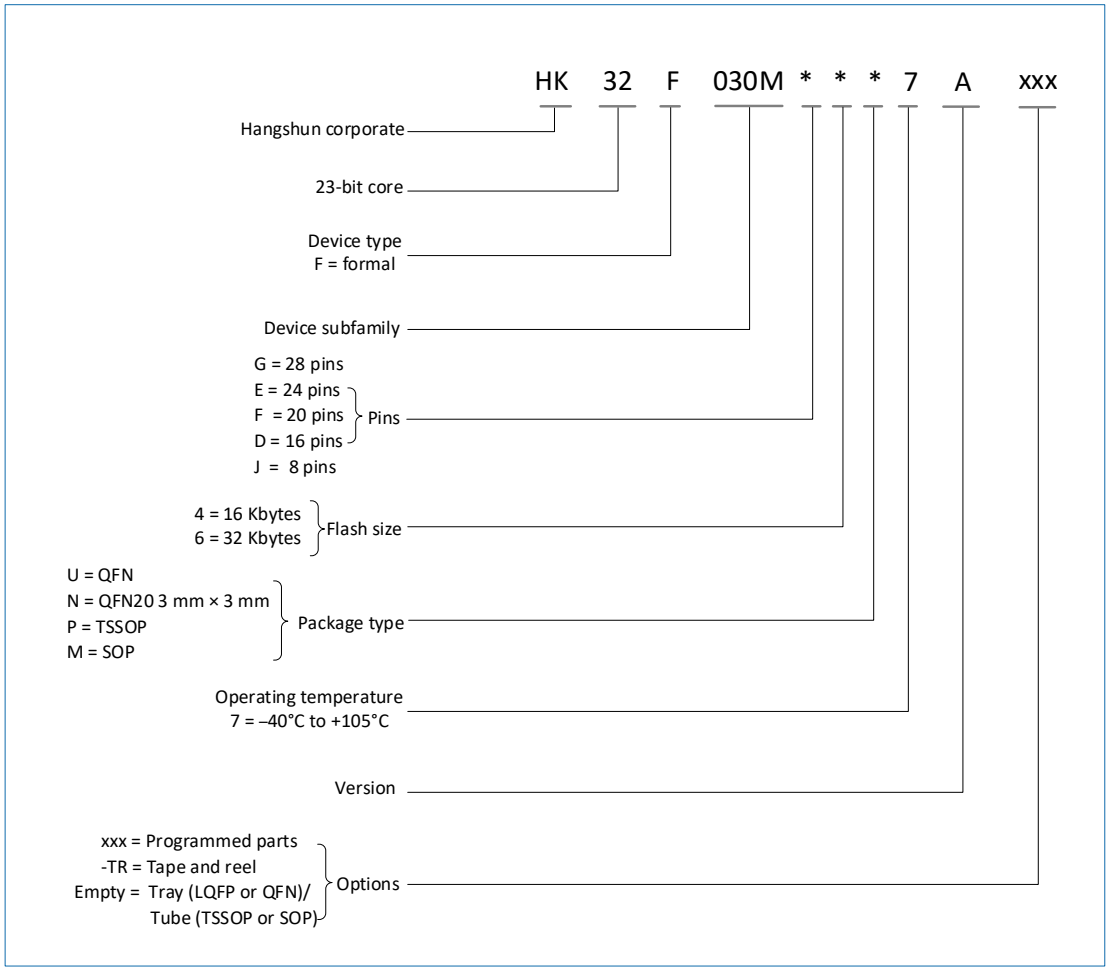


Figure 8-1 HK32F030MxxxxA device numbering conventions

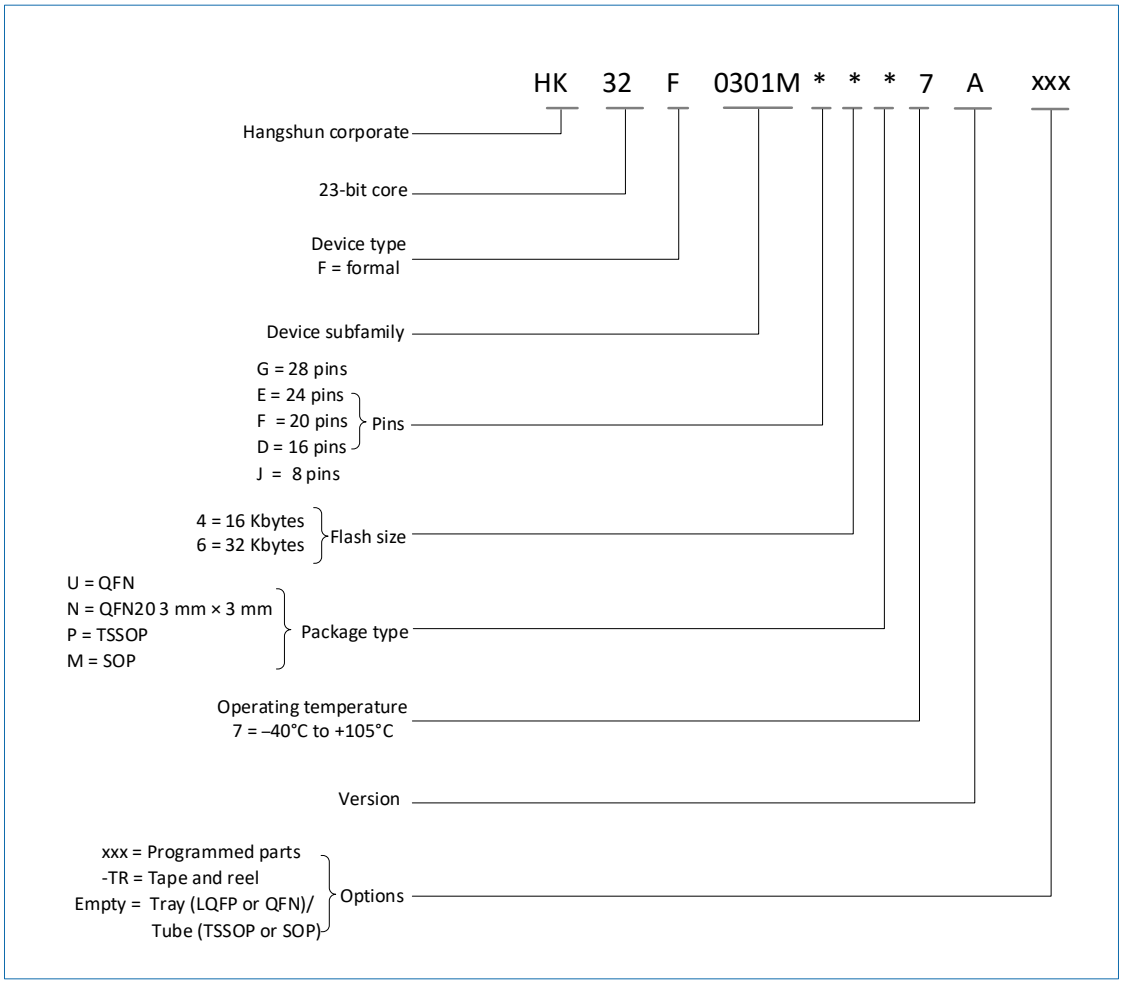


Figure 8-2 HK32F0301MxxxxA device numbering conventions

8.2 Packaging information

Table 8-1 HK32F030MxxxxA packaging information

Package	Part Number	Shipping Option	Remarks
QFN28	HK32F030MG6U7A	Tape and reel/Tray	-
	HK32F030MG4U7A	Tape and reel/Tray	-
QFN24	HK32F030ME6U7A	Tape and reel/Tray	-
	HK32F030ME4U7A	Tape and reel/Tray	-
QFN20	HK32F030MF6U7A	Tape and reel/Tray	The QFN20 package has two types of outlines. For details, see section "7.1.3 QFN20".
	HK32F030MF4U7A	Tape and reel/Tray	
	HK32F030MF4N7A	Tape and reel/Tray	
	HK32F030MF6N7A	Tape and reel/Tray	
TSSOP28	HK32F030MG6P7A	Tape and reel/Tube	
	HK32F030MG4P7A	Tape and reel/Tube	
TSSOP24	HK32F030ME6P7A	Tape and reel/Tube	
	HK32F030ME4P7A	Tape and reel/Tube	
TSSOP20	HK32F030MF6P7A	Tape and reel/Tube	
	HK32F030MF4P7A	Tape and reel/Tube	
TSSOP16	HK32F030MD6P7A	Tape and reel/Tube	
	HK32F030MD4P7A	Tape and reel/Tube	
SOP8	HK32F030MJ6M7A	Tape and reel/Tube	
	HK32F030MJ4M7A	Tape and reel/Tube	

Table 8-2 HK32F0301MxxxxA packaging information

Package	Part Number	Shipping Option	Remarks
QFN28	HK32F0301MG6U7A	Tape and reel/Tray	-
	HK32F0301MG4U7A	Tape and reel/Tray	-
QFN24	HK32F0301ME6U7A	Tape and reel/Tray	-
	HK32F0301ME4U7A	Tape and reel/Tray	-
QFN20	HK32F0301MF6U7A	Tape and reel/Tray	The QFN20 package has two types of outlines. For details, see section "7.1.3 QFN20".
	HK32F0301MF4U7A	Tape and reel/Tray	
	HK32F0301MF4N7A	Tape and reel/Tray	
	HK32F0301MF6N7A	Tape and reel/Tray	
TSSOP28	HK32F0301MG6P7A	Tape and reel/Tube	
	HK32F0301MG4P7A	Tape and reel/Tube	
TSSOP24	HK32F0301ME6P7A	Tape and reel/Tube	
	HK32F0301ME4P7A	Tape and reel/Tube	
TSSOP20	HK32F0301MF6P7A	Tape and reel/Tube	
	HK32F0301MF4P7A	Tape and reel/Tube	
TSSOP16	HK32F0301MD6P7A	Tape and reel/Tube	
	HK32F0301MD4P7A	Tape and reel/Tube	
SOP8	HK32F0301MJ6M7A	Tape and reel/Tube	
	HK32F0301MJ4M7A	Tape and reel/Tube	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CLU	Configurable Logic Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EMACC	Electric Motor Acceleration
EXTI	Extended Interrupt/Event Controller
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

航顺芯片 and other Hangshun trademarks are trademarks of Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). All other trademarks or trade names mentioned in this document are the property of their respective holders.

No part or sub-part of Hangshun product specifications and datasheets may be modified in any form or by any means without consent. Hangshun reserves the right to modify the datasheets and/or products, discontinue any product, or terminate any service without notice. It is recommended that customers obtain relevant information from the latest version and verify that the information is up-to-date and complete before placing an order. All products are sold in accordance with the terms of the sales contract provided at the time of order confirmation. The terms include the scope of warranty, intellectual property rights, and responsibility.

Hangshun guarantees the performance of Hangshun products in accordance with Hangshun's standards during the sales period. Hangshun believes it is necessary to support this warranty by using testing and other quality control techniques. Unless mandatory government regulations are brought in, special tests or measurements by using other instruments are unnecessary.

The customer acknowledges that Hangshun products are not designed or manufactured for purposes related to life support, or for systems or products in dangerous activities or environments. Malfunctioning products may cause personal injuries, deaths, or damage to property or environments (collectively referred to as high-risk activities). The Hangshun products that are used in high-risk activities are not under warranty. Hangshun assumes no liability for customers or third parties involved therein.

Hangshun will provide the same technical support, help, advice, and information as it does now (including the design, development, or debugging of the purchased circuit boards or other applications). Hangshun makes no guarantee and assumes no legal liability for all support technologies, merchantability, or fitness for a particular purpose if the support technologies are error-free and circuit boards and other applications can operate normally.

Shenzhen Hangshun Chip Technology R&D Co., Ltd.

TEL: +86-755-83247667

Website: www.hsxp-hk.com