HK32F0301MxxxxC Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32F0301MxxxxC series microcontrollers (MCUs). This document helps you quickly understand the characteristics and functions of HK32F0301MxxxxC.

Audience

This document is intended for:

- HK32F0301MxxxxC developers
- HK32F0301MxxxxC testers
- HK32F0301MxxxxC users

Release Notes

This document is applicable to HK32F0301MxxxxC series MCUs.

Revision History

Version	Date	Description
1.0	2022/11/21	The initial release.
1.1	2022/11/25	1. Updated Table 2-1 HK32F0301MxxxxC series features. 2. Updated section "4.2.14 ADC characteristics".
1.2	2023/02/16	1. Updated Table 2-1 HK32F0301MxxxxC series features. 2. Updated section "6 Pinouts and pin descriptions".
1.3	2023/07/10	1. Added the table in section "4.2.3 BOR characteristics". 2. Added section "7.2 Device marking".
1.4	2023/09/22	1. Updated section "6.4 QFN20": added the description that the bottom thermal pad is used as VSS pin. 2. Updated section "6.5 Pin descriptions": added the description of pin 0 VSS in the QFN20 package.
1.5	2024/01/04	1. Updated the section “3.8.1 System reset”: modified the “Figure 3-3 Reset signal”. 2. Updated the section “2.1 Features” by modifying the “Typical operating current” data. 3. Updated the section “4.2.5 Operating current characteristics” by modifying the table content.

Contents

1 Introduction

This document is the datasheet for HK32F0301MxxxxC series MCUs. HK32F0301MxxxxC is a family of cost-effective MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32F0301MJ4M7C (SOP8 package)
- HK32F0301MD4P7C (TSSOP16 package)
- HK32F0301MF4P7C (TSSOP20 package)
- HK32F0301MF4x7C
  - HK32F0301MF4U7C (QFN20 package)
  - HK32F0301MF4N7C (QFN20 package)

For more details of HK32F0301MxxxxC, see *HK32F0301MxxxxC User Manual*.

2 Product overview

HK32F0301MxxxxC adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 48 MHz and has 16 Kbytes of Flash and 4 Kbytes of SRAM. You can configure the Flash controller register to remap interrupt vectors in the 16-Kbyte space.

Except for the power pins and ground pins, all the other pins of HK32F0301MxxxxC can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32F0301MxxxxC incorporates a wide selection of communication interfaces:

- 2 × high-speed UARTs of up to 6 Mbit/s
- 1 × high-speed SPI of up to 18 Mbit/s

  The SPI supports the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, and automatic CRC.
- 1 × high-speed I2C of up to 400 kbit/s

  The I2C supports the 100 kbit/s and 400 kbit/s transmission rates, master/slave mode, multimaster mode, 7-bit/10-bit addressing, and SMBus protocol. The I2C can wake up the MCU from Stop mode when receiving data.

HK32F0301MxxxxC embeds a 16-bit advanced PWM timer (four PWM outputs in total, three of which have programmable inserted dead-times), a 16-bit general-purpose PWM timer (four PWM outputs in total), and a 16-bit basic timer (for periodic outputs of CPU interrupts).

HK32F0301MxxxxC also incorporates the analog circuitry: a 1 MSPS ADC, a power-on reset (POR)/power-down reset (PDR)/brown-out reset (BOR) circuit, and an internal reference (sampled by on-chip ADC).

HK32F0301MxxxxC supports multiple power consumption modes. In low-power modes, HK32F0301MxxxxC MCUs can be automatically woken up by the internal low-power timer.

HK32F0301MxxxxC operates in the –40°C to +105°C temperature range, from a 2.4 V to 5.5 V power supply. It meets the environmental requirements of most applications.

With its diversified peripheral interfaces, HK32F0301MxxxxC is suitable for a wide range of applications:

- Programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- CPU core
  - ARM® Cortex™-M0
  - Maximum frequency: 48 MHz
  - 24-bit SysTick timer
  - Supports the remapping of interrupt vectors (by configuring the Flash controller register)
- Operating voltage range: 2.4 V to 5.5 V

- Operating temperature range: –40°C to +105°C
- Typical operating current
  - Run mode: 6.221 mA@48 MHz@5 V
  - Sleep mode: 2.208 mA@48 MHz@5 V
  - Stop mode: 373.354 µA@5 V (LDO in normal operation)
  - Low-power Stop mode: 6.876 µA@5V（LDO in low power mode）
- 16-Kbyte Flash (64 pages, 256 bytes per page; 32-bit reading, 32-bit writing)
  - Separate read and write protection for Flash data
  - 4-Kbyte SRAM
- Cyclic redundancy check (CRC) hardware implementation unit
- Clock
  - High-speed internal clock (HSI): 48 MHz
  - Low-speed internal clock (LSI): 60 kHz
  - GPIO external input clock: 32 MHz (maximum value)
- Reset
  - Low level on the NRST pin (external reset)
  - Window watchdog reset (WWDG reset)
  - Independent watchdog reset (IWDG reset)
  - Power reset
  - Software reset (SW Reset)
  - Low-power management reset
- GPIOs
  - Up to 18 GPIOs
  - Each can be used for external interrupt inputs
  - Built-in switchable pull-up/pull-down resistors
  - Support open-drain outputs
  - Output drive capacity configurable
- Pin multiplexing controller IOMUX
  - In small packages like SOP8 and TSSOP16, the mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX.
- Data communication interface
  - 2 × high-speed UARTs of up to 6 Mbit/s
  - 1 × high-speed I2C of up to 400 kbit/s: can wake up the MCU from Stop mode when receiving data
  - 1 × high-speed SPI of up to 18 Mbit/s
- Timer and PWM generator
  - 1 × 16-bit advanced PWM timer: four PWM outputs in total, three of which have complementary programmable inserted dead-times
  - 1 × 16-bit general-purpose PWM timer (four PWM outputs in total)
  - 1 × 16-bit basic timer (supports CPU interrupts)
  - An auto-wakeup unit timer (AWUT) working in Stop mode
- On-chip analog circuitry

- 1 × 12-bit ADC (1 MSPS, up to seven external analog input channels and two internal channels, differential pair input supported)
- 1 × POR/PDR circuit
- 1 × BOR circuit
- 1 × internal reference voltage (sampled by on-chip ADC)

- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- UID
  - Each HK32F0301MxxxxC MCU provides a 96-bit UID.
- Reliability
  - Passed HBM7000V/CDM2000V/LU800mA level tests.

2.2 Device overview

Table 2-1 HK32F0301MxxxxC series features

Feature		HK32F0301MJ4M7C	HK32F0301MD4P7C	HK32F0301MF4P7C	HK32F0301MF4N7C/ HK32F0301MF4U7C
GPIOs		6	14	18	18
Package		SOP8	TSSOP16	TSSOP20	QFN20
Operating voltage		2.4 V – 5.5 V			
Operating temperature		–40°C to +105°C			
Memory	Flash (Kbyte)	16			
	SRAM (Kbyte)	4			
CPU	Core	Cortex®-M0			
	Frequency	48 MHz			
Clock	LSI	60 kHz			
	HSI	48 MHz			
	External GPIO clock	32 MHz (maximum value)			
Timer	Advanced timer	1 (16-bit): TIM1			
	General-purpose timer	1 (16-bit): TIM2			
	Basic timer	1 (16-bit): TIM6			
	SysTick timer	1			
	AWUT	1			
	IWDG	1			
	WWDG	1			
Comm. interface	UART	2			
	I2C	1			
	SPI	1			

Feature		HK32F0301MJ4M7C	HK32F0301MD4P7C	HK32F0301MF4P7C	HK32F0301MF4N7C/ HK32F0301MF4U7C
ADC	ADC (Channels)	1 (3)	1 (5)	1 (7)	1 (7)
	Reference selection	Internal reference voltage			
	ADC sampling rate	1 MSPS			
	ADC accuracy	12-bit			
CRC		1			
96-bit UID		1			

3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor which provides an MCU platform featuring low cost and low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M0 core, the HK32F0301MxxxxC family is compatible with ARM tools and software.

The following figure shows the block diagram of HK32F0301MxxxxC MCUs:

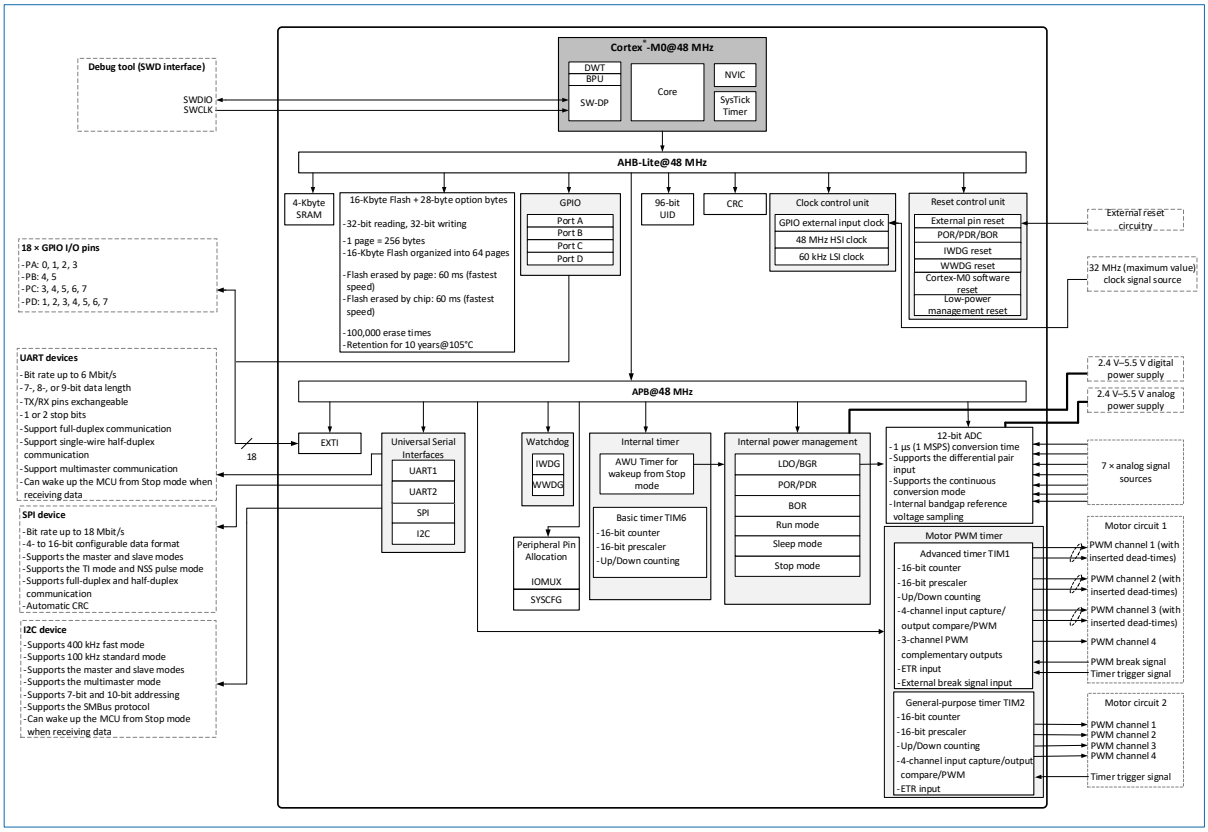

Figure 3-1 HK32F0301MxxxxC block diagram

3.2 Memory mapping

The following figure shows the memory mapping of HK32F0301MxxxxC MCUs:

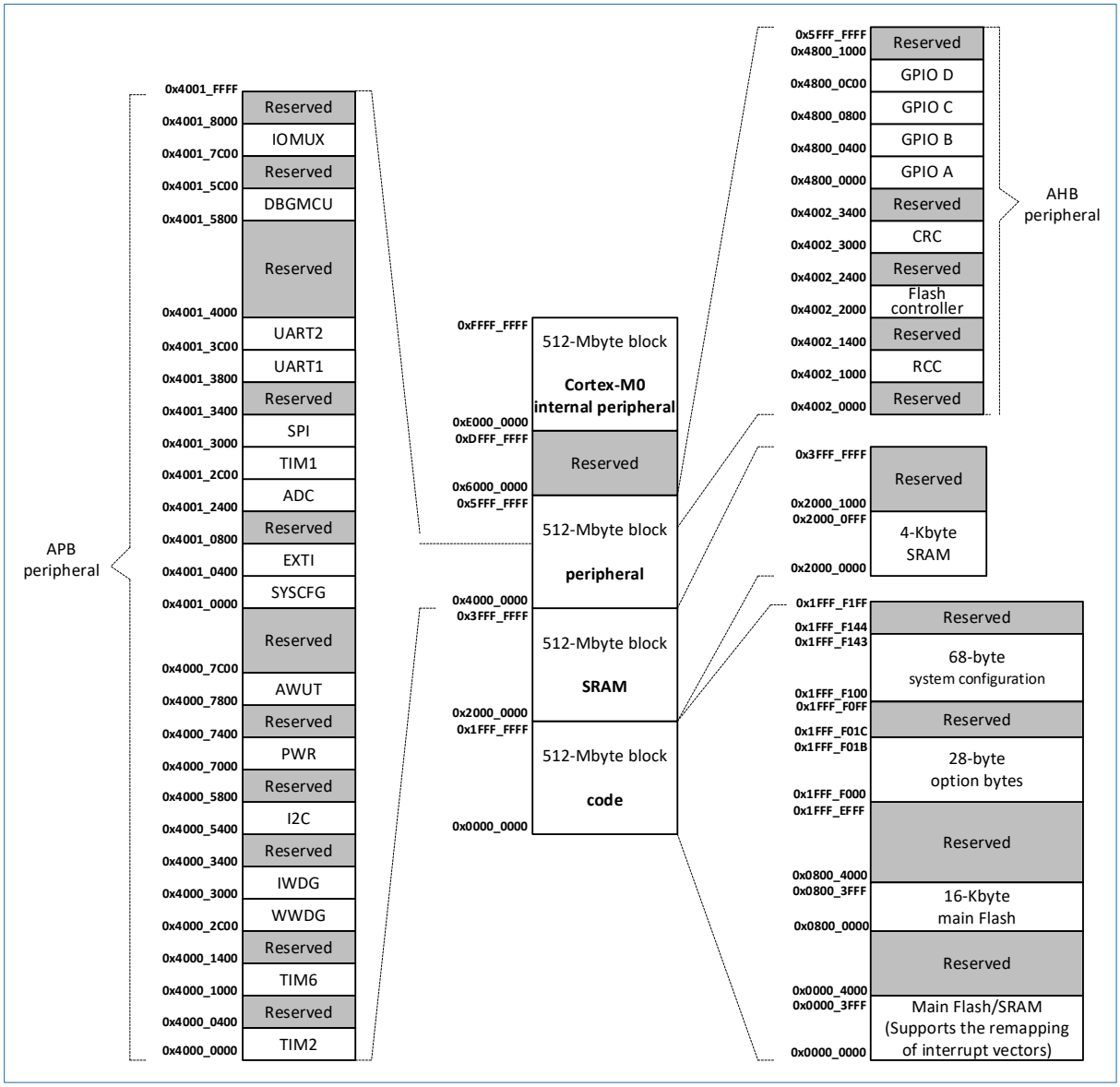

Figure 3-2 HK32F0301MxxxxC memory mapping

3.3 Memory

3.3.1 Flash

HK32F0301MxxxxC integrates a Flash memory of 16 Kbytes to store programs and data.

You can configure the Flash controller register to remap interrupt vectors.

3.3.2 SRAM

HK32F0301MxxxxC integrates a 4-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.4 CRC calculation unit

Cyclic redundancy check (CRC) is used to verify data integrity during transmission and storage. HK32F0301MxxxxC integrates a CRC calculation unit to reduce application processing burden and accelerate processing.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with a reference signature, which is generated at link time and stored at a specified memory location.

3.5 Power supply scheme

HK32F0301MxxxxC has a single power supply. V_{DD} and V_{DDA} supply power to the digital circuitry and analog circuitry of the MCU via the same pin.

V_{DD}/V_{DDA} = 2.4 V – 5.5 V

3.6 Power supply monitor

HK32F0301MxxxxC embeds the power-on reset (POR)/power-down reset (PDR) circuit. (By default, the BOR circuit is disabled). The POR/PDR circuit keeps operating to ensure that the system runs properly when the power supply exceeds 2.4 V. When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuit is required.

3.7 Low-power modes

HK32F0301MxxxxC supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain and the HSI RC oscillator are disabled. MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any external I/O pin.

3.8 Resets

HK32F0301MxxxxC supports the system reset and power reset.

3.8.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain.

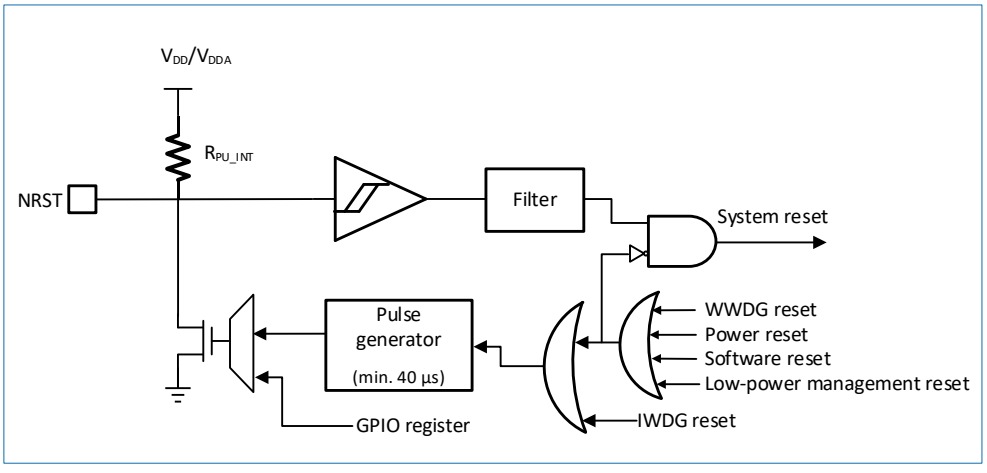

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)

- Power reset
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset

The reset sources finally act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004. The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.8.2 Power reset

A power reset is generated when any of the following events occurs:

- POR/PDR
- BOR

HK32F0301MxxxxC MCUs contain the POR/PDR/BOR circuitry. The POR/PDR circuits keep operating to ensure that the system runs properly when the power supply exceeds 2.4 V. By default, the BOR circuit is disabled. When V_{DD} is less than the POR/PDR/BOR threshold, the MCU will be reset without using any external reset circuit.

3.9 Clocks and clock tree

The following figure shows the clock tree of HK32F0301MxxxxC.

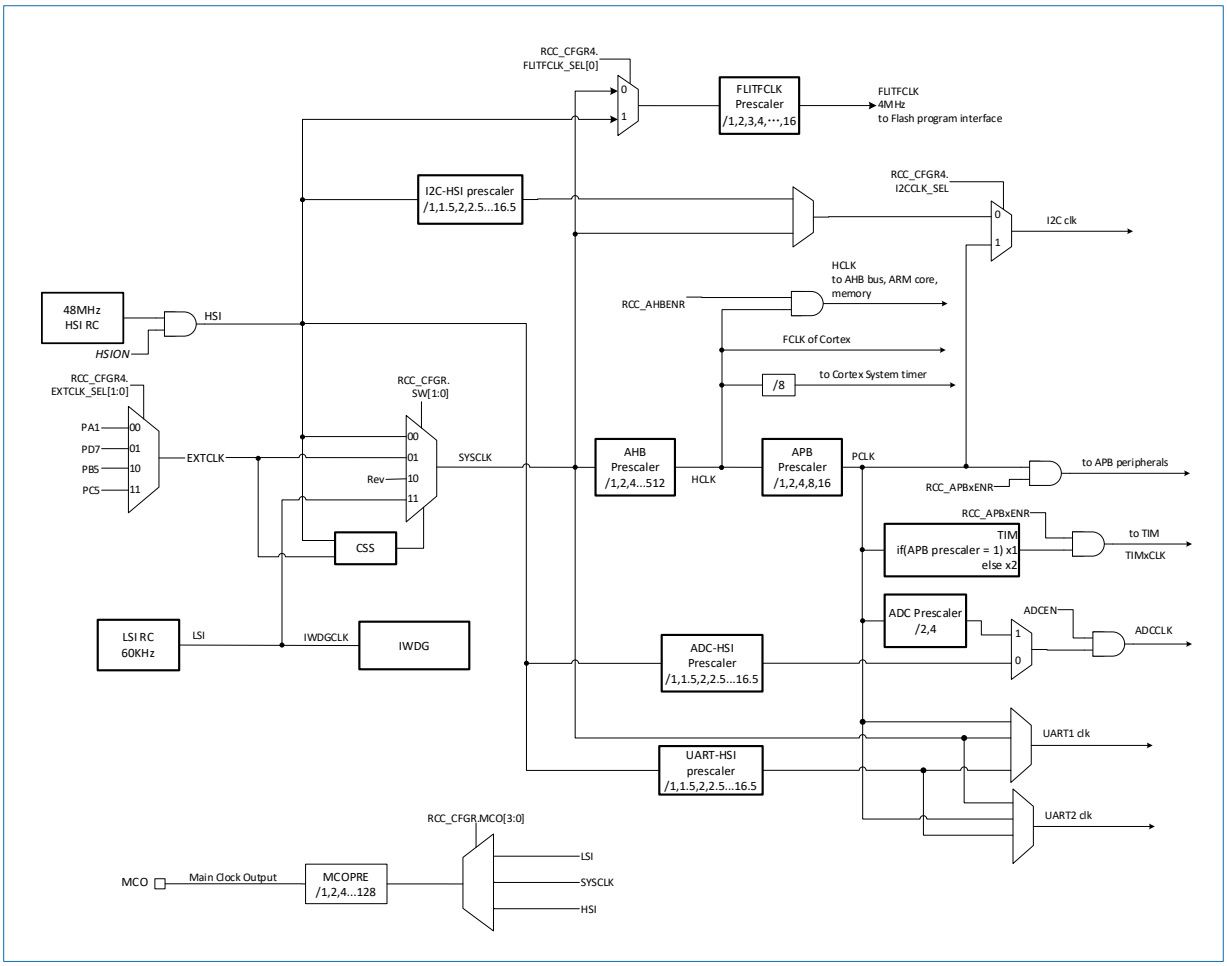

Figure 3-4 Clock tree of HK32F0301MxxxxC

As Figure 3-4 shows, HK32F0301MxxxxC supports the following clock sources:

- High-speed internal clock (HSI): 48 MHz
- Low-speed internal clock (LSI): 60 kHz
- GPIO external input clock: 32 MHz (maximum value)

Each clock source can be enabled and disabled independently. The clock source not in use can be disabled to reduce power consumption. Multiple prescalers are available for the configuration of AHB and APB clock domains. The maximum clock frequency of AHB and APB clock domains is 48 MHz. The AHB clock (HCLK) divided by eight can drive the Cortex system timer (by configuring the Cortex SysTick configuration bit).

All peripheral clocks are driven by the clock (HCLK or PCLK) of the bus to which the peripheral is connected. However, there are some exceptions:

- The Flash programming interface clock (FLITFCLK) is driven by the HSI clock or SYSCLK (selected by using the software).
- The clock source of I2C is one of the following (selected by using the software):
  - SYSCLK
  - 48 MHz HSI divided by I2C-HSI prescaler
  - APB clock (PCLK)
- The FCLK of Cortex is provided by AHB clock (HCLK).
- The clock of AHB, ARM core, and memory is provided by the AHB clock (HCLK).
- The clock source of ADC is one of the following (selected by using the software):
  - APB clock (PCLK) divided by 2 or 4 by the ADC prescaler
  - 48 MHz HSI divided by ADC-HSI prescaler
- The clock source of UART1/UART2 is one of the following (selected by using the software):
  - PCLK
  - SYSCLK
  - 48 MHz HSI divided by UART-HSI prescaler
- The APB clock (PCLK) or the APB clock (PCLK) multiplied by two provides the timer clock. (The clock frequency is selected by using the software and implemented by hardware.)
- The AHB clock (HCLK) divided by eight is used as the external clock of the Cortex SysTick timer. You can set the SysTick control/status register to select HCLK/8 as the SysTick timer clock.

3.10 SYSCFG

The HK32F0301MxxxxC MCU has a set of configuration registers that provide the following functions:

- Remapping memory areas
- Managing the connections between external interrupts and GPIOs
- Managing the reliability feature of the system.

3.11 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. I/O alternate functions can be locked as needed to prevent unexpected writes to the I/O registers.

3.12 IOMUX

In small packages (such as SOP8 and TSSOP16) of HK32F0301MxxxxC, the mapping from multiple GPIOs or

peripheral I/Os to one pin can be implemented by using IOMUX. When a pin is assigned with another alternate function through IOMUX, the pin still provides the functions of a GPIO. The following example illustrates how to use IOMUX to remap functions to pins on a SOP8 package.

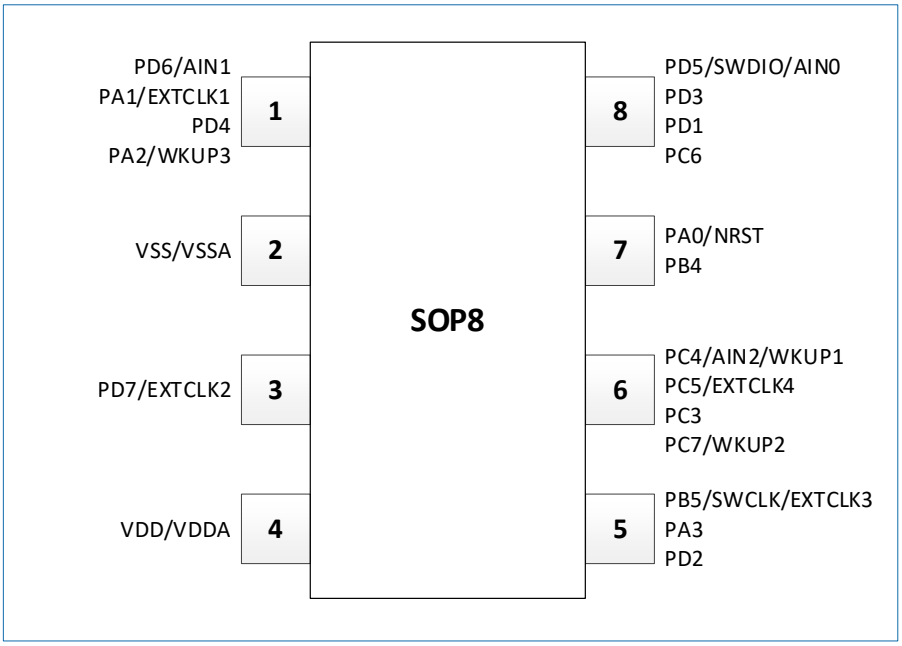

Figure 3-5 SOP8 pinout

After the reset of the MCU, pin 8 is assigned with PD5 by default. You can configure the IOMUX register to remap pin 8 to PD3, PD1, or PC6.

By configuring IOMUX, you can use 18 GPIOs and all internal peripheral I/Os on SOP8 and TSSOP16 packages.

3.13 Interrupts and events

3.13.1 NVIC

HK32F0301MxxxxC incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 22 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities.

- The closely coupled NVIC ensures low-latency interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Closely coupled NVIC core interface
- Supports the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

3.13.2 EXTI

The extended interrupt/event controller (EXTI) manages 11 interrupt lines that are used to generate interrupt/event requests and wake up the system through edge detection. The trigger event of each EXTI line can be configured and masked independently. The trigger event can be a rising edge, a falling edge, or both. The pending register stores the status of each interrupt request. EXTI can detect external interrupt line signals whose pulse width is shorter than the internal clock period. EXTI can be categorized into edge-configurable EXTI and edge-fixed EXTI, whose difference lies in that the interrupt/event trigger edge is configurable or fixed. Among the 11 EXTI lines, up to nine are edge-configurable EXTI lines.

The EXTI lines from EXTI 0 to EXTI 7 are connected to I/O pins. The connections of the other EXTI lines are as follows:

- EXTI 8 connected to the ADC AWD event
- EXTI 10 connected to the I2C wakeup event
- EXTI 11 connected to the AWU wakeup event

EXTI lines from EXTI 8 to EXTI 10 are connected to fixed events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). EXTI lines from EXTI 8 to EXTI 10 can detect the rising edge of events and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system only in Stop mode. The corresponding interrupt control bit and status bit are stored in the peripheral from which events are generated.

3.14 ADC

The ADC of HK32F0301MxxxxC has the following features:

- A total of nine channels. Channels AIN0 to AIN6 are external channels connected to I/O pins. AIN7 is an internal channel connected to the internal PMU (only for the calibration of internal power supply voltage). AIN8 is an internal channel connected to the internal reference voltage.
- Supports the differential pair input mode. AIN0 and AIN1, AIN2 and AIN3, AIN4 and AIN5 form three differential pairs. (When ADC is configured to the differential pair input mode, AIN7 and AIN8 act as ADC channels for the sampling of the internal PMU and reference voltage. AIN6, AIN7, and AIN8 are unavailable.)
- Supports only the 12-bit ADC sampling resolution.

3.15 Timer

The HK32F0301MxxxxC MCU has an advanced timer, a general-purpose timer, and a basic timer. The features of the timers are listed in the following table.

Table 3-1 Features of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	1 to 65536	No	Yes	4	3
General-purpose timer	TIM2	16-bit	Up, down, up/down	1 to 65536	No	No	4	No
Basic timer	TIM6	16-bit	Up, down	1 to 65536	No	No	No	No

3.15.1 Advanced timer

HK32F0301MxxxxC integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output
- Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Many functions of TIM1 are

the same as those of the general-purpose timer. Therefore, TIM1 can work together with the general-purpose timer through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

3.15.2 General-purpose timer

HK32F0301MxxxxC integrates a 4-channel general-purpose timer TIM2.

TIM2 can generate PWM outputs or serve as a simple time benchmark. TIM2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. In debug mode, the counter can be frozen.

TIM2 can work with the advanced timer through the Timer Link feature for synchronization and event chaining. Additionally, TIM2 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors.

3.15.3 Basic timer

HK32F0301MxxxxC integrates a basic timer TIM6.

TIM6 embeds a 16-bit up/down counter and a 16-bit prescaler. It is used to generate periodic CPU interrupt requests. In debug mode, the counter can be frozen.

3.16 AWUT

HK32F0301MxxxxC provides an auto-wakeup timer (AWUT). The AWUT can count and generate an interrupt to wake up the MCU from Stop mode. An ultra-low-power 22-bit timer is embedded in the AWUT. The operating clock of AWUT can be the GPIO input clock or the low-speed internal (LSI) clock. The AWUT adopts the down-counting mode.

3.17 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent RC oscillator (LSI). The RC oscillator is independent of the main clock, so it can operate in Stop mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use IWDG in window mode.

3.18 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.19 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.20 I2C bus

The I2C bus interface can work as a master or slave and supports the standard and fast modes. The I2C bus interface supports the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C

interface embeds hardware CRC generation/verification and supports SMBus V2.0/PMBus.

Table 3-2 I2C features

I2C Feature	I2C
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast mode	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

3.21 UART

HK32F0301MxxxxC embeds two universal asynchronous receivers/transmitters (UART1/UART2). The UARTs provide hardware management of multiprocessor communication mode and single-wire half-duplex communication mode. The UARTs are in a clock domain independent of the CPU clock.

Table 3-3 UART features

UART Mode/Feature	UART1/2
Data word length	7/8/9-bit
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported
Dual clock domains	Supported

3.22 SPI

HK32F0301MxxxxC has a serial peripheral interface (SPI) communicating at up to 18 Mbit/s. The SPI interface can work as the master or slave and supports full-duplex and half-duplex communication. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4-bit to 16-bit. The SPI interface supports the CRC and TI mode. The following table lists the features of the SPI interface.

Table 3-4 SPI features

SPI Feature	SPI
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported

3.23 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32F0301MxxxxC MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process of the security mechanism.

3.24 Debug port

Based on the ARM SWJ-DP embedded in HK32F0301MxxxxC, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Note:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	5.8	V
V_{IN}	Input voltage on pins	–0.3	5.8	
$\|V_{SSX} – V_{SS}\|$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	105	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	30	
	Output current sourced by any I/O and control pin	30	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–55	130	°C
T_J	Maximum junction temperature	–45	125	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	48	
V_{DD}	Standard operating voltage	2.4	5.5	V
V_{DDA}(1)	Analog operating voltage	2.4	5.5	V
T_A	Operating temperature	–40	105	°C

(1). V_{DDA} is connected to V_{DD} on the chip.

4.2.2 POR/PDR characteristics

Table 4-5 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge	1.68	1.80	1.93	V
		Rising edge	1.85	1.96	2.07	V
$V_{PDRhyst}$	PDR hysteresis	-	140	160	170	mV
$t_{RSTTEMPO}$(2)	Reset duration	-	-	2	-	ms

(1) PDR and POR are based on the monitoring of only V_{DD}.

(2) The value is guaranteed in design.

4.2.3 BOR characteristics

Table 4-6 BOR characteristics

Symbol	Parameter	Condition (–40°C to 105°C)	Min	Typ	Max	Unit
V_{BOR}(1)	BOR detection level selection (V_{DD} rising edge)	V_{BOR1}	2.62	2.85	3.07	V
		V_{BOR2}	3.04	3.21	3.53	
		V_{BOR3}	3.45	3.64	4.01	
		V_{BOR4}	3.89	4.04	4.46	
		V_{BOR5}	4.30	4.57	5.01	
		V_{BOR6}	4.80	5.03	5.49	
		V_{BOR7}	5.23	5.49	5.97	
	BOR detection level selection (V_{DD} falling edge)	V_{BOR1}	2.46	2.59	2.83	
		V_{BOR2}	2.84	2.99	3.26	
		V_{BOR3}	3.24	3.40	3.70	
		V_{BOR4}	3.68	3.80	4.14	
		V_{BOR5}	4.06	4.19	4.58	
		V_{BOR6}	4.46	4.62	5.03	
		V_{BOR7}	4.84	5.05	5.48	
t_{BORRST}(2)	Time for BOR to take effect after reaching the threshold	-	-	10	-	μs

(1) BOR is based on the monitoring of only V_{DD}.

(2) The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	-	1.2	-	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition	Parameter	–40°C, V_{DD} = 5 V	25°C, V_{DD} = 5 V	105°C, V_{DD} = 5 V	Unit
Run	**HCLK = 48 MHz**; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled**; **Two** wait states to access Flash.	Operating current	6.194	6.221	6.213	mA

Mode	Condition	Parameter	–40°C, V_{DD} = 5 V	25°C, V_{DD} = 5 V	105°C, V_{DD} = 5 V	Unit
	HCLK = 8MHz; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled**; **Zero** wait states to access Flash.	Operating current	2.704	2.751	2.782	mA
Sleep	**HCLK = 48 MHz;** AHB/APB disabled; Core clock disabled; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals **disabled;** SRAM and peripheral data retained.	Operating current	2.184	2.208	2.301	mA
		Wakeup time	-	2.72	-	µs
	HCLK = 8 MHz; AHB/APB disabled; Core clock disabled; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals **disabled;** SRAM and peripheral data retained.	Operating current	1.227	1.361	1.390	mA
		Wakeup time	-	2.72	-	µs
	HCLK = 60 kHz; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled;** **Zero** wait states to access Flash.	Operating current	0.875	0.997	1.014	mA
		Wakeup time	-	1.63	-	ms
Stop	All clocks in the core domain stopped; HSI and LSI oscillators disabled; LDO operating in normal mode; All I/Os configured in high impedance; Except for AWUT, all the other peripherals disabled.	Operating current	343.475	373.354	453.543	µA
		Wakeup time	-	32.4	-	µs
Low-power Stop	All clocks stopped; HSI and LSI oscillators disabled; LDO operating in low-power mode; All I/Os configured in high impedance; All peripherals disabled, including AWUT.	Operating current	5.705	6.876	27.260	µA
		Wakeup time	-	125.5	-	µs

4.2.6 HSI clock characteristics

Table 4-9 HSI clock characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-		-	48	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-		45	-	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user		–1	-	1	
		Factory calibrated	T_A = –40°C to +105°C	–1.6	-	1.6	%
$T_{su\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		-	5	8	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	-		-	70	85	µA

(1). The value is guaranteed in design.

4.2.7 LSI clock characteristics

Table 4-10 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	60	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	50	150	µs

$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	0.2	-	μA

(1). The value is guaranteed in design.

4.2.8 GPIO external clock input characteristics

Table 4-11 Characteristics of the input GPIO external clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{GPIO_ext}	External clock source frequency	-	0	-	32	MHz
DuCy $_{(HSE)}$(1)	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.9 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-word programming time	-	20	-	μs
T_{ERASE}	Page erase time	30	60	80	ms
	Mass erase time	30	60	80	ms
I_{DDPROG}	One-byte programming current	-	-	5	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	2	mA
I_{DDREAD}	Supply current@24 MHz (read mode)	-	2	3	mA
	Supply current@1 MHz (read mode)	-	0.25	0.4	mA
N_{END}	Erasure endurance	100,000	-	-	Cycles
t_{RET}	Data retention	10	-	-	Years

4.2.10 I/O pin input characteristics

Table 4-13 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	-	0.65 × V_{DD}	-	-	V
V_{IL}	Input low level voltage	-	-	-	0.2 × V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD} = 5 V	2.31	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 5 V	-	-	2.23	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 5 V	80	-	-	mV
I_{lkg}	Input leakage current	V_{DD} = 5 V; 0 < V_{IN} < 5 V	-	5	-	nA
		V_{DD} = 3.3 V; V_{IN} = 5 V	-	5	-	nA
R_{PU}	Pull-up resistor	-	-	33	-	kΩ
R_{PD}	Pull-down resistor	-	-	33	-	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The value is guaranteed in design.

4.2.11 I/O pin output characteristics

Table 4-14 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}			V
V_{OL}	Output low level voltage	2.4 V ≤ V_{DD} ≤ 5.5 V			0.2 × V_{DD}	V

Table 4-15 I/O pin output drive characteristics

Drive Level	V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
	Sink current	Source current	Sink current	Source current	
Level1	4.17	5.24	7.86	17.83	mA
Level2	16.86	13.64	28.29	45.89	mA

Level3	23.73	16.78	39.82	59.93	mA

4.2.12 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-16 NRST pin input characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{Noise}	Low level ignored duration	-	-	80	ns

4.2.13 TIM timer characteristics

Table 4-17 TIM pin input characteristics(1)

Symbol	Parameter	Min	Max	Unit
F_{EXT}	Timer external clock frequency	-	$f_{TIMxCLK}/2$	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 48MHz.

4.2.14 ADC characteristics

Table 4-18 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when ADC is enabled	-	2.4	5	5.5	V
V_{REFP}	Positive reference voltage	-	2.4	5	5.5	V
V_{REFN}	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	12	28	MHz
f_S (1)	Sampling frequency	f_{ADC} = 12 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 12 MHz	-	-	706	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	V_{REFN}	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	For details, see Table 4-19.				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	2	kΩ
C_{ADC}(1)	Sampling and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S(2)	Sampling time	f_{ADC} = 12 MHz	1.5	-	239	Cycles
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz 12-bit resolution	14	-	252	Cycles

(1) The value is guaranteed in design.

(2) The value is measured based on the ADC clock. The register access latency is not taken into account.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f}_{ADC} \times \boldsymbol{C}_{ADC} \times \ln(2^{N+2})} - \boldsymbol{R}_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-19 Maximum input impedance values (f_{ADC} = 12 MHz)

Sampling Cycles Ts (Cycles)	Sampling Time tS (μs)	Maximum Input Impedance (kΩ)
1.5	0.13	0.58
7.5	0.63	10.88
13.5	1.13	21.19
28.5	2.38	46.95
41.5	3.46	69.28
55.5	4.63	93.32
71.5	5.96	120.80
239.5	19.96	409.34

Table 4-20 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	V_{DD} = V_{DDA} = 5 V f_{ADC} = 12 MHz, Test after ADC calibration	-	3	LSB
EO	Offset error(2)		-	1	
EG	Gain error(3)		-	1	
ED	Differential linearity error(4)		-	4	
EL	Integral linearity error(5)		-	2	

(1). Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3). Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4). Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5). Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With restricted V_{DDA}, frequency, and temperature ranges, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

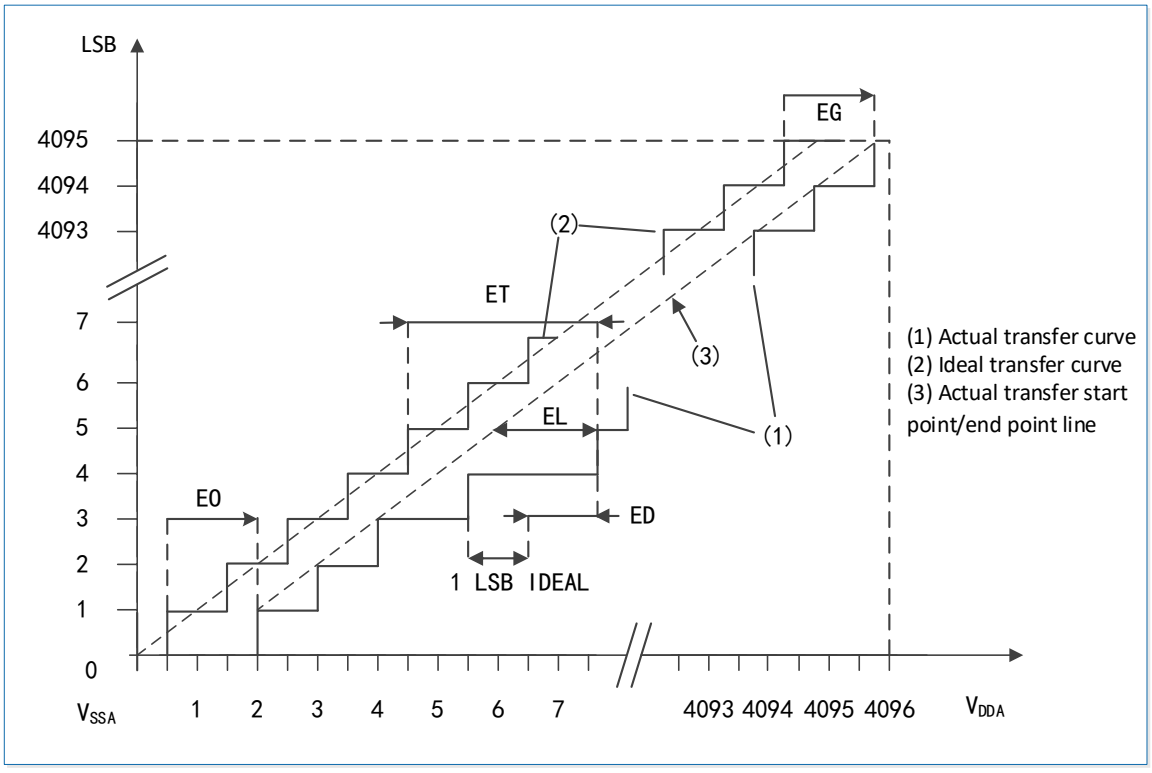

Figure 4-1 ADC accuracy characteristics

Note: For the explanations of EO, ET, EG, EL, and ED, see Table 4-20.

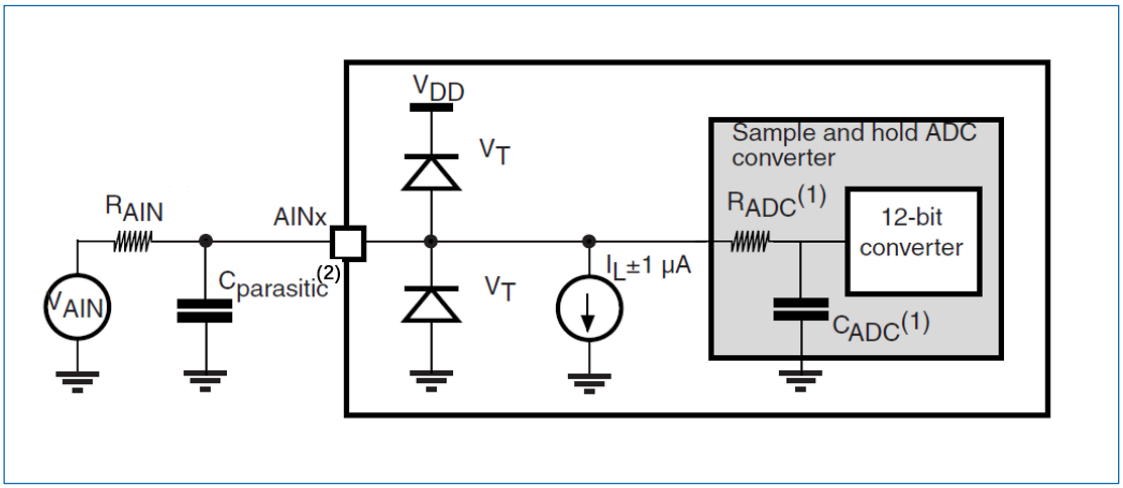

Figure 4-2 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-18.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

5 Typical circuitry

5.1 Power supply scheme

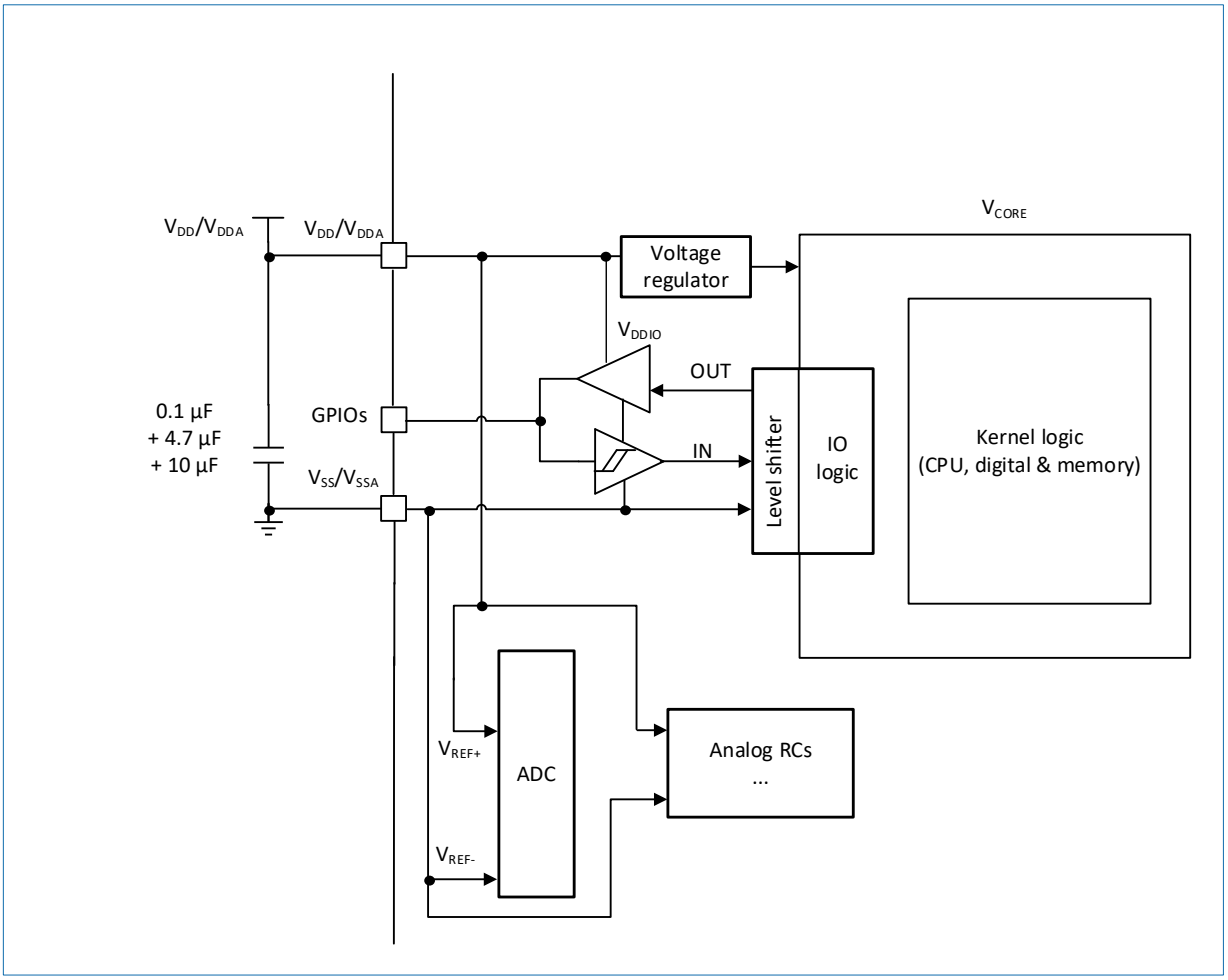

Figure 5-1 Power supply reference circuitry

6 Pinouts and pin descriptions

HK32F0301MxxxxC MCUs are offered in SOP8, TSSOP16, TSSOP20, and QFN20 packages. The pinouts of the packages are as follows:

6.1 SOP8

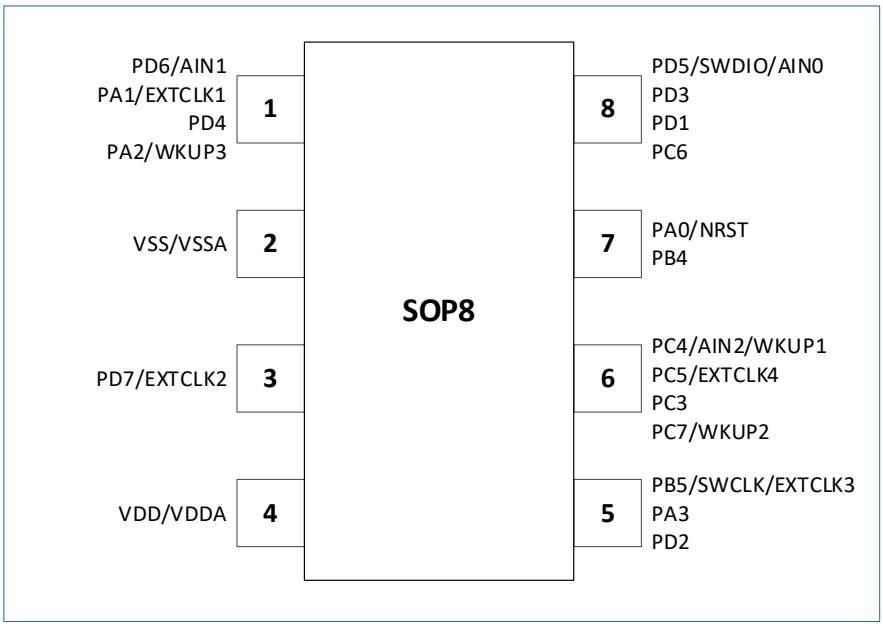

Figure 6-1 SOP8 pinout

6.2 TSSOP16

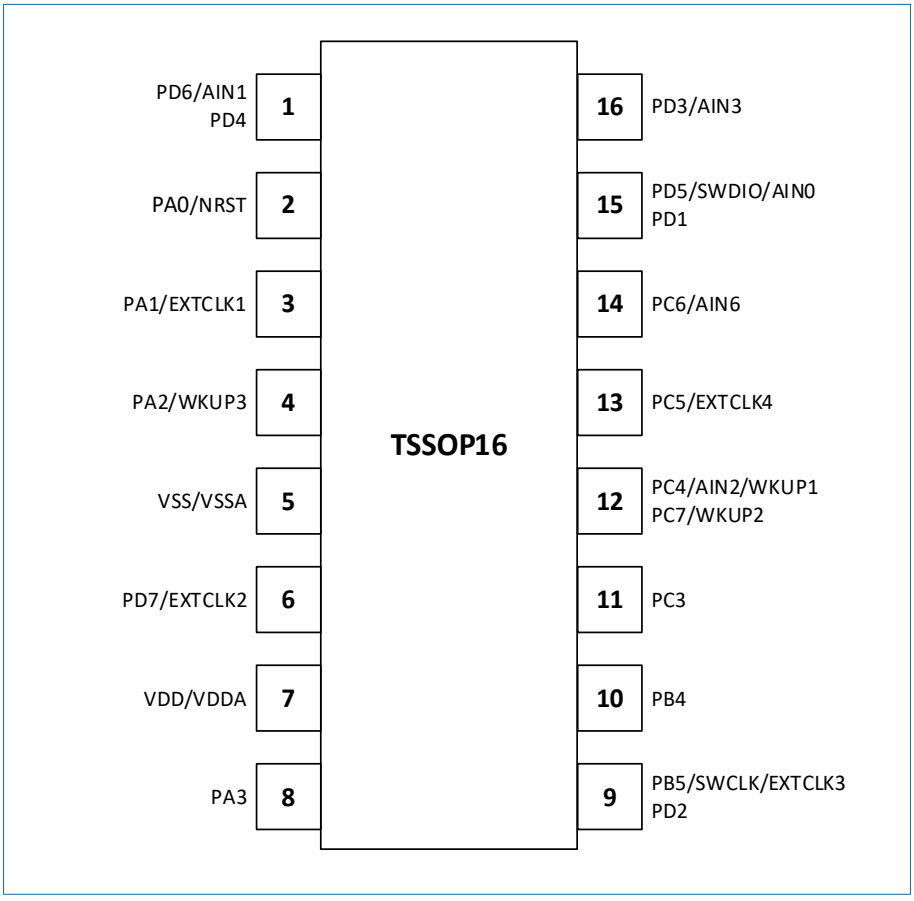

Figure 6-2 TSSOP16 pinout

6.3 TSSOP20

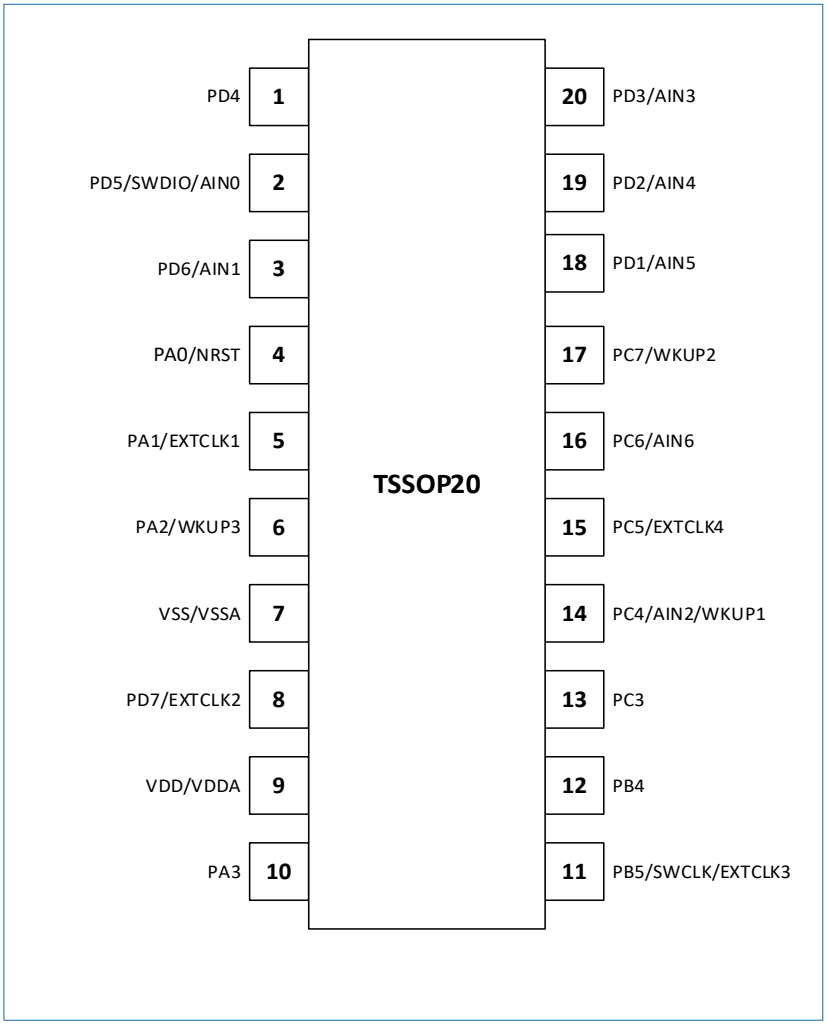

Figure 6-3 TSSOP20 pinout

6.4 QFN20

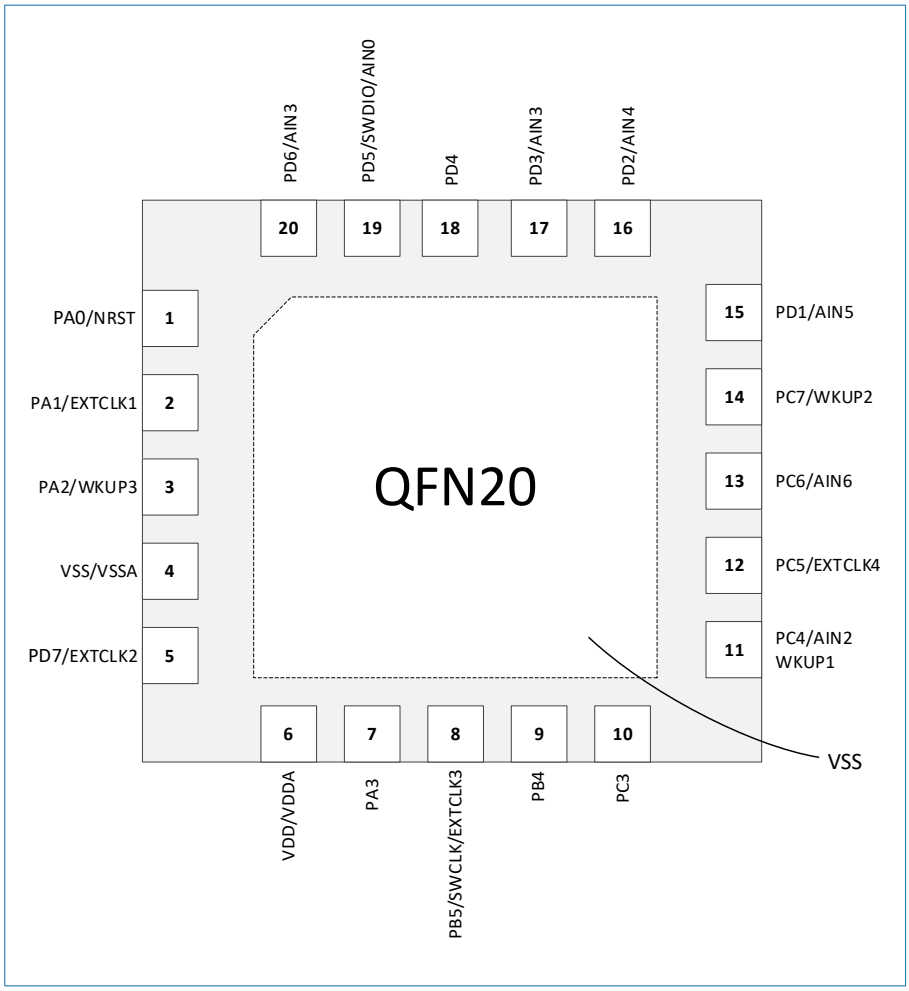

Figure 6-4 QFN20 pinout

6.5 Pin descriptions

Table 6-1 Pin description of each package

QFN20	TSSOP20	TSSOP16	SOP8	Pin Name (default function after resets)	Pin Type[1]	5 V-tolerant	Alternate Function	Additional Function
0	-	-	-	VSS	S	-	Ground (Pin 0 is the thermal pad on the QFN package bottom.)	
1	4	2	7	NRST_PA0	I/O	FT[4]	I2C_SMBA UART1_TX UART2_TX SPI_NSS TIM1_BKIN TIM2_CH3 ADC_ETR	NRST EXTI0
2	5	3	1	PA1	I/O	FT	ADC_ETR I2C_SCL UART1_TX UART2_TX SPI_SCK TIM1_CH1N TIM2_ETR	EXTCLK1 EXTI1
3	6	4	1	PA2	I/O	FT	ADC_ETR I2C_SMBA UART1_RX	EXTI2 WKUP3

QFN20	TSSOP20	TSSOP16	SOP8	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
							UART2_RX SPI_SCK TIM1_CH2N TIM2_CH4	
4	7	5	2	VSS/VSSA	S		Ground	
5	8	6	3	PD7	I/O	FT	ADC_ETR I2C_SMBA UART1_RX UART2_RX SPI_NSS TIM1_BKIN TIM1_CH3 TIM2_CH1	EXTCLK2_MCO EXTI7
6	9	7	4	VDD/VDDA	S		Power supply	
7	10	8	5	PA3	I/O	FT	MCO ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_NSS TIM1_CH3N TIM2_CH3	EXTI3
8	11	9	5	PB5	I/O	FT	SWCLK ADC_ETR I2C_SDA UART1_RX UART2_RX SPI_NSS TIM1_BKIN TIM2_CH2	EXTCLK3 EXTI5
9	12	10	7	PB4	I/O	FT	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_MISO TIM1_CH2N TIM2_ETR	EXTI4
10	13	11	6	PC3	I/O	FT	MCO ADC_ETR I2C_SCL UART1_TX UART2_TX SPI_MOSI TIM1_CH1N TIM1_CH3 TIM2_CH1	EXTI3
11	14	12	6	PC4	I/O	-	ADC_ETR I2C_SDA UART1_RX UART2_RX SPI_MISO TIM1_CH2N TIM1_CH4 TIM2_CH4	WKUP1 EXTI4 ADC_AIN2
12	15	13	6	PC5	I/O	FT	ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_SCK TIM1_ETR TIM2_CH1	EXTCLK4 EXTI5
13	16	14	8	PC6	I/O	-	ADC_ETR I2C_SCL	EXTI6 ADC_AIN6(2)

QFN20	TSSOP20	TSSOP16	SOP8	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
							UART1_RX UART2_RX SPI_MOSI TIM1_CH1 TIM2_CH3	
14	17	12	6	PC7	I/O	FT	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_MISO TIM1_CH2 TIM2_ETR	EXTI7 WKUP2
15	18	15	8	PD1	I/O	-	ADC_ETR I2C_SMBA UART1_TX UART2_TX SPI_MOSI TIM1_CH1 TIM2_CH4	EXTI1 ADC_AIN5(2)
16	19	9	5	PD2	I/O	-	ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_MOSI TIM1_CH2 TIM2_CH3	EXTI2 ADC_AIN4(2)(3)
17	20	16	8	PD3	I/O	-	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_SCK TIM1_CH3 TIM2_CH2	EXTI3 ADC_AIN3(2)
18	1	1	1	PD4	I/O	FT	MCO ADC_ETR I2C_SMBA UART1_TX UART2_TX SPI_MOSI TIM1_CH4 TIM2_CH1	EXTI4
19	2	15	8	PD5	I/O	-	MCO SWDIO ADC_ETR UART1_TX UART2_TX SPI_MISO TIM1_ETR TIM2_ETR	EXTI5 ADC_AIN0
20	3	1	1	PD6	I/O	-	MCO ADC_ETR I2C_SMBA UART1_RX UART2_RX SPI_MISO TIM1_CH2 TIM2_CH2	EXTI6 ADC_AIN1

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). This function is not supported in the SOP8 package.

(3). This function is not supported in the SOP16 package.

(4). FT= 5 V tolerant.

Note: Unless otherwise specified, all I/Os are configured in analog mode during and after resets.

6.6 IOMUX

In small packages (such as SOP8 and TSSOP16) of HK32F0301MxxxxC, the mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX.

6.6.1 IOMUX of the SOP8 package

Table 6-2 SOP8 IOMUX table

Pin	Map To	Pin Type	5 V-tolerant	Alternate Function	Additional Function
1	PD6 (default)	I/O	-	MCO ADC_ETR I2C_SMBA UART1_RX UART2_RX SPI_MISO TIM1_CH2 TIM2_CH2	EXTI6 ADC_AIN1
	PA1	I/O	FT(1)	ADC_ETR I2C_SCL UART1_TX UART2_TX SPI_SCK TIM1_CH1N TIM2_ETR	EXTCLK1 EXTI1
	PD4	I/O	FT	MCO ADC_ETR I2C_SMBA UART1_TX UART2_TX SPI_MOSI TIM1_CH4 TIM2_CH1	EXTI4
	PA2	I/O	FT	ADC_ETR I2C_SMBA UART1_RX UART2_RX SPI_SCK TIM1_CH2N TIM2_CH4	EXTI2 WKUP3
5	PB5 (default)	I/O	FT	SWCLK ADC_ETR I2C_SDA UART1_RX UART2_RX SPI_NSS TIM1_BKIN TIM2_CH2	EXTCLK3 EXTI5
	PA3	I/O	FT	MCO ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_NSS TIM1_CH3N TIM2_CH3	EXTI3
	PD2	I/O	-	ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_MOSI TIM1_CH2 TIM2_CH3	EXTI2
6	PC4 (default)	I/O	-	ADC_ETR	WKUP1

Pin	Map To	Pin Type	5 V-tolerant	Alternate Function	Additional Function
				I2C_SDA UART1_RX UART2_RX SPI_MISO TIM1_CH2N TIM1_CH4 TIM2_CH4	EXTI4 ADC_AIN2
	PC3	I/O	FT	MCO ADC_ETR I2C_SCL UART1_TX UART2_TX SPI_MOSI TIM1_CH1N TIM1_CH3 TIM2_CH1	EXTI3
	PC5	I/O	FT	ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_SCK TIM1_ETR TIM2_CH1	EXTCLK4 EXTI5
	PC7	I/O	FT	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_MISO TIM1_CH2 TIM2_ETR	EXTI7 WKUP2
7	NRST_PA0 (default)	I/O	FT	I2C_SMBA UART1_TX UART2_TX SPI_NSS TIM1_BKIN TIM2_CH3 ADC_ETR	NRST EXTI0
	PB4	I/O	FT	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_MISO TIM1_CH2N TIM2_ETR	EXTI4
8	PD5 (default)	I/O	-	MCO SWDIO ADC_ETR UART1_TX UART2_TX SPI_MISO TIM1_ETR TIM2_ETR	EXTI5 ADC_AIN0
	PD3	I/O	-	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_SCK TIM1_CH3 TIM2_CH2	EXTI3
	PD1	I/O	-	ADC_ETR I2C_SMBA UART1_TX UART2_TX SPI_MOSI TIM1_CH1	EXTI1

Pin	Map To	Pin Type	5 V-tolerant	Alternate Function	Additional Function
				TIM2_CH4	
	PC6	I/O	-	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_MOSI TIM1_CH1 TIM2_CH3	EXTI6

(1). FT= 5 V tolerant.

6.6.2 IOMUX of the TSSOP16 package

Table 6-3 TSSOP16 IOMUX table

Pin	Map To	Pin Type	5 V-tolerant	Alternate Function	Additional Function
1	PD6 (default)	I/O	-	MCO ADC_ETR I2C_SMBA UART1_RX UART2_RX SPI_MISO TIM1_CH2 TIM2_CH2	EXTI6 ADC_AIN1
	PD4	I/O	FT(1)	MCO ADC_ETR I2C_SMBA UART1_TX UART2_TX SPI_MOSI TIM1_CH4 TIM2_CH1	EXTI4
9	PB5 (default)	I/O	FT	SWCLK ADC_ETR I2C_SDA UART1_RX UART2_RX SPI_NSS TIM1_BKIN TIM2_CH2	EXTCLK3 EXTI5
	PD2	I/O	-	ADC_ETR I2C_SDA UART1_TX UART2_TX SPI_MOSI TIM1_CH2 TIM2_CH3	EXTI2
12	PC4 (default)	I/O	-	ADC_ETR I2C_SDA UART1_RX UART2_RX SPI_MISO TIM1_CH2N TIM1_CH4 TIM2_CH4	WKUP1 EXTI4 ADC_AIN2
	PC7	I/O	FT	ADC_ETR I2C_SCL UART1_RX UART2_RX SPI_MISO TIM1_CH2 TIM2_ETR	EXTI7 WKUP2
15	PD5 (default)	I/O	-	MCO SWDIO ADC_ETR UART1_TX	EXTI5 ADC_AIN0

Pin	Map To	Pin Type	5 V-tolerant	Alternate Function	Additional Function
				UART2_TX SPI_MISO TIM1_ETR TIM2_ETR	
	PD1	I/O	FT	ADC_ETR I2C_SMBA UART1_TX UART2_TX SPI_MOSI TIM1_CH1 TIM2_CH4	EXTI1

(1). FT= 5 V tolerant.

6.7 Alternate function table

Table 6-4 Alternate function table

Pin Name	AF0 (I2C/SWD)	AF1 (UART1)	AF2 (SPI)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6 (UART2)	AF7 (ADC)
PA0	I2C_SMBA	UART1_TX	SPI_NSS	TIM1_BKIN	TIM2_CH3	-	UART2_TX	ADC_ETR
PA1	I2C_SCL	UART1_TX	SPI_SCK	TIM1_CH1N	TIM2_ETR	-	UART2_TX	ADC_ETR
PA2	I2C_SMBA	UART1_RX	SPI_SCK	TIM1_CH2N	TIM2_CH4	-	UART2_RX	ADC_ETR
PA3	I2C_SDA	UART1_TX	SPI_NSS	TIM1_CH3N	TIM2_CH3	RCC_MCO	UART2_TX	ADC_ETR
PB4	I2C_SCL	UART1_RX	SPI_MISO	TIM1_CH2N	TIM2_ETR	-	UART2_RX	ADC_ETR
PB5	SWCLK/I2C_SDA (1)	UART1_RX	SPI_NSS	TIM1_BKIN	TIM2_CH2	-	UART2_RX	ADC_ETR
PC3	I2C_SCL	UART1_TX	SPI_MOSI	TIM1_CH3/TIM1_CH1N (1)	TIM2_CH1	RCC_MCO	UART2_TX	ADC_ETR
PC4	I2C_SDA	UART1_RX	SPI_MISO	TIM1_CH4/TIM1_CH2N (1)	TIM2_CH4	-	UART2_RX	ADC_ETR
PC5	I2C_SDA	UART1_TX	SPI_SCK	TIM1_ETR	TIM2_CH1	-	UART2_TX	ADC_ETR
PC6	I2C_SCL	UART1_RX	SPI_MOSI	TIM1_CH1	TIM2_CH3	-	UART2_RX	ADC_ETR
PC7	I2C_SCL	UART1_RX	SPI_MISO	TIM1_CH2	TIM2_ETR	-	UART2_RX	ADC_ETR
PD1	I2C_SMBA	UART1_TX	SPI_MOSI	TIM1_CH1	TIM2_CH4	-	UART2_TX	ADC_ETR
PD2	I2C_SDA	UART1_TX	SPI_MOSI	TIM1_CH2	TIM2_CH3	-	UART2_TX	ADC_ETR
PD3	I2C_SCL	UART1_RX	SPI_SCK	TIM1_CH3	TIM2_CH2	-	UART2_RX	ADC_ETR
PD4	I2C_SMBA	UART1_TX	SPI_MOSI	TIM1_CH4	TIM2_CH1	RCC_MCO	UART2_TX	ADC_ETR
PD5	SWDIO	UART1_TX	SPI_MISO	TIM1_ETR	TIM2_ETR	RCC_MCO	UART2_TX	ADC_ETR
PD6	I2C_SMBA	UART1_RX	SPI_MISO	TIM1_CH2	TIM2_CH2	RCC_MCO	UART2_RX	ADC_ETR
PD7	I2C_SMBA	UART1_RX	SPI_NSS	TIM1_CH3/TIM1_BKIN (1)	TIM2_CH1	RCC_MCO	UART2_RX	ADC_ETR

(1). Configure the IOMUX register to set the following alternate functions: PC3 as CH3 or CH1N of TIM1, PC4 as CH4 or CH2N of TIM1, PB5 as SWCLK or I2C_SDA, PD7 as CH3 or BKIN of TIM1. For more information, see the IOMUX section in the *HK32F0301MxxxxC User Manual.*

7 Packages

7.1 Package outlines

7.1.1 SOP8

SOP8 is a 4.9 mm × 3.8 mm, 1.27 mm pitch package.

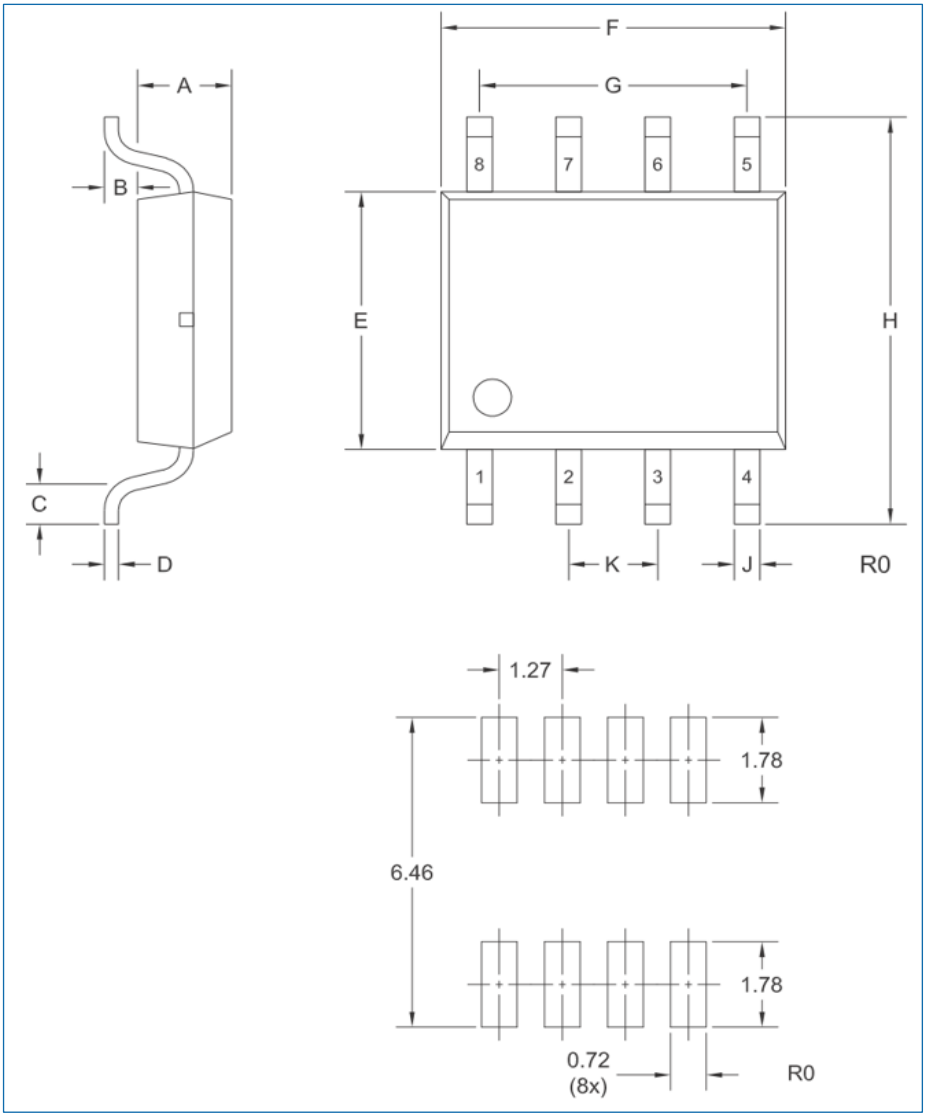

Figure 7-1 SOP8 package outline

Table 7-1 S0P8 package parameters

Symbol	Min (mm)	Max (mm)	Min (inches) (1)	Max (inches) (1)
A	1.24	1.44	0.049	0.057
B	0.00	0.27	0.000	0.011
C	0.46	-	0.018	-
D	0.16	0.27	0.006	0.011
E	3.70	3.90	0.145	0.154
F	4.81	5.01	0.189	0.198
G	3.81		0.150	
H	5.88	6.18	0.231	0.244
J	0.35	0.52	0.013	0.021
K	1.27		0.050	

7.1.2 TSSOP16

TSSOP16 is a 5.0 mm × 4.4 mm, 0.65 mm pitch package.

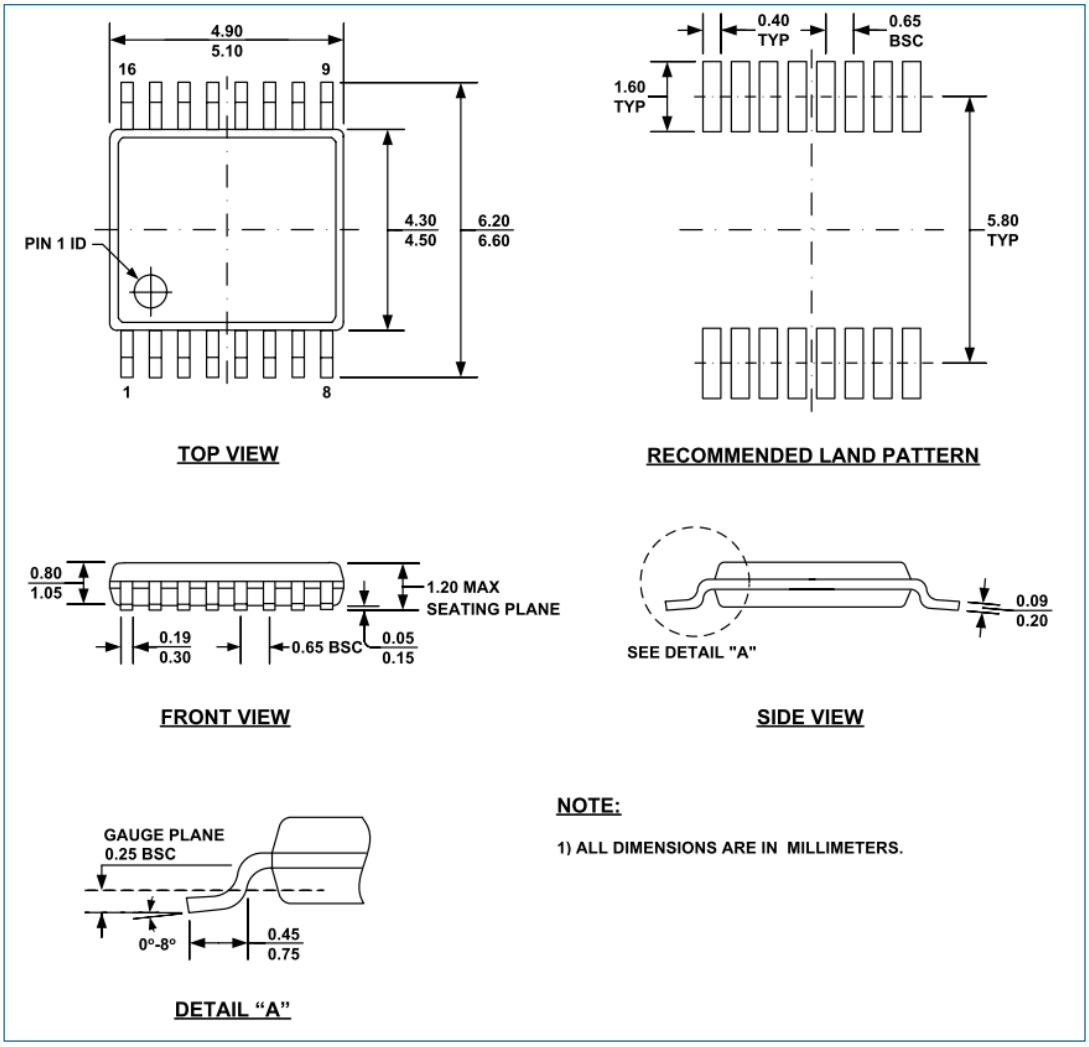

Figure 7-2 TSSOP16 package outline

Table 7-2 TSSOP16 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
b1	0.20	0.22	0.24
c	0.10	-	0.19
C1	0.10	0.13	0.15
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

7.1.3 TSSOP20

TSSOP20 is a 6.5 mm × 4.4 mm, 0.65 mm pitch package.

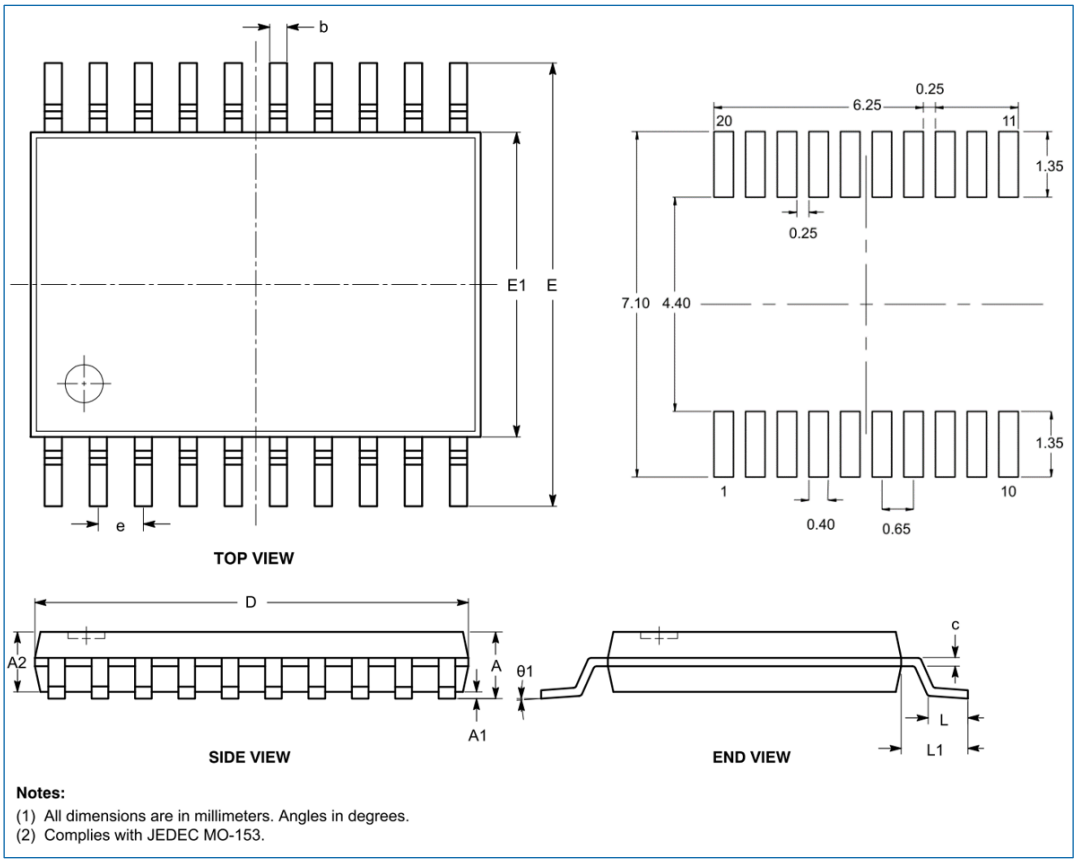

Figure 7-3 TSSOP20 package outline

Table 7-3 TSSOP20 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	-	8°

7.1.4 QFN20

The QFN20 package has two types of outlines. One is the 3 mm × 3 mm, 0.4 mm pitch package, as shown in Figure 7-4. This is the package of HK32F0301MF4N7C MCUs. Another is the 4 mm × 4 mm, 0.5 mm pitch package, as shown in Figure 7-5. This is the package of HK32F0301MF4U7C MCUs.

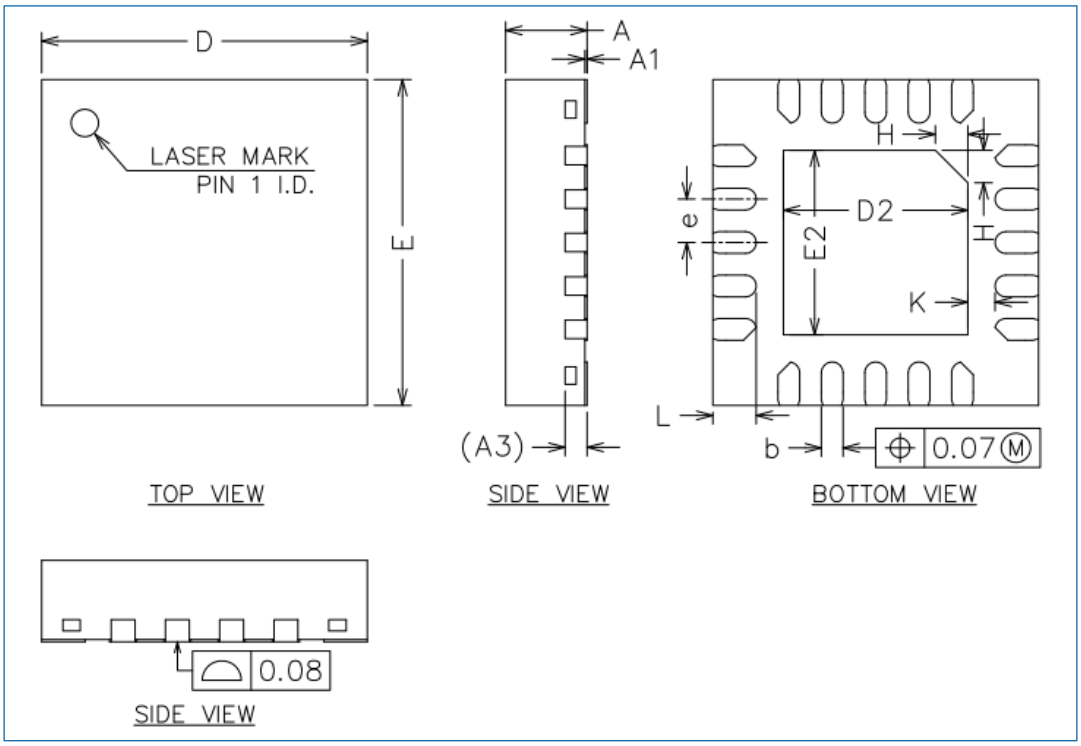

Figure 7-4 Outline of QFN20 package 1

Table 7-4 Parameters of QFN20 package 1

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75
e	0.30	0.40	0.50
H	0.30 REF		
K	0.15	-	-
L	0.35	0.40	0.45

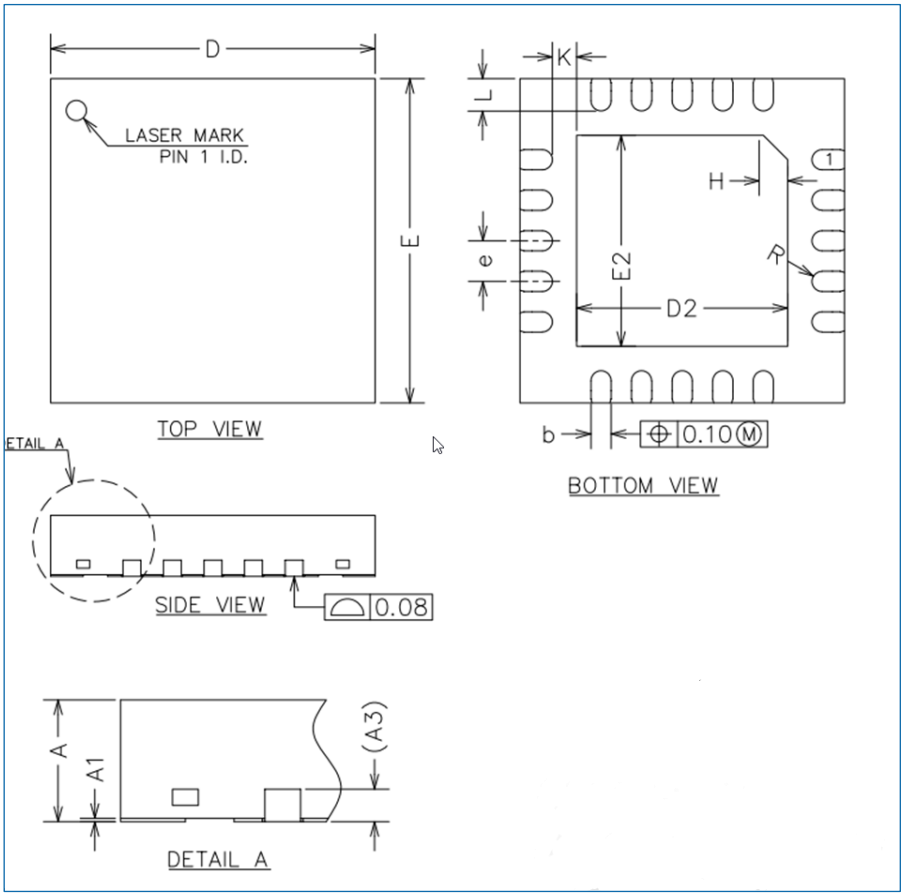

Figure 7-5 Outline of QFN20 package 2

Table 7-5 Parameters of QFN20 package 2

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
H	0.30 REF		
K	0.20	-	-
L	0.35	0.40	0.45
R	0.10	-	-

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-6 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 SOP8 marking

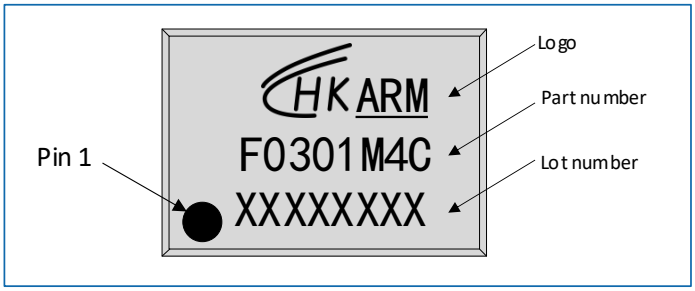

Figure 7-6 SOP8 HK32F0301MJ4M7C marking example

7.2.2 TSSOP16 marking

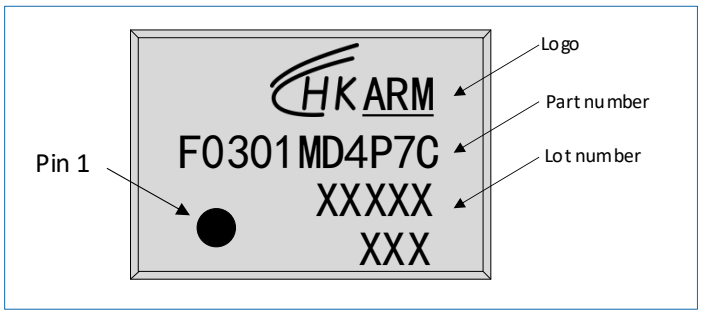

Figure 7-7 TSSOP16 HK32F0301MD4P7C marking example

7.2.3 TSSOP20 marking

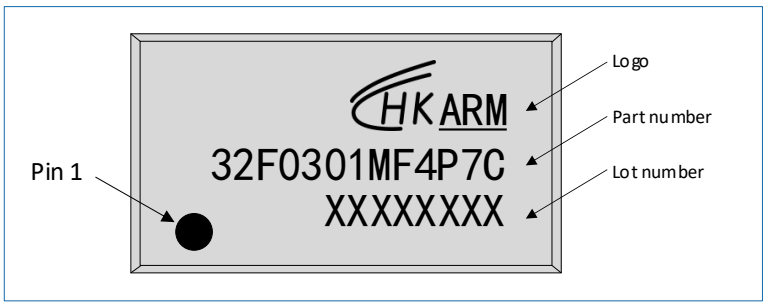

Figure 7-8 TSSOP20 HK32F0301MF4P7C marking example

7.2.4 QFN20 marking

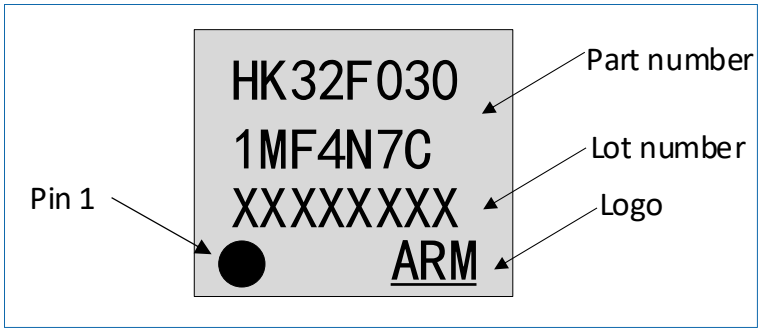

Figure 7-9 QFN20 HK32F0301MF4N7C marking example

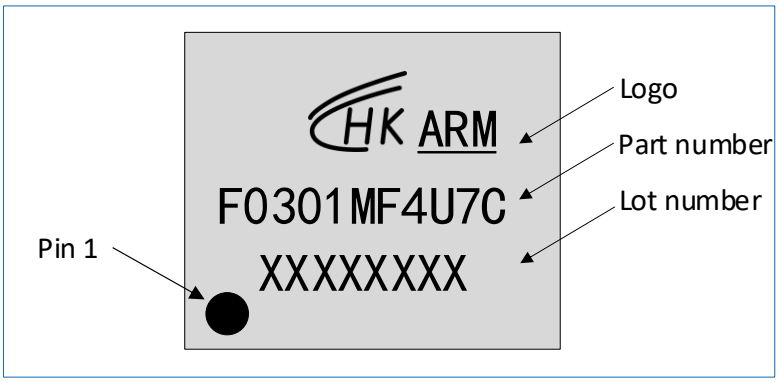

Figure 7-10 QFN20 HK32F0301MF4U7C marking example

8 Ordering information

8.1 Device numbering conventions

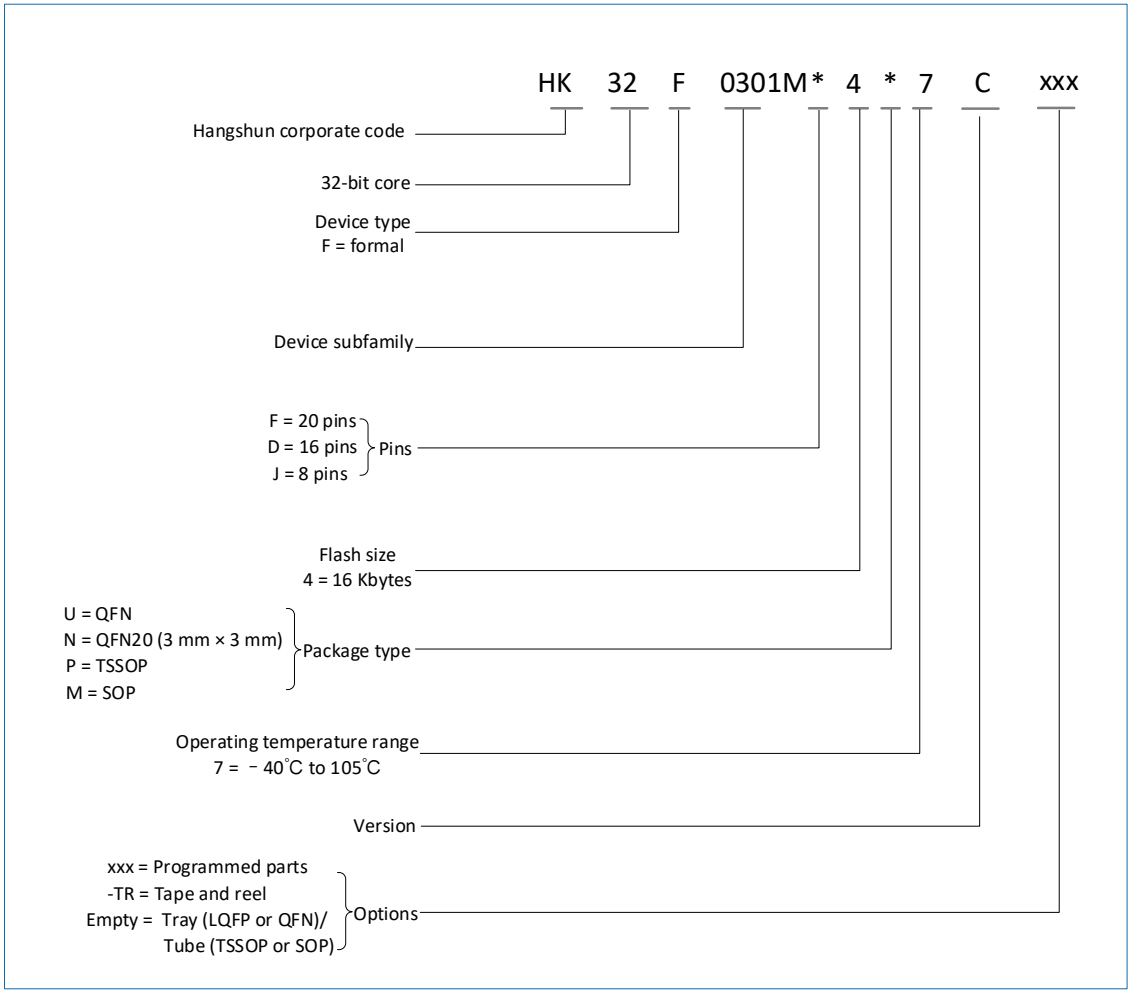

Figure 8-1 Device numbering conventions

8.2 Packaging information

Table 8-1 HK32F0301MxxxxC packaging information

Package	Part Number	Shipping Option	Remarks
SOP8	HK32F0301MJ4M7C	Tube	
SOP8	HK32F0301MJ4M7C-TR	Tape and reel	
TSSOP16	HK32F0301MD4P7C	Tube	
TSSOP16	HK32F0301MD4P7C-TR	Tape and reel	
TSSOP20	HK32F0301MF4P7C	Tube	
TSSOP20	HK32F0301MF4P7C-TR	Tape and reel	
QFN20	HK32F0301MF4N7C	Tray	The QFN20 package has two types of outlines. For details, see section "7.1.4 QFN20".
QFN20	HK32F0301MF4N7C-TR	Tape and reel	
QFN20	HK32F0301MF4U7C	Tray	
QFN20	HK32F0301MF4U7C-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CLU	Configurable Logic Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EMACC	Electric Motor Acceleration
EXTI	Extended Interrupt/Event Controller
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
UART	Universal Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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