HK32E032 Datasheet

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Shenzhen Hangshun Chip Technology R&D Co., Ltd.

http://www.hsxp-hk.com

Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32E032 series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32E032.

Audience

This document is intended for:

- HK32E032 developers
- HK32E032 testers
- HK32E032 users

Release Notes

This document is applicable to HK32E032 series MCUs.

Revision History

Version	Date	Description
1.0	2023/11/14	The initial release.

Contents

1 Introduction

This document is the datasheet for HK32E032 series MCUs. HK32E032 is a family of cost-effective MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32E032R4T5

For more details on HK32E032, see *HK32E032 User Manual*.

2 Product overview

HK32E032 adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 48 MHz. Each HK32E032 MCU has 16 Kbytes of Flash, 448 bytes of EEPROM, and four Kbytes of SRAM. You can configure the Flash controller register to remap interrupt vectors in the 16-Kbyte space.

Except for the power pins and ground pins, all the other pins of HK32E032 can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32E032 incorporates a wide selection of communication interfaces:

- 1 × high-speed USART of up to 6 Mbit/s

  The universal synchronous asynchronous receiver and transmitter (USART) supports synchronous and asynchronous full-duplex or half-duplex communication, multimaster communication, LIN protocol, Smart Card protocol, and IrDA SIR ENDEC. The RX and TX pins can be exchanged by using the software. The polarity of RX and TX pins can be configured by using the software. The USART can wake up the MCU from Stop mode when receiving data.

- 1 × high-speed SPI/I2S of up to 18 Mbit/s

  The SPI/I2S supports the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, automatic CRC, and I2S protocol.

- 1 × high-speed I2Cs of up to 1 Mbit/s

  The I2C supports 1 Mbit/s, 400 kbit/s, and 100 kbit/s transmission rates, master/slave mode, multimaster mode, 7-bit/10-bit addressing, and SMBus protocol. The I2C can wake up the MCU from Stop mode when receiving data.

HK32E032 embeds a 16-bit advanced PWM timer (four PWM outputs in total, three of which have programmable inserted dead-times), a 16-bit general-purpose PWM timer (four PWM outputs in total), and a 16-bit basic timer (for periodic outputs of CPU interrupts).

HK32E032 also incorporates the analog circuitry: a 12-bit 1 MSPS ADC, a power-on reset (POR)/power-down reset (PDR) circuitry, and an internal reference voltage (sampled by on-chip ADC).

HK32E032 supports multiple power consumption modes. In low-power modes, the typical leakage current of HK32E032 MCUs is lower than 50 nA, and HK32E032 MCUs can be automatically woken up by the internal low-power timer.

HK32E032 embeds an LCD that can drive up to 4 × 32 pixels.

HK32E032 MCUs operate in the –25°C to +75°C temperature range, from a 2.4 V to 3.6 V power supply. It meets the environmental requirements of most applications.

With its diversified peripheral interfaces, HK32E032 is suitable for a wide range of applications:

- Programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- CPU core

- ARM® Cortex®-M0
- Maximum frequency: 48 MHz
- 24-bit SysTick timer
- Supports the remapping of interrupt vectors (by configuring the Flash controller register)

- Operating voltage range: 2.4 V to 3.6 V
- Operating temperature range: –25°C to +75°C
- Typical operating current
  - Run mode: 3.02 mA@48 MHz@3.3 V (63 µA/MHz)
  - Sleep mode: 1.486 mA@48 MHz@3.3 V (31 µA/MHz), wakeup time 21 ns
  - Deep Sleep mode: 0.646 mA@114 kHz@3.3 V, wakeup time 7.8 µs
  - Stop mode: 30.12 µA@3.3 V, wakeup time 10 µs (can be woken up by external pins or the internal timer)
  - Standby mode: 20 nA@3.3 V, wakeup time 457 µs (can be woken up by external pins or the internal timer)
- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Memory
  - 16-Kbyte Flash (128 pages, 128 bytes per page; 32-bit reading, 16-bit writing)
  - Separate read and write protection for Flash data
  - 448-byte EEPROM
  - 4-Kbyte SRAM
- Data security
  - Cyclic redundancy check (CRC) hardware implementation unit
- Clock
  - GPIO external input clock: up to 48 MHz
  - High-speed internal clock (HSI): 48 MHz
  - Low-speed internal clock (LSI): 114 kHz
- Reset
  - External pin reset
  - POR/PDR
  - Software reset
  - IWDG reset and WWDG reset
  - Low-power management reset
- GPIO
  - 12 GPIOs
  - Each can be used for external interrupt inputs
  - Built-in pull-up/pull-down resistors that can be turned on or off
  - Support open-drain output

- Configurable output drive capacity: high/low

- Pin multiplexing controller IOMUX
  - The mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX.
- Data communication interfaces
  - 1 × high-speed USART of up to 6 Mbit/s (can wake up the MCU from Stop mode when receiving data)
  - 1 × high-speed I2C of up to 1 Mbit/s (can wake up the MCU from Stop mode when receiving data)
  - 1 × high-speed SPI of up to 18 Mbit/s (supports the I2S protocol)
- Timer and PWM generator
  - 1 × 16-bit advanced PWM timer (four PWM outputs in total, three of which are complementary outputs with programmable inserted dead-times)
  - 1 × 16-bit general-purpose PWM timer (four PWM outputs in total)
  - 1 × 16-bit basic timer (supports CPU interrupts)
  - 2 × auto-wakeup timers:
    - The AWU timer can work in Stop mode.
    - The STBAWU timer can work in Standby mode.
- Beeper
  - 1 × beeper, which can output 1 kHz, 2 kHz, 4 kHz, or 8 kHz pulses
  - In Stop mode, the beeper keeps operating and can trigger ADC sampling periodically.
- On-chip analog circuitry
  - 1 × 12-bit 1 MSPS ADC (five external analog input channels in total, support the differential pair input)
  - 1 × POR/PDR circuitry
  - 1 × 0.8 V internal reference voltage (sampled by ADC on chip)
- UID
  - Each HK32E032 MCU provides a 64-bit unique ID (UID).
- LCD
  - A 32 × 4-bit LCD SRAM is embedded.
  - 1/2 or 1/3 bias selectable, 1/2, 1/3, or 1/4 duty cycle selectable
- Reliability
  - Passes HBM6000V/CDM500V/LU700mA level tests.

2.2 Device overview

Table 2-1 HK32E032 series features

Feature	HK32E032R4T5
Operating voltage	2.4 V to 3.6 V
Operating temperature	–25°C to +75°C
CPU frequency	48 MHz
SysTick	1
Flash	16 Kbytes
EEPROM	448 bytes
SRAM	4 Kbytes
CRC	1
IWDG	1
WWDG	1
USART	1
I2C	1
SPI/I2S	1/1

Feature	HK32E032R4T5
Advanced timer	1
General-purpose timer	1
Basic timer	1
LCD	1
AWU timer	1
STBAWU timer	1
Beeper	1
ADC (External channels)	1 (5)
POR/PDR	1
Internal reference voltage	1
64-bit UID	1
GPIO	12
Package	LQFP64

3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor that provides an MCU platform featuring low cost and low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With the ARM Cortex®-M0 core embedded, the HK32E032 family is compatible with ARM tools and software.

The following figure shows the block diagram of HK32E032:

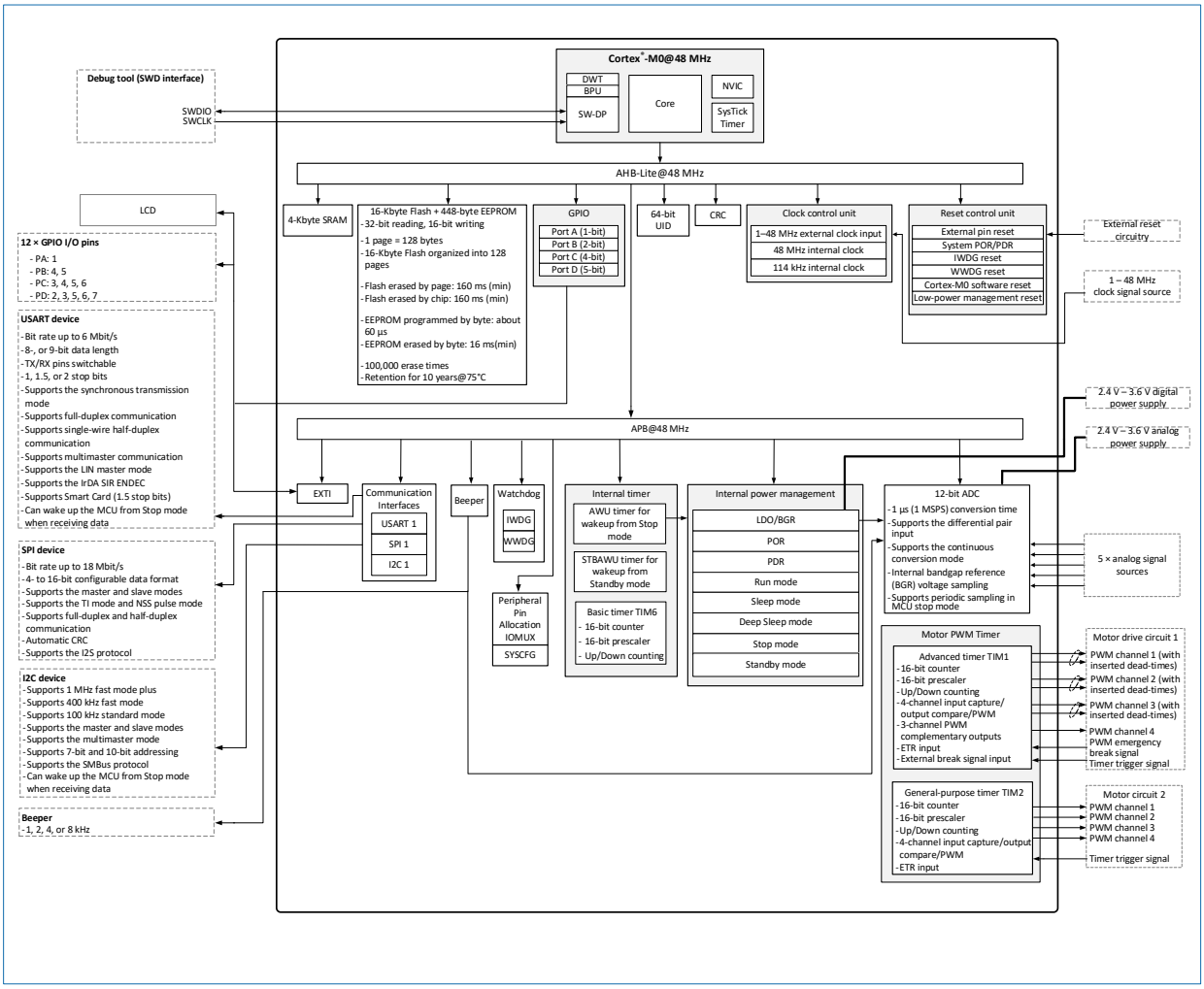

Figure 3-1 HK32E032R4T5 block diagram

3.2 Memory mapping

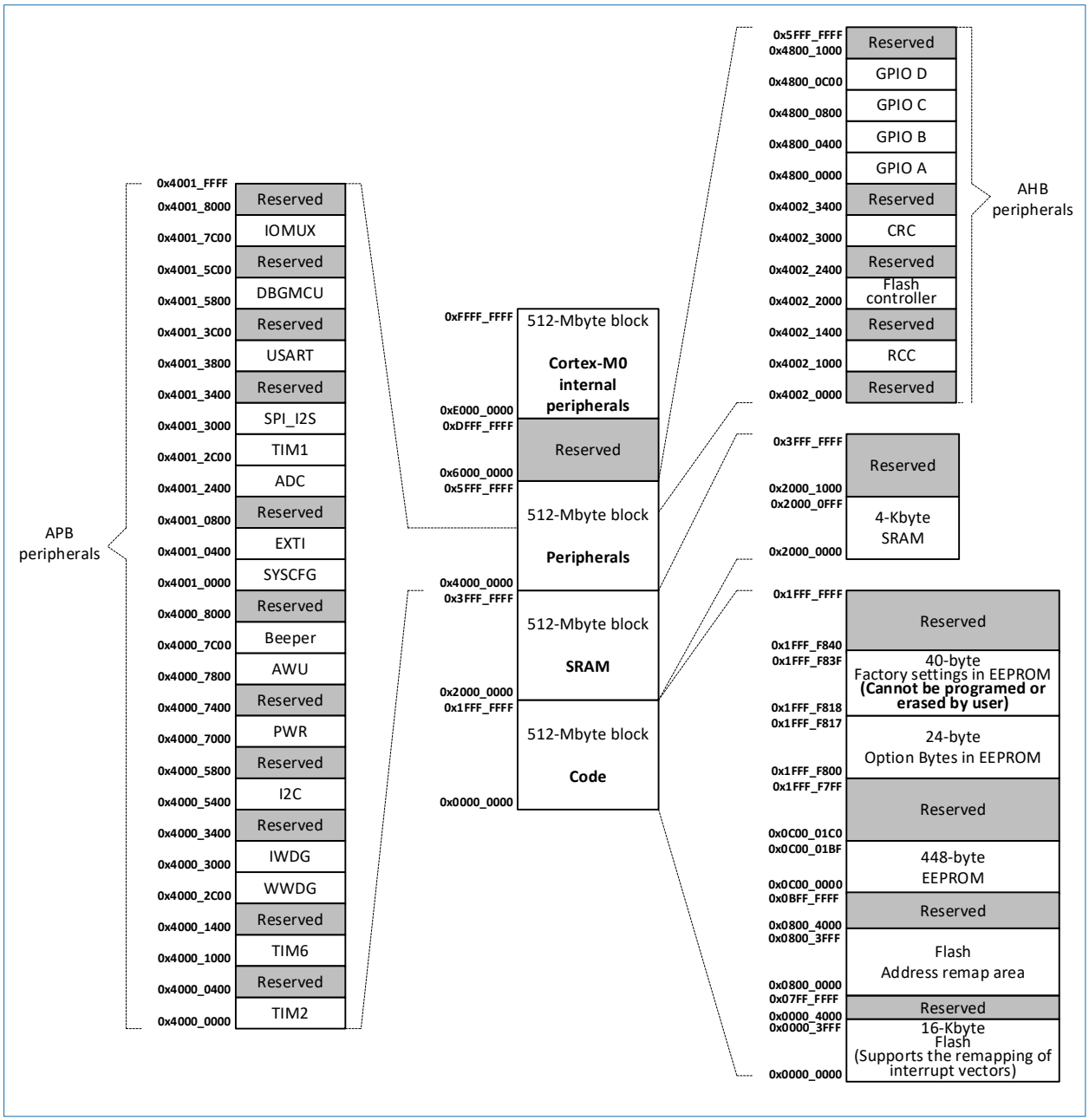

Figure 3-2 HK32E032R4T5 memory mapping

3.2.1 Flash features

- Flash data width: 32-bit reading, 16-bit writing.
- Page size: 128 bytes.
- Access to Flash: half-word (16 bits) writing, 32-bit reading
- Supports Flash read/write protection.
- The interrupt vectors can be remapped by configuring the register.

Table 3-1 Flash features

	Read Operation	Erase/Programming Operation
Operation time	• When VCC = 2.4 V: ○ 000: zero wait states (when HCLK ≤ 16 MHz) ○ 001: one wait state (when 16 MHz < HCLK ≤ 32 MHz) ○ 010: two wait states (when 32 MHz< HCLK ≤ 48 MHz) • When 2.4 V < VCC ≤ 3.6 V: ○ 000: zero wait states (when HCLK ≤ 24 MHz) ○ 001: one wait state (when 24 MHz < HCLK ≤ 48 MHz)	• Half-word programming: about 60 μs • Page erase: about 160 ms (t_{erase} = 1/$f_{FLITFCLK}$ × 320000) • Mass erase: about 160 ms (t_{erase} = 1/$f_{FLITFCLK}$ × 320000)
Endurance	Supports about 100,000 cycles of erase, read, and write operations.	

3.2.2 Flash option word

Table 3-2 Flash option word structure

Address	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFF F800	nUSER	USER	nRDP	RDP
0x1FFF F804	nDATA1	DATA1	nDATA0	DATA0
0x1FFF F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF F80C	nWRP3	WRP3	nWRP2	WRP2
0x1FFF F810	IWDG_INI_KEY[15:0]		Reserved	IWDG_RL_IV[11:0]
0x1FFF F814	DBG_CLK_CTL[15:0]		LSI_LP_CTL[15:0]	

- IWDG_RL_IV[11:0]: stores the initial values of the IWDG_RLR register. If IWDG acts as a hardware watchdog, configure the IWDG_RL_IV register to set the interval of the IWDG reset time.
- IWDG_INI_KEY[15:0]: determines whether IWDG_RL_IV is effective. When the value of IWDG_INI_KEY equals 0x5B1E, IWDG_RL_IV is effective.
- LSI_LP_CTL[15:0]: enters the Stop mode after IWDG is enabled and sets whether the system needs to be periodically woken up by IWDG.
  - If LSI_LP_CTL is set to 0x369C, when the MCU enters the Stop or Standby mode, LSI can be turned off according to the LSION value. When the MCU is woken up, LSI returns to the status before entering the Stop or Standby mode.
  - If LSI_LP_CTL is not set, after IWDG is enabled and the MCU enters the Stop or Standby mode, the system can be periodically woken up by IWDG.
- DBG_CLK_CTL[15:0]: When DBG_CLK_CTL stores 0x12DE, the CPU debug clock is turned off. Otherwise, it is turned on.

Note:

For the definitions of bit fields corresponding to 0x1FFF_F800 – 0x1FFF_F80C in Table 3-2, see section "Flash option word register" in *HK32E032 User Manual*.

3.2.3 SRAM

HK32E032 integrates a 4-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.2.4 EEPROM

HK32E032 integrates a 448-byte EEPROM.

Table 3-3 EEPROM features

	Read Operation	Erase/Programming Operation
Operation time	• When VCC = 2.4 V: ○ 000: zero wait states (when HCLK ≤ 16 MHz) ○ 001: one wait state (when 16 MHz < HCLK ≤ 32 MHz) ○ 010: two wait states (when 32 MHz< HCLK ≤ 48 MHz) • When 2.4 V < VCC ≤ 3.6 V: ○ 000: zero wait states (when HCLK ≤ 24 MHz) ○ 001: one wait state (when 24 MHz < HCLK ≤ 48 MHz)	• Byte programming: about 60 μs (t_{erase_byte} = 1/$f_{FLITFCLK}$ × 120) • Byte erase: about 16 ms (t_{erase_byte} = 1/$f_{FLITFCLK}$ × 32000)
Endurance	Supports about 100,000 cycles of erase, read, and write operations, or a service life of 10 years. (The shorter one prevails.)	

3.3 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32E032 integrates a CRC calculation unit to reduce the application processing burden and accelerate processing.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with the reference signature that is generated at link time and stored at a specified memory location.

3.4 NVIC

HK32E032 embeds a nested vectored interrupt controller (NVIC) to manage interrupts flexibly with the lowest interrupt latency. An HK32E032 MCU has 21 external interrupts.

- The NVIC closely coupled with the core interface ensures low latencies in interrupt processing.
- The interrupt vector entry address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- Saves the processor state automatically.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

Table 3-4 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	–3	Fixed	Reset	Reset	0x0000 0004
-	–2	Fixed	NMI	Non-maskable interrupt.	0x0000 0008
-	–1	Fixed	HardFault	All classes of faults	0x0000 000C
-	3	Configurable	SVCall	System service call via SWI instruction	0x0000 002C
-	5	Configurable	PendSV	Pendable request for system service	0x0000 0038
-	6	Configurable	SysTick timer	SysTick timer	0x0000 003C
0	7	Configurable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Configurable	-	-	0x0000 0044
2	9	Configurable	EXTI11	Automatic wakeup interrupt of EXTI line 11 (AWU_WKP)	0x0000 0048
3	10	Configurable	Flash	Flash global interrupt	0x0000 004C
4	11	Configurable	RCC	RCC global interrupt	0x0000 0050
5	12	Configurable	EXTI0	EXTI line 0 interrupt	0x0000 0054
6	13	Configurable	EXTI1	EXTI line 1 interrupt	0x0000 0058

Position	Priority		Name	Description	Address
7	14	Configurable	EXTI2	EXTI line 2 interrupt	0x0000 005C
8	15	Configurable	EXTI3	EXTI line 3 interrupt	0x0000 0060
9	16	Configurable	EXTI4	EXTI line 4 interrupt	0x0000 0064
10	17	Configurable	EXTI5	EXTI line 5 interrupt	0x0000 0068
11	18	Configurable	TIM1_BRK	TIM1 break interrupt	0x0000 006C
12	19	Configurable	ADC	ADC interrupt (combined with EXTI line 8)	0x0000 0070
13	20	Configurable	TIM1_UP_TRG_COM	TIM1 update, trigger, and COM interrupt	0x0000 0074
14	21	Configurable	TIM1_CC	TIM1 capture/compare interrupt	0x0000 0078
15	22	Configurable	TIM2	TIM2 global interrupt	0x0000 007C
16	23	Configurable	-	-	0x0000 0080
17	24	Configurable	TIM6	TIM6 global interrupt	0x0000 0084
18	25	Configurable	-	-	0x0000 0088
19	26	Configurable	-	-	0x0000 008C
20	27	Configurable	-	-	0x0000 0090
21	28	Configurable	EXTI6	EXTI line 6 interrupt	0x0000 0094
22	29	Configurable	EXTI7	EXTI line 7 interrupt	0x0000 0098
23	30	Configurable	I2C	I2C global interrupt (combined with EXTI line 10)	0x0000 009C
24	31	Configurable	-	-	0x0000 00A0
25	32	Configurable	SPI	SPI global interrupt	0x0000 00A4
26	33	Configurable	-	-	0x0000 00A8
27	34	Configurable	USART	USART global interrupt (combined with EXTI line 9)	0x0000 00AC
28	35	Configurable	-	-	0x0000 00B0
29	36	Configurable	-	-	0x0000 00B4
30	37	Configurable	-	-	0x0000 00B8
31	38	Configurable	-	-	0x0000 00BC

3.5 EXTI

HK32E032 has 12 EXTI lines (EXTI lines 0 to 11). The EXTI lines from EXTI 0 to EXTI 7 are connected to I/O pins. The connections of the other EXTI lines are as follows:

- EXTI 8 connected to the ADC AWD event
- EXTI 9 connected to the USART wakeup event
- EXTI 10 connected to the I2C wakeup event
- EXTI 11 connected to the AWU wakeup event

EXTI lines from 8 to 10 are connected to internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). EXTI lines from 8 to 10 can only detect the rising edge of events in Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system.

3.6 Resets

HK32E032 supports the system reset and power reset.

3.6.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the

registers in the backup domain. A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset

You can identify the reset source by checking reset status flags in the RCC_CSR register.

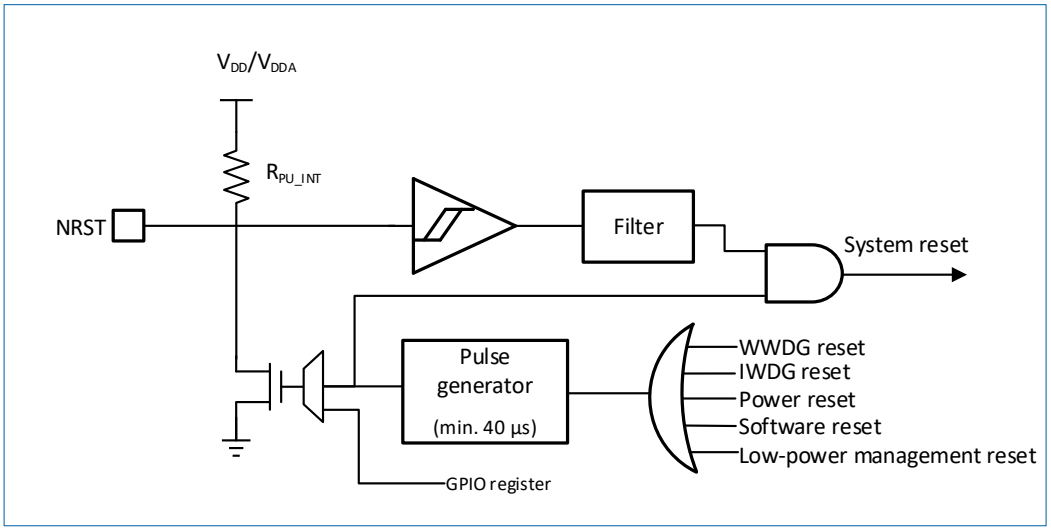

Figure 3-3 Reset circuitry

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004.

The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.6.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Exit from Standby mode

The power reset resets all registers, except for the registers in the backup domain.

HK32E032 MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

3.7 Clocks

A system clock is selected when the HK32E032 MCU starts. During the reset, the 48 MHz HSI is selected as the CPU clock by default, then the LSI can be selected.

HK32E032 also provides LSI and GPIO input as clock sources for the low-power and low-cost design scheme.

3.7.1 Clock sources

Table 3-5 Clock sources

Clock	Description
HSI clock	Frequency: 48 MHz
LSI clock	Frequency: 114 kHz
GPIO external input clock	Up to 48 MHz, input from EXTCLK1, EXTCLK2, EXTCLK3, EXTCLK4

3.7.2 Clock tree

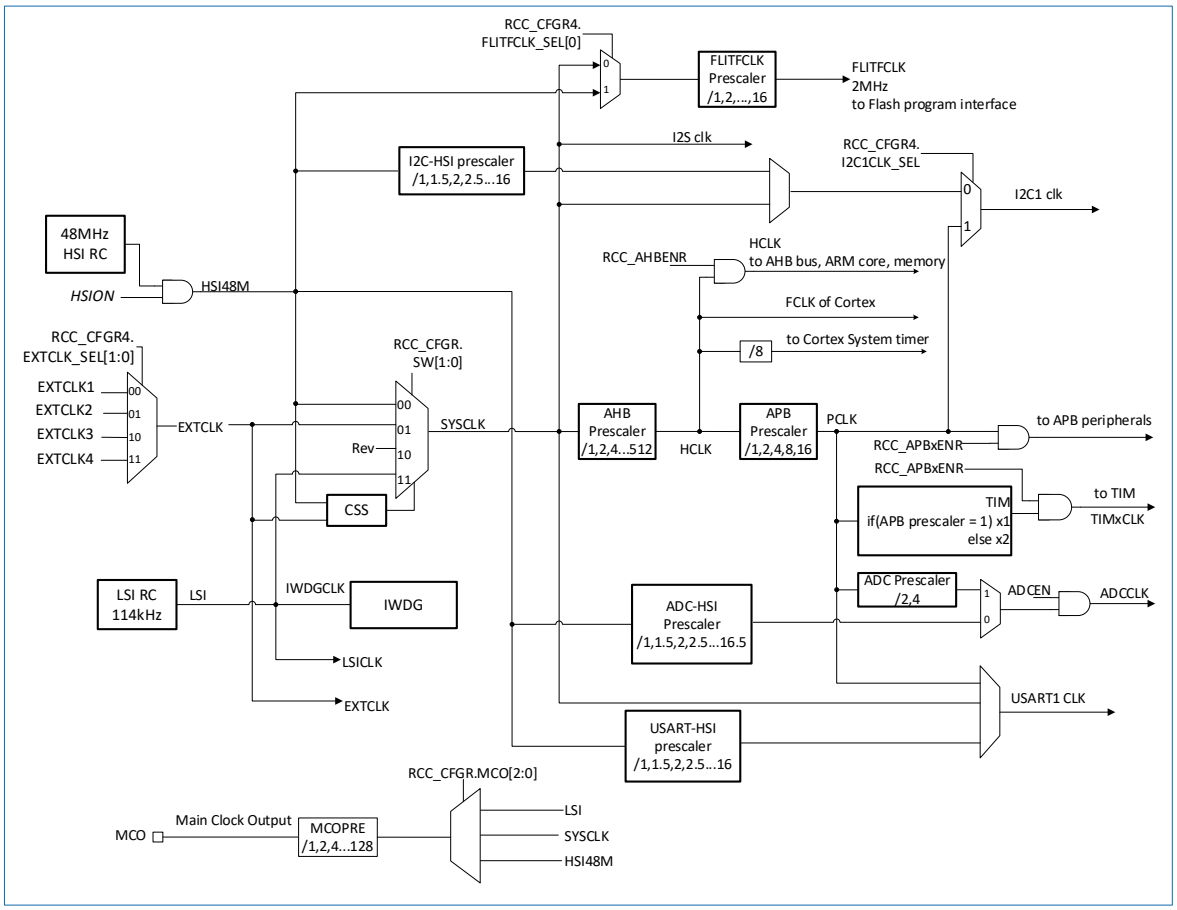

Figure 3-4 Clock tree

- SYSCLK: HSI48M, LSI, or GPIO input clock selectable. Default: HSI48M.
- HCLK: The default AHB prescaler factor is six.
- FLITFCLK: HSI48 or SYSCLK selectable.
- In clock security system (CSS) detection, the threshold for GPIO input clock frequency is adjustable.

3.8 Power supply scheme

- V_{DD} and V_{DDA} supply power to the digital circuitry and analog circuitry of the MCU via the same pin. The range of V_{DD}/V_{DDA} is from 2.4 V to 3.6 V.
- V_{CC} supplies power to the digital circuitry of the LCD module. V_{LCD} supplies power to the LCD module. When LCD is used, both V_{CC} and V_{LCD} supply power ranging from 2.4 V to 3.6 V, which is the same as the MCU operating voltage range.

3.9 Low-power modes

HK32E032 supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and available wake-up sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Deep Sleep mode

  In Deep Sleep mode, the system clock operates at 114 kHz to reduce power consumption. In Deep Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs. The power consumption of Deep Sleep mode is higher than that of Stop mode.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain and the HSI RC oscillator are disabled.

  MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any external I/O pin.

- Standby mode

  In Standby mode, MCUs achieve the lowest power consumption. The internal LDO is off, so the entire core domain is powered off. The HSI is disabled. The SRAM and register content is lost while the content in 4-byte backup registers is retained. The Standby circuitry works as normal.

  MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an STBAWU timer overflow occurs.

Table 3-6 Power consumption and wakeup time in different operating modes

Operating Mode	Power Consumption(1)	Wakeup Time
Run mode	Dynamic power consumption: 3.02 mA@48 MHz@3.3 V (63 µA/MHz)	-
Sleep mode	Dynamic power consumption: 1.486 mA@48 MHz@3.3 V (31 µA/MHz)	21 ns
Deep Sleep mode	Static power consumption: 0.646 mA@114 kHz@3.3 V	7.8 µs
Stop mode	Static power consumption: 30.12 µA@3.3 V	10 µs
Standby mode	Static power consumption: 20 nA@3.3 V	457 µs

(1). For more information about the power consumption and test conditions in different modes, see Table 4-8.

The following table describes the conditions of entering and exiting low-power modes:

Table 3-7 Conditions of entering and exiting low-power modes

Operating Mode	Entry	Exit	Core Domain Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
Sleep	1. Set PWR_CR: LPDS = 0. 2. The software executes WFI/WFE instructions.	Any interrupt request (IRQ), including SysTick.	The CPU clock is off. No impact on other clocks or the ADC clock.	On	On
Deep Sleep	1. Switch to the LSI clock. 2. Set PWR_CR: LPDS = 0. 3. The software executes WFI/WFE instructions.	Any interrupt request (IRQ), including SysTick.	The CPU clock is off. No impact on other clocks or the ADC clock.	On	On
Stop	1. Set PWR_CR: LPDS = 0. 2. Set the SLEEPDEEP bit in the Cortex-M0 system control register. 3. The software executes WFI/WFE instructions.	• Any EXTI line. ○ If the MCU enters Stop mode after the WFI instructions are executed: Set any interrupt line to the interrupt mode. (The corresponding external interrupt vector must be enabled in NVIC.) ○ If the MCU enters Stop mode after the WFE instructions are executed: Set any interrupt line to the event mode.	All clocks stop.	HSI disabled.	On or in low-power mode (configured in PWR_CR)

Operating Mode	Entry	Exit	Core Domain Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
		• Pre-wakeup by ADC sampling triggered by the beeper. The real wakeup occurs when the conditions are met. • AWU			
Standby	1. Set the SLEEPDEEP bit in the Cortex-M0 system control register. 2. Set the PDDS bit in the Power control register PWR_CR. 3. Clear the WUF bit in the Power control/status register PWR_CSR.	• External reset on the NRST pin • IWDG reset • A rising edge on the WKUP pin • STBAWU timer overflow	All clocks stop.	HSI disabled.	Off

3.10 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 114 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop and Standby modes. The IWDG can reset the system when a problem occurs or work as a free-running timer to provide timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

3.11 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.12 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.13 Basic timer

HK32E032 integrates a basic timer TIM6.

TIM6 embeds a 16-bit counter and a 16-bit prescaler. The counter can operate in up counting, down counting, or up/down counting mode. It is used to generate periodic CPU interrupt requests. In debug mode, the counter can be frozen.

3.14 General-purpose timer

HK32E032 integrates a 4-channel general-purpose timer TIM2.

TIM2 can generate PWM outputs or serve as a simple time base. TIM2 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. In debug mode, the counter can be frozen.

TIM2 can work with the advanced timer through the Timer Link feature for synchronization and event chaining. Additionally, TIM2 can process quadrature (incremental) encoder signals and the digital outputs from one to

three hall-effect sensors.

3.15 Advanced timer

HK32E032 integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of the advanced timer can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). Many functions of TIM1 are the same as those of the general-purpose timer. Therefore, the advanced timer can work together with the general-purpose timer through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

3.16 AWU timer

HK32E032 provides an auto-wakeup unit (AWU) timer. The AWU timer can count and generate an interrupt to wake up the MCU from Stop mode. It is based on an ultra-low-power 22-bit counter. The operating clock of the counter can be a 1 – 48 MHz GPIO input clock or the 114 kHz low-speed internal (LSI) clock. The AWU adopts the down-counting mode.

3.17 STBAWU timer

HK32E032 MCU integrates a standby auto-wakeup unit (STBAWU) timer. The STBAWU timer can count and generate a wakeup event to wake up the MCU from Standby mode. The STBAWU timer is based on a 26-bit counter which uses the 114 kHz LSI as the operating clock. The wakeup interval can be set to a value from 8 ms to 524.28s.

3.18 Beeper

An ultra-low-power 7-bit timer is embedded in the beeper. The operating clock of the timer can be the 1 – 48 MHz GPIO external input clock or the 114 kHz low-speed internal (LSI) clock. The timer adopts the down-counting mode and can output 1 kHz, 2 kHz, 4 kHz, or 8 kHz pulses.

In Stop mode, the beeper keeps operating and can trigger ADC sampling periodically. The frequency at which ADC sampling is triggered is 1/1024 of the frequency of the pulse output by the beeper. For example, if the beeper outputs 1 kHz pulses, ADC sampling is triggered at a frequency of 1 kHz/1024 ≈ 0.98 Hz (at an interval of about 1.02s).

3.19 I2C bus

HK32E032 provides an I2C bus interface that can work as a master or slave and supports the standard mode, fast mode, and fast mode plus. The I2C bus interface supports the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interface embeds hardware CRC generation/verification and supports SMBus V2.0/PMBus.

3.20 USART

A universal synchronous/asynchronous receiver/transmitter (USART) is embedded in each HK32E032 MCU. It can communicate at a speed of up to 6 Mbit/s.

The USART supports the multiprocessor communication mode, host synchronous communication mode, and single-wire half-duplex communication mode. The USART also supports Smart Card communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability, and automatic baud rate detection.

The USART has a clock independent of the CPU clock domain, so it can wake up the MCU from Stop mode.

Table 3-8 USART features

USART Mode/Feature	USART1
DMA transmission	No supported
Multiprocessor communication	Supported
Synchronous mode	Supported
Single-wire half-duplex communication	Supported
Dual clock domains and wakeup from Stop mode	Supported
Automatic baud rate detection	Supported
Modbus communication	Supported
RS232 hardware flow control	No supported
RS485 driver enable	No supported
IrDA SIR ENDEC	Supported
LIN mode	Supported
Smart Card mode	Supported

3.21 SPI

HK32E032 has an SPI interface operating at up to 18 Mbit/s. The SPI interface supports full-duplex or half-duplex communication in master and slave modes. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4- to 16-bit.

The standard I2S interface (with SPI multiplexed) provides four types of audio standards and supports half-duplex communication in master or slave mode. The I2S interface has dedicated signals for data synchronization. The data format can be 16-bit, 24-bit, or 32-bit and the I2S interface can operate with 16- or 32-bit resolution. The I2S interface can be set to an audio sampling frequency from 8 kHz to 192 kHz by the 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components.

Table 3-9 SPI features

SPI Feature	SPI1
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
I2S mode	Supported
TI mode	Supported

3.22 GPIO

Each general-purpose input/output (GPIO) pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.23 LCD

HK32E032 embeds the multi-functional liquid crystal display (LCD) driver and 128-bit LCD SRAM. The bias can be set to 1/2 or 1/3, and the duty cycle can be set to 1/2, 1/3, or 1/4.

3.24 ADC

HK32E032 incorporates an ADC that has the following features:

The ADC has a total of six internal and external channels. AIN0 to AIN4 are external channels connected to I/Os. AIN5 is an internal channel connected to the internal reference voltage.

- Supports the differential pair input mode. AIN0-AIN1 and AIN2-AIN3 form two differential pairs. (When ADC is configured to the differential pair input mode, AIN4 and the ADC channel for the sampling of the internal BGR voltage are unavailable.)
- Supports only the 12-bit ADC sampling resolution (eight bits valid).

3.24.1 ADC external trigger sources

Table 3-10 ADC external trigger sources

Name	Source	External Trigger Selection Mode (EXTSEL[2:0])
TRG0	TIM1_TRGO	000
TRG1	TIM1_CC4	001
TRG2	TIM2_TRGO	010
TRG3	TIM6_TRGO	011
TRG4	TIM1_CC1	100
TRG5	TIM1_CC2	101
TRG6	TIM1_CC3	110
TRG7	IO_TRIG	111

IO_TRIG can be triggered by any I/O. You need to set the MODER and AFR registers of the corresponding I/O. For details, see section "GPIO registers" in *HK32E032 User Manual*.

3.24.2 AWD wakeup function

In Stop mode, the beeper counts and sends a signal to the ADC. The ADC samples the signal and wakes up the ADC clock. Then the ADC clock triggers ADC conversions and generates an AWD event according to ADC conversion results. Then the AWD event is sent to an EXTI line to wake up the system.

To use the AWD wakeup function, you need to configure not only the related threshold and channel, but also the ADC_CR2.WAKE_EN register, beeper internal counting control register, and ADC wakeup enable register.

3.25 64-bit UID

The 64-bit unique identifier (UID) provides a reference number for each HK32E032 MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 64-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) as needed. The 64-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process that has a security mechanism.

3.26 Debug port

Based on the ARM SWJ-DP embedded in HK32E032, SWDIO and SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	4.0	V
$V_{CC} – V_{SS}$	LCD main supply voltage	2.4	5.2	
V_{IN}	Input voltage on pins	$V_{SS} – 0.3$	$V_{DD} + 4.0$	
$\lvert \Delta V_{DDx} \rvert$	Variation between different power pins	-	50	mV
$\lvert V_{SSx} – V_{SS} \rvert$	Variation between different ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	
I_{VCC1}	LCD operating current (uses the LCD RC oscillator)	300	μA
I_{VCC2}	LCD operating current (uses the external oscillator)	120	
I_{VCC3}	LCD operating current (uses the external clock source)	200	
I_{STB}	LCD module standby current	5	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to +125	°C
T_J	Maximum junction temperature	100	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	48	MHz
f_{PCLK}	Internal APB clock frequency	0	48	
V_{DD}/V_{DDA}	Operating voltage(1)	2.4	3.6	V
T	Operating temperature	–25	75	°C

(1). V_{DD} and V_{DDA} are combined on the chip and supplied by a single external power supply. It is recommended that you add the filter capacitor.

4.2.2 POR characteristics

Table 4-5 POR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{delay}	NRST signal establishment time	-	-	40	-	μs

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge(2)	-	2.40	-	V
		Rising edge	-	2.40	-	V

(1). PDR is based on the monitoring of V_{DD} and V_{DDA}. POR is based on the monitoring of only V_{DD}.

(2). The actual performance value is guaranteed to be smaller than the minimum $V_{POR/PDR}$ value.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–25°C to 75°C	-	0.8	-	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition	V_{DD} = 3.3 V			Unit
		–25°C	25°C	75°C	
Run mode	SYSCLK = HSI (48 MHz); All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **enabled**; Two wait states to access Flash.	3.132	3.025	3.079	mA
	SYSCLK = HSI (48 MHz); All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled**; Two wait states to access Flash.	3.122	3.020	3.074	mA
	SYSCLK = LSI (114 kHz); All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; APB clock **disabled**; Zero wait states to access Flash.	1.802	1.711	1.822	mA
Sleep mode	SYSCLK = 48 MHz; AHB/APB disabled; Clock in the core domain disabled; All I/Os configured in high impedance;	1.383	1.486	1.694	mA

Mode	Condition	V_{DD} = 3.3 V			Unit
		–25°C	25°C	75°C	
	SRAM and Flash data retained, other peripherals disabled.				
Deep Sleep mode	SYSCLK = 114 kHz; AHB/APB disabled; Clocks in the core domain disabled; All I/Os configured in high impedance; SRAM and Flash data retained, other peripherals disabled.	0.554	0.646	0.798	mA
Stop mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO operating in low-power mode; All I/Os configured in high impedance; AWU **enabled**, other peripherals disabled.	21.83	34.08	213.6	µA
	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO operating in low-power mode; All I/Os configured in high impedance; AWU **disabled**, all the other peripherals disabled.	18.02	30.12	210.44	µA
Standby mode	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO power supply disabled; STBAWU timer **enabled**; PDR of Standby circuitry **enabled**; All I/Os configured in high impedance; Power supply to backup registers and Standby circuitry kept, all the other peripherals disabled, SRAM and register content lost.	5.61	5.89	6.27	µA
	All clocks in the core domain stopped, HSI oscillator and LSI oscillator disabled; LDO power supply disabled; STBAWU timer **disabled**; PDR of Standby circuitry **enabled**; All I/Os configured in high impedance; Power supply to backup registers and Standby circuitry kept, all the other peripherals disabled, SRAM and register content lost.	1.66	2.06	2.56	µA
	All clocks in the core domain stopped; HSI oscillator and LSI oscillator disabled; LDO power supply disabled; STBAWU timer **enabled**; PDR of Standby circuitry **disabled**; All I/Os configured in high impedance; Power supply to backup registers and Standby circuitry kept, all the other peripherals disabled, SRAM and register content lost.	0.01	0.02	0.25	µA
	All system clocks stopped; HSI oscillator and LSI oscillator disabled; LDO power supply disabled; STBAWU timer **disabled**; PDR of Standby circuitry **disabled**; All I/Os configured in high impedance; Power supply to backup registers and Standby circuitry kept, all the other peripherals disabled, SRAM and register content lost.	3.98	3.93	3.87	µA

4.2.6 HSI clock characteristics

Table 4-9 Characteristics of the HSI clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
DuCy(HSI)	Duty cycle	-	45	-	55	%
ACC	Oscillator	RCC_CR register calibration	-	-	1	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	accuracy	completed by the user				
		Factory calibration: T_A = –25°C to +75°C	–1	-	1	%
T_{su} (HSI)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	1	-	2	µs
I_{DD} (HSI)	Oscillator power consumption	-	-	80	100	µA

4.2.7 LSI clock characteristics

Table 4-10 Characteristics of the LSI clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	114	-	kHz
$DuCy_{(LSI)}$	Duty cycle	-	45	-	55	%
ACC	Oscillator accuracy	Default factory value: T_A = –25°C to +75°C	1.5	-	2.2	
$T_{su\ (LSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	1	-	2	µs
$I_{DD(LSI)}$	Oscillator power consumption	-	-	5	8	µA

4.2.8 GPIO input clock

An external clock can be input to HK32E032 from EXTCLK1, EXTCLK2, EXTCLK3, or EXTCLK4.

Table 4-11 GPIO input clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Fext	Input clock frequency	1	8.0	48	MHz
	Input clock duty cycle	40	-	60	%
Jitter	Cycle-to-cycle jitter	-	-	300	ps

4.2.9 Flash memory characteristics

Table 4-12 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	Half word programming time	-	60	-	µs
T_{ERASE}	Page erase time	120	160	200	ms
	Mass erase time	120	160	200	ms
I_{DDPROG}	Half word programming current	-	-	5	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	2	mA
I_{DDREAD}	Read current@24 MHz	-	2	3	mA
	Read current@1 MHz	-	0.25	0.4	mA
N_{END}	Erasure endurance	100	-	-	Thousand cycles
t_{RET}	Data retention	10	-	-	Years

4.2.10 I/O pin input characteristics

Table 4-13 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	1.65@without Schmitt trigger 1.75@with Schmitt trigger	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	–0.3	-	1.60@with Schmitt trigger 1.45@without Schmitt trigger	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	450	-	-	mV
I_{lkg}	Input leakage current	V_{IN} = 3.3 V	-	-	3	µA
R_{PU}	Pull-up resistor	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Pull-down	$V_{IN} = V_{DD}$	30	40	50	kΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	resistor					
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.11 I/O pin output characteristics

Table 4-14 I/O pin output voltage characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}	Output low level voltage	V_{DD} = 3.3 V I_{OL} = –8 mA	0	0.8	V
V_{OH}	Output high level voltage	V_{DD} = 3.3 V I_{OH} = 8 mA	2.4	3.3	
V_{OL}	Output low level voltage	V_{DD} = 3.3 V I_{OL} = –20 mA	0	0.8	
V_{OH}	Output high level voltage	V_{DD} = 3.3 V I_{OH} = 20 mA	2.4	3.3	

Table 4-15 I/O pin output alternating current characteristics

Mode (MODER bit)	Symbol	Parameter	Condition	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	C_L = 50 pF, V_{DD} = 2.4 V – 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	C_L = 50 pF, V_{DD} = 2.4 V – 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	C_L = 50 pF, V_{DD} = 2.7 V – 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2.7 V – 3.6 V	-	5	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 2.7 V – 3.6 V	-	5	ns

4.2.12 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuits.

Table 4-16 NRST pin input characteristics

Symbol	Parameter	Min	Max	Unit
V_{IL}	NRST reset low level voltage		0.8	V
V_{IH}	NRST input high level voltage	2	-	V
V_{hys}	Schmitt trigger voltage	-	200	mV
R_{pull}	Internal weak pull-up resistor	-	50	kΩ
T_{Noise}	Low level ignored duration	-	100	ns

4.2.13 TIM characteristics

Table 4-17 TIM1 characteristics

Symbol	Parameter	Min	Max	Unit
$T_{res(TIM)}$	Timer resolution time	1	-	$T_{TIMxCLK}$
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2^{(1)}$	MHz
RES_{TIM}	Timer resolution	-	16	Bit

Symbol	Parameter	Min	Max	Unit
$T_{counter}$	16-bit counter clock period when an internal clock is selected	1	65536	$T_{TIMxCLK}$
T_{MAX_COUNT}	Maximum possible count	-	65536 × 65536	$T_{TIMxCLK}$

(1). $f_{TIMxCLK}$ = 48 MHz

Table 4-18 TIM2 characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	External input clock frequency on CH1 – CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit counter clock period when an internal clock is selected	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	ms

4.2.14 ADC characteristics

Table 4-19 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	ADC power supply	-	2	3.3	3.6	V
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 12 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DD}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sample switch resistance	-	-	-	1	kΩ
C_{ADC}	Sample and hold capacitance	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 12 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.143	µs
		-	-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 12 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1	-	18	µs
		-	14 to 252 (sampling time ts + 12.5 for successive approximation)			$1/f_{ADC}$
ADC bit width	12-bit (8 bits valid)	-	-			-

5 Typical circuitry

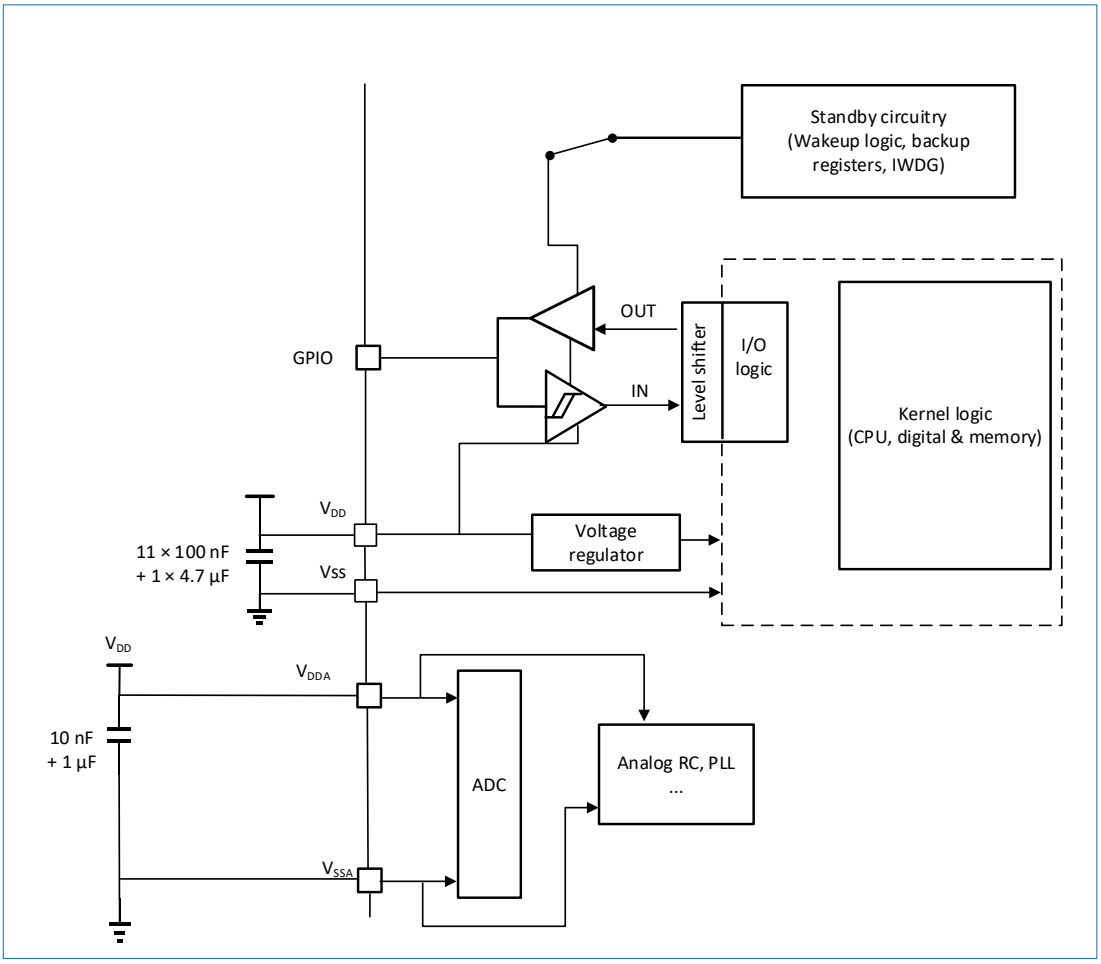

Figure 5-1 Power supply reference circuitry

6 Pinouts and pin descriptions

HK32E032 MCUs are delivered in the LQFP64 package.

6.1 LQFP64

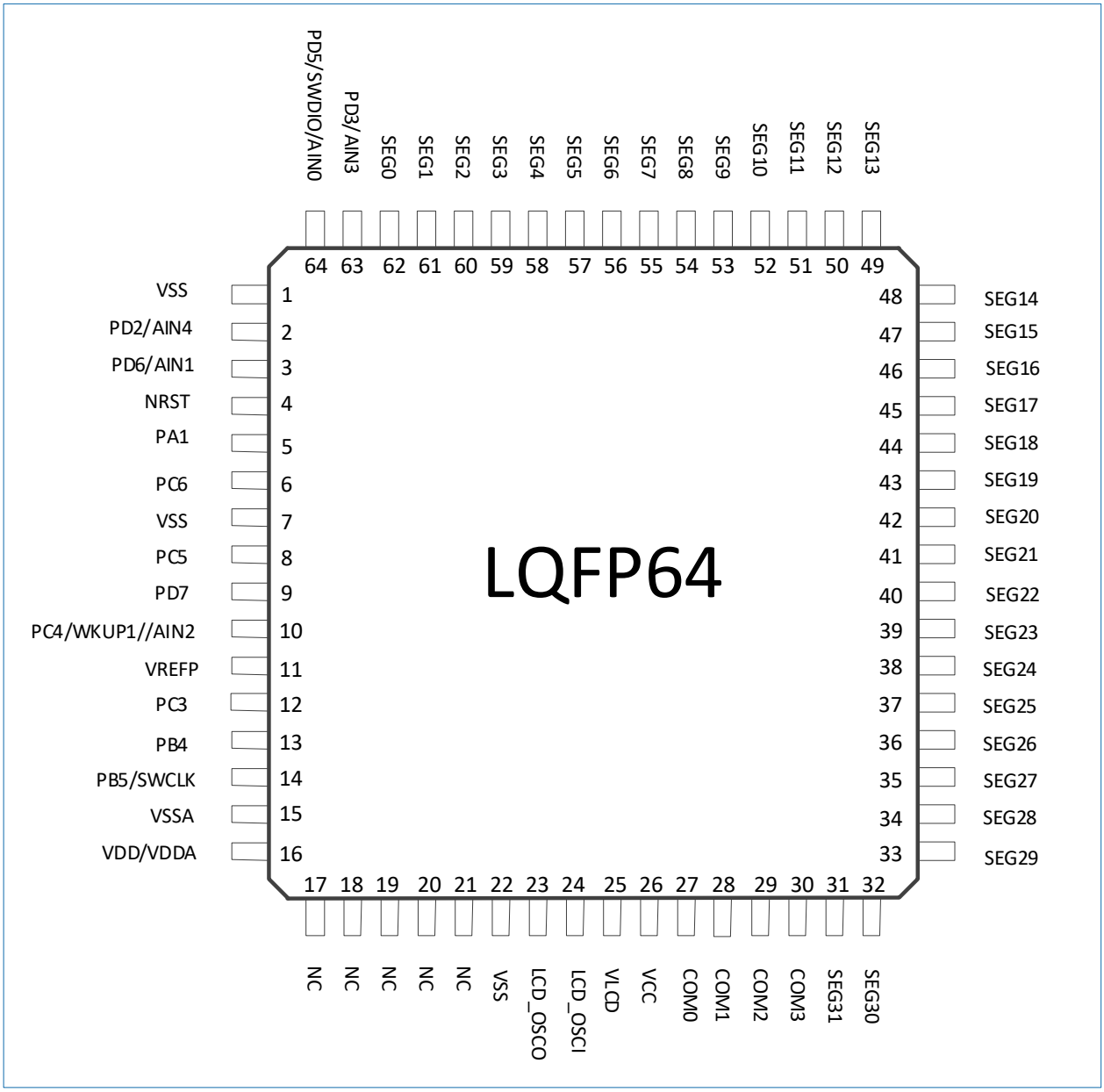

Figure 6-1 LQFP64 pinout

6.2 Pinout description

Table 6-1 LQFP64 pin description

Pin No.	Pin Name	Pin Type(1)	Default Function After Power-on	Default Alternate Function (AF0)
1	VSS	S	Digital ground	
2	PD2/AIN4(2)	I/O	PD2	-
3	PD6/AIN1(2)	I/O	PD6	-
4	NRST	I	NRST	GPIO
5	PA1/EXTCLK1	I/O	PA1	-
6	PC6	I/O	PC6	I2C1_SCL
7	VSS	S	Ground	
8	PC5/EXTCLK4	I/O	PC5	I2C1_SDA
9	PD7	I/O	PD7	-

Pin No.	Pin Name	Pin Type(1)	Default Function After Power-on	Default Alternate Function (AF0)
10	PC4/AIN2(2)	I/O	PC4	-
11	VREF(4)			
12	PC3	I/O	PC3	-
13	PB4	I/O	PB4	I2C1_SCL
14	PB5/SWCLK/EXTCLK3	I/O	SWCLK	SWCLK_I2C1_SDA(3)
15	VSSA	S	Analog ground	
16	VDD/VDDA	S	Digital/Analog power supply	
17	NC	-	-	-
18	NC	-	-	-
19	NC	-	-	-
20	NC	-	-	-
21	NC	-	-	-
22	VSS	S	Ground	
23	LCD_OSCO	O	OSC_OUT	-
24	LCD_OSCI	I	OSC_IN	-
25	VLCD	I	LCD power supply input	
26	VCC	S	LCD digital power supply	
27	COM0	I/O	LCD_COM0	-
28	COM1	I/O	LCD_COM1	-
29	COM2	I/O	LCD_COM2	-
30	COM3	I/O	LCD_COM3	-
31	SEG31	I/O	LCD_SEG31	-
32	SEG30	I/O	LCD_SEG30	-
33	SEG29	I/O	LCD_SEG29	-
34	SEG28	I/O	LCD_SEG28	-
35	SEG27	I/O	LCD_SEG27	-
36	SEG26	I/O	LCD_SEG26	-
37	SEG25	I/O	LCD_SEG25	-
38	SEG24	I/O	LCD_SEG24	-
39	SEG23	I/O	LCD_SEG23	-
40	SEG22	I/O	LCD_SEG22	-
41	SEG21	I/O	LCD_SEG21	-
42	SEG20	I/O	LCD_SEG20	-
43	SEG19	I/O	LCD_SEG19	-
44	SEG18	I/O	LCD_SEG18	-
45	SEG17	I/O	LCD_SEG17	-
46	SEG16	I/O	LCD_SEG16	-
47	SEG15	I/O	LCD_SEG15	-
48	SEG14	I/O	LCD_SEG14	-
49	SEG13	I/O	LCD_SEG13	-
50	SEG12	I/O	LCD_SEG12	-
51	SEG11	I/O	LCD_SEG11	-
52	SEG10	I/O	LCD_SEG10	-
53	SEG9	I/O	LCD_SEG9	-
54	SEG8	I/O	LCD_SEG8	-
55	SEG7	I/O	LCD_SEG7	-
56	SEG6	I/O	LCD_SEG6	-
57	SEG5	I/O	LCD_SEG5	-
58	SEG4	I/O	LCD_SEG4	-
59	SEG3	I/O	LCD_SEG3	-
60	SEG2	I/O	LCD_SEG2	-
61	SEG1	I/O	LCD_SEG1	-
62	SEG0	I/O	LCD_SEG0	-
63	PD3/AIN3(2)	I/O	PD3	N/A
64	PD5/SWDIO/AIN0(2)	I/O	SWDIO	SWDIO

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). The analog input to the ADC can be input through AIN0 – AIN4.

(3). For the PB5 pin, the SWCLK or I2C_SDA function is selected by configuring additional registers.

(4). VREF is internally connected to VDDA.

6.3 Alternate function table

Table 6-2 Alternate function table

Pin Name	AF0 (I2C/SWD)	AF1 (USART)	AF2 (SPI/I2S)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6 (Beeper)	AF7 (ADC)
PA1	-	-	-	TIM1_CH1N	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PB4	I2C_SCL	USART_RX	SPI_MISO/ I2S_MCK	TIM1_CH2N	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PB5	SWCLK_I2C_SDA (1)	USART_RX	SPI_NSS/ I2S_WS	TIM1_BKIN	TIM2_CH2	RCC_MCO	BEEP	ADC_ETR
PC3	-	USART_CK	-	TIM1_CH3_CH1N (2)	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC4	-	-	SPI_MISO/ I2S_MCK	TIM1_CH4_CH2N (2)	TIM2_CH4	RCC_MCO	BEEP	ADC_ETR
PC5	I2C_SDA	-	SPI_SCK/ I2S_CK	TIM1_ETR	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR
PC6	I2C_SCL	-	SPI_MOSI/ I2S_SD	TIM1_CH1	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PD2	-	-	SPI_MOSI/ I2S_SD	TIM1_CH2	TIM2_CH3	RCC_MCO	BEEP	ADC_ETR
PD5	SWDIO	USART_TX	-	TIM1_ETR	TIM2_ETR	RCC_MCO	BEEP	ADC_ETR
PD7	I2C_SMBA	USART_RX	SPI_NSS/ I2S_WS	TIM1_CH3	TIM2_CH1	RCC_MCO	BEEP	ADC_ETR

(1). The PB5 pin can be assigned to the SWCLK or I2C_SDA function by configuring the PB5_I2C1_SEL bit of the IOMUX pin function selection register.

(2). The PC3 pin can be assigned to the TIM1 CH3 or CH1N function by configuring the PC3_TIM1_SEL bit, and the PC4 pin can be assigned to the TIM1 CH4 or CH2N function by configuring the PC4_TIM1_SEL bit of the IOMUX pin function selection register.

Bit	2	1	0
	PB5_I2C1_SEL	**PC4_TIM1_SEL**	**PC3_TIM1_SEL**
Access mode	rw	rw	rw
Reset value	0	0	0

Figure 6-2 Alternate function selection of PB5/PC4/PC3

- If AF0 is assigned to PB5_AF, configure the PB5_I2C1_SEL bit to configure the function of PB5:
  - 0: PB5 is the input pin of SWCLK (the configuration when the system resets)
  - 1: PB5 is the SDA pin of I2C1
- If AF3 is assigned to PC4_AF, configure the PC4_TIM1_SEL bit to configure the function of PC4:
  - 0: PC3 is the CH4 pin of TIM1
  - 1: PC3 is the CH2N pin of TIM1
- If AF3 is assigned to PC3_AF, configure the PC3_TIM1_SEL bit to configure the function of PC3:
  - 0: PC3 is the CH3 pin of TIM1
  - 1: PC3 is the CH1N pin of TIM1

6.4 Pin multiplexing (IOMUX)

The mapping from multiple GPIOs or peripheral I/Os to one pin can be implemented by using IOMUX.

The following table uses pin 14 in Figure 6-1 as an example to describe pin multiplexing.

Table 6-3 Pin 14 multiplexing

Operation	Function of Pin 14
MCU reset	PB5 and the corresponding peripheral I/O in SYSCFG
Configuration of the IOMUX register	SWCLK

7 LQFP64 package

LQFP64 is a 12 mm × 12 mm, 0.5 mm pitch package.

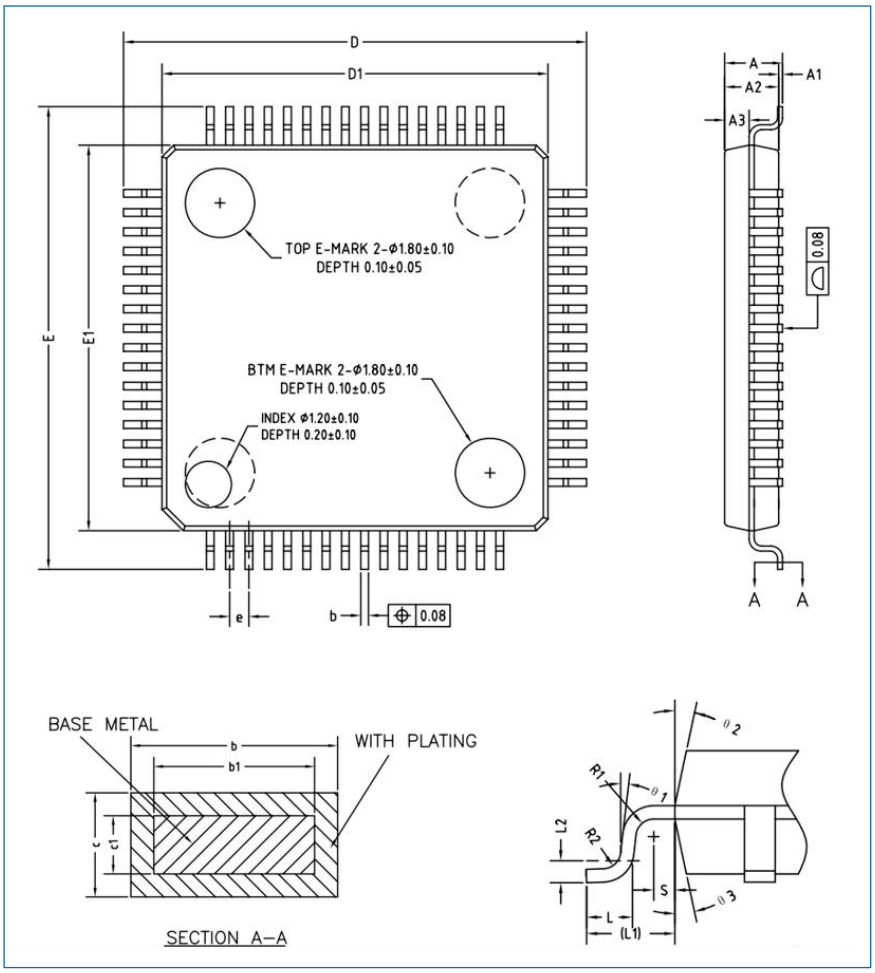

Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
A3	0.590	0.640	0.690
b	0.180	-	0.270
b1	0.170	0.200	0.270
c	0.130	-	0.180
c1	0.120	0.127	0.134
D	11.800	12.000	12.200
D1	9.900	10.000	10.100
E	11.800	12.000	12.200
E1	9.900	10.000	10.100
e	0.500BSC		
L	0.450	0.600	0.750
L1	1.000REF		
L2	0.25BSC		
R1	0.080	-	-
R2	0.080	-	0.200
S	0.200	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°

8 Ordering information

8.1 Device numbering conventions

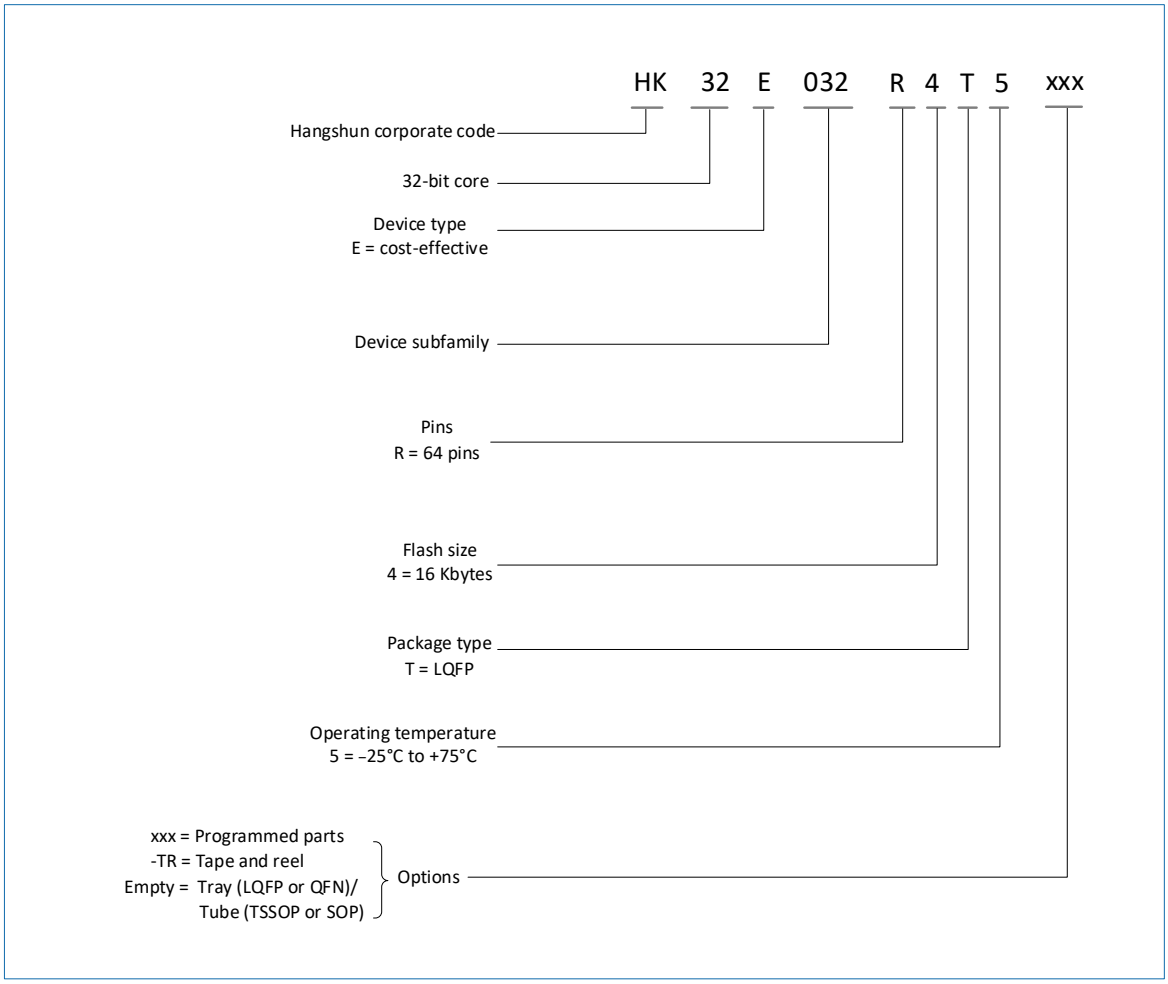

Figure 8-1 Device numbering conventions

8.2 Packaging information

Table 8-1 HK32E032 packaging information

Package	Part Number	Shipping Option	Remarks
LQFP64	HK32E032R4T5	Tray	-
LQFP64	HK32E032R4T5-TR	Tape and reel	-

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EEPROM	Electrically Erasable Programmable Read-only Memory
EXTI	Extended Interrupt/Event Controller
GPIO	General-purpose Input/Output
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PWM output	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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Shenzhen Hangshun Chip Technology R&D Co., Ltd.

TEL: +86-755-83247667

Website: www.hsxp-hk.com