HK32D010 Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32D010 series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32D010.

Audience

This document is intended for:

- HK32D010 developers
- HK32D010 testers
- HK32D010 users

Release Notes

This document is applicable to HK32D010 series MCUs.

Revision History

Version	Date	Description
1.0	2023/11/03	The initial release.

Contents

1 Introduction

This document is the datasheet for HK32D010 series MCUs. HK32D010 is a family of LCD/LED display MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32D010K8T7 (LQFP32 package)
- HK32D010S8T7 (LQFP44 package)
- HK32D010C8T7 (LQFP48 package)

For more details of HK32D010, see *HK32D010 User Manual*.

2 Product overview

HK32D010 adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 32 MHz. Each HK32D010 MCU has 64 Kbytes of Flash and 4 Kbytes of SRAM. You can configure the Flash controller register to remap interrupt vectors in the 16-Kbyte space.

Except for the power pin and ground pin, all the other pins of HK32D010 can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32D010 incorporates a wide selection of communication interfaces:

- 6 × high-speed UARTs of up to 4 Mbit/s
- 1 × high-speed SPI of up to 16 Mbit/s

  The SPI supports the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, and automatic CRC.
- 1 × high-speed I2C of up to 400 kbit/s

  The I2C supports the 100 kbit/s and 400 kbit/s transmission rates, master and slave modes, multimaster mode, 7-bit and 10-bit addressing, and SMBus protocol. The I2C can wake up the MCU from Stop mode when receiving data.

HK32D010 embeds two 16-bit general-purpose PWM timers (seven PWM outputs in total) and a 16-bit basic timer (for periodic outputs of CPU interrupts).

HK32D010 also incorporates the analog circuitry: a 12-bit ADC (1 MSPS), a power-on reset (POR)/power-down reset (PDR)/brown-out reset (BOR) circuit, and an internal reference voltage (sampled by ADC on chip).

HK32D010 can operate in the –40°C to +105°C temperature range, from a 2.6 V to 5.5 V power supply. It meets the environmental requirements of most applications.

With its diversified peripheral interfaces, HK32D010 is suitable for a wide range of applications:

- Programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Low-power terminals with sensors for Internet of Things (IoT)
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots
- Smartwatches and fitness trackers

2.1 Features

- CPU core
  - ARM® Cortex™-M0
  - Maximum frequency: 32 MHz
  - 24-bit SysTick timer
  - Supports the remapping of interrupt vectors (by configuring the Flash controller register)
- Operating voltage range: 2.6 V to 5.5 V
- Operating temperature range: –40°C to +105°C
- Typical operating current Run mode
  - 0.493 mA@3.3 V@40 kHz

    - 1.494 mA@3.3 V@8 MHz
    - 4.095 mA@3.3 V@32 MHz
  - Sleep mode
    - 352 µA@3.3 V@40 kHz
    - 736 µA@3.3 V@8 MHz
    - 1681 µA@3.3 V@32 MHz
  - Stop mode
    - Normal: 333.9 µA@3.3 V@40 kHz
    - Low-power: 3.62 µA@3.3 V@40 kHz
- 64-Kbyte Flash (256 pages, 256 bytes per page; 32-bit read/write)
  - Separate read and write protection for Flash data
- 4-Kbyte SRAM
- Clock
  - High-speed internal clock (HSI): 32 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - High-speed external clock (HSE): 4 MHz to 32 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - GPIO external input clock: 32 MHz (maximum value)
- Reset
  - Low level on the NRST pin (external reset)
  - Window watchdog reset (WWDG reset)
  - Independent watchdog reset (IWDG reset)
  - Power reset
  - Software reset (SW Reset)
  - Low-power management reset
- GPIO
  - Up to 42 GPIOs
  - Each can be used for external interrupt inputs
  - Built-in switchable pull-up/pull-down resistors
  - Open-drain output supported
  - Output drive capacity configurable
- Pin multiplexing (IOMUX)
- Cyclic redundancy check (CRC) hardware implementation unit
- Data communication interfaces
  - 6 × high-speed UARTs of up to 4 Mbit/s
  - 1 × high-speed I2C of up to 400 kbit/s: can wake up the MCU from Stop mode when receiving data
  - 1 × high-speed SPI of up to 16 Mbit/s
- Timer and PWM generator
  - 2 × 16-bit general-purpose PWM timers (seven PWM outputs in total)
  - 1 × 16-bit basic timer

- LCD
  - Can drive 8 × 24 or 4 × 28 pixels
  - Supports the display in low-power modes.
  - The double buffered memory allows LCD_RAM data to be updated at any time.
- LED
  - LED dot matrix and LED matrix supported
- RTC
  - Provides the clock calendar function
- Beeper
  - In Stop mode, the beeper can trigger ADC sampling periodically.
- On-chip analog circuitry
  - 1 × 12-bit ADC (1 MSPS, up to six external analog input channels and three internal channels, differential pair input supported)
  - 1 × POR/PDR/BOR circuit
  - 1 × internal reference voltage (sampled by ADC on chip)
- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- UID
  - Each HK32D010 MCU provides a 96-bit UID.
- Reliability
  - Passed HBM6000/CDM2000 level tests.

2.2 Device overview

Table 2-1 HK32D010 series features

Feature		HK32D010K8T7	HK32D010S8T7	HK32D010C8T7
GPIO		30	42	42
Package		LQFP32	LQFP44	LQFP48
Operating voltage		2.6 V to 5.5 V		
Operating temperature		–40°C to +105°C		
Memory	Flash (Kbyte)	64 (including 61 Kbytes of main Flash1 and three Kbytes of bootloader/main Flash2(1))		
	SRAM (Kbyte)	4		
CPU	Core	Cortex®-M0		
	Frequency	32 MHz		
Clock	Low-speed internal clock (LSI)	40 kHz		
	High-speed internal clock (HSI)	32 MHz		
	Low-speed external clock (LSE)	32.768 kHz		
	High-speed external clock (HSE)	4 MHz – 32 MHz		

Feature		HK32D010K8T7	HK32D010S8T7	HK32D010C8T7
	External GPIO clock	32 MHz (maximum value)		
Timer	General-purpose timer	2 (16-bit): TIM3, TIM15		
	Basic timer	1 (16-bit): TIM6		
	SysTick timer	1		
	IWDG	Supported		
	WWDG	Supported		
Comm. peripheral	UART	6		
	I2C	1		
	SPI (I2S not supported)	1		
LCD		1		
LED		1		
Beeper		1		
COMP		1		
ADC	ADC (Channels)	1 (5 external channels)	1 (6 external channels)	1 (6 external channels)
	Reference selection	Internal reference voltage		
	ADC sampling rate	1 MSPS (12-bit ADC)		
	ADC accuracy	12-bit		
CRC		Supported		
96-bit UID		Supported		

(1). The 64-Kbyte Flash memory comprises 61 Kbytes of main Flash1 and three Kbytes of bootloader that can be used as main Flash2 by configuring the option byte.

3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor that provides an MCU platform featuring low cost and low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M0 core, the HK32D010 family is compatible with ARM tools and software.

The following figure shows the block diagram of HK32D010C8T7 as an example:

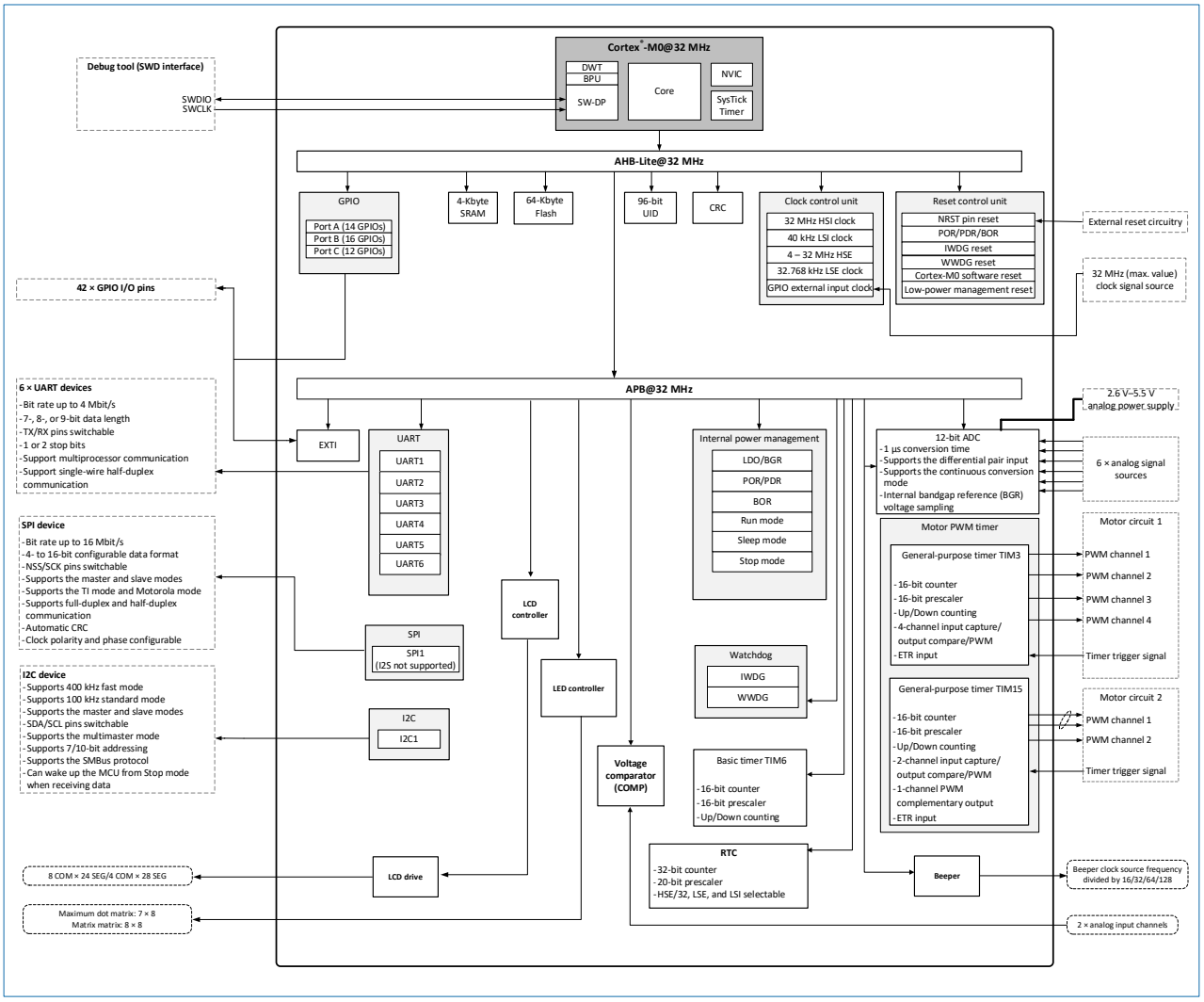

Figure 3-1 HK32D010C8T7 block diagram

3.2 Memory mapping

The following figure shows the memory mapping of HK32D010 MCUs:

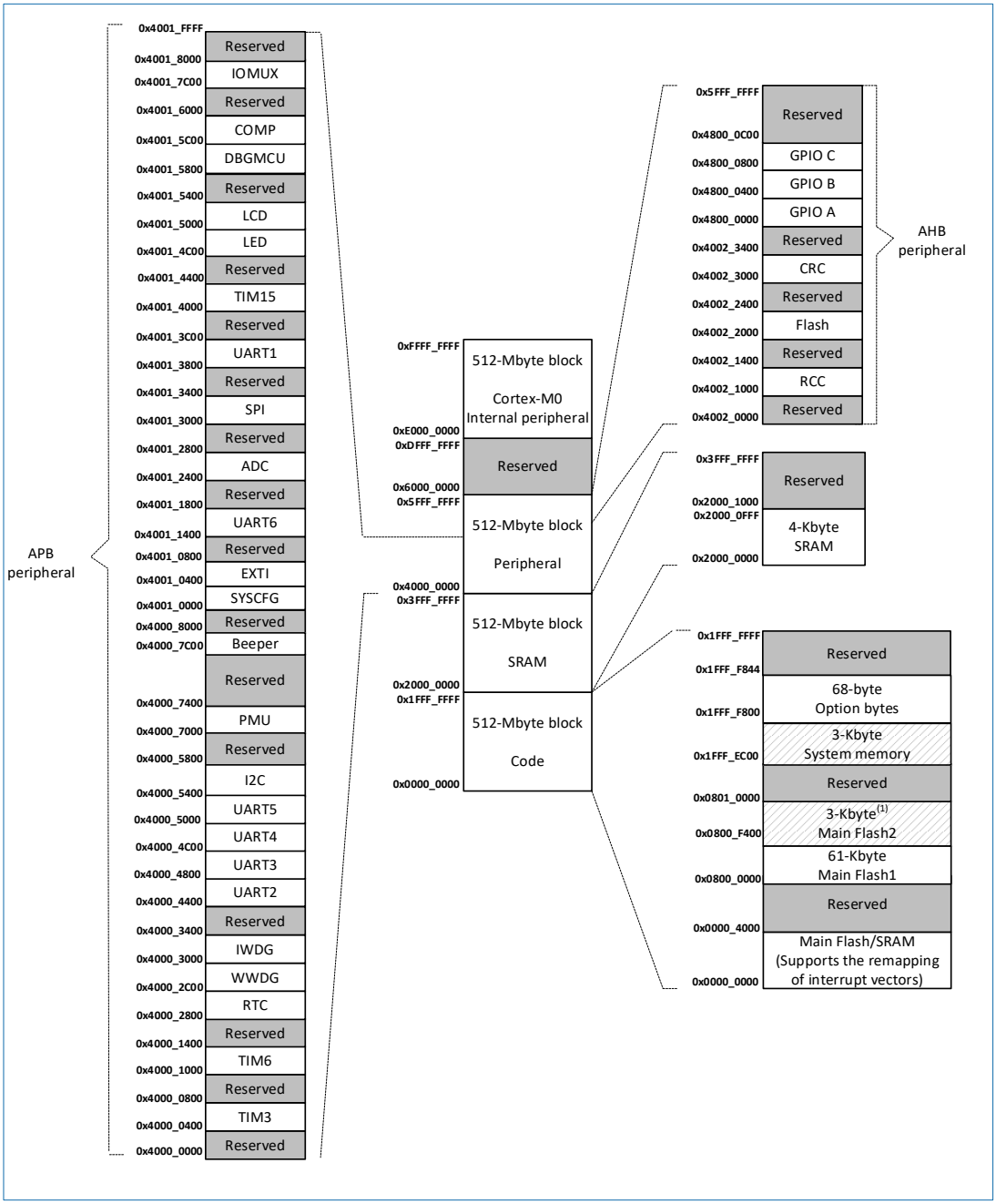

Figure 3-2 HK32D010 memory mapping

(1). The main Flash area and system memory area cannot be used at the same time. You can configure the option byte to use either the main Flash area or the system memory area.

3.3 Memory

3.3.1 Flash

HK32D010 integrates a Flash memory of up to 64 Kbytes to store programs and data. The Flash memory comprises 61 Kbytes of main Flash and three Kbytes of bootloader that can be used as main Flash by configuring the option byte.

You can configure the Flash controller register to remap interrupt vectors.

3.3.2 SRAM

HK32D010 integrates a 4-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.4 CRC calculation unit

Cyclic redundancy check (CRC) is used to verify data integrity during transmission and storage. HK32D010 integrates a CRC calculation unit to reduce application processing burden and accelerate processing.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with the reference signature which is generated at link time and stored at a specified memory location.

3.5 Power supply scheme

HK32D010 has a single power supply. V_{DD} and V_{DDA} supply power to the digital circuitry and analog circuitry of the MCU via the same pin.

V_{DD}/V_{DDA} range: 2.6 V to 5.5 V.

3.6 Power supply monitor

HK32D010 embeds the power-on reset (POR)/power-down reset (PDR) circuitry. (By default, the BOR circuitry is disabled). The POR/PDR circuitry keeps operating to ensure that the system runs properly when the power supply exceeds 2.6 V. When V_{DD}/V_{DDA} is lower than the specified V_{POR}/V_{PDR} threshold, the MCU will be reset without using any external reset circuit.

When BOR is enabled, BOR guarantees that the MCU is in the reset state during the power-on process until the supply voltage reaches the specified V_{BOR} threshold. When BOR is disabled, the power supply is under the monitoring of POR/PDR.

3.7 Low-power modes

HK32D010 supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain and the HSI oscillator are disabled. MCUs can be woken up from Stop mode by any EXTI line.

3.8 Resets

HK32D010 supports the system reset and power reset.

3.8.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain.

You can identify the reset source by checking reset status flags in the RCC_CSR register.

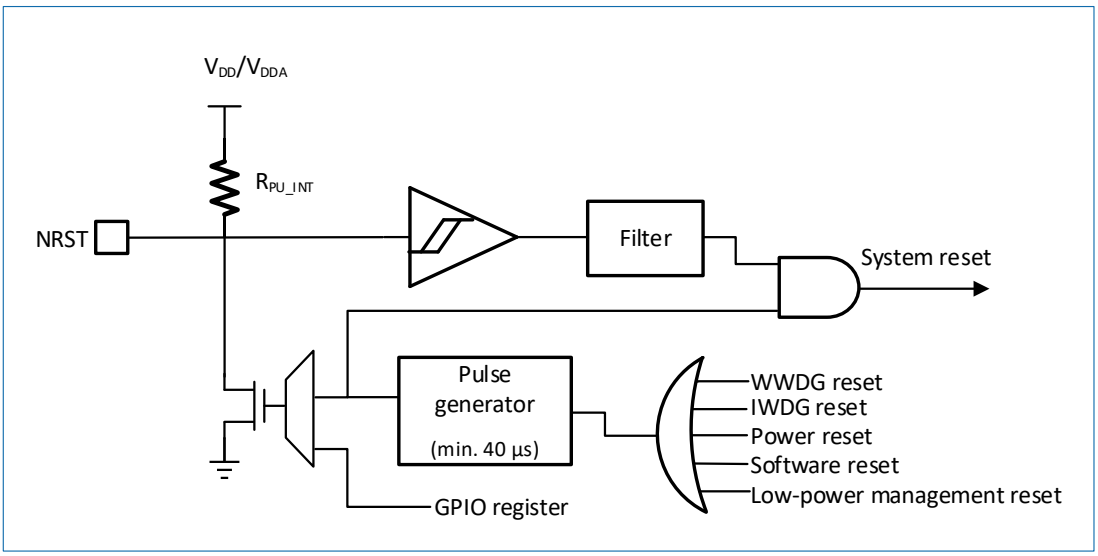

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Power reset
- Software reset (SW Reset)
- Low-power management reset

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004. The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.8.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Brown-out reset (BOR)

3.9 Clocks and clock tree

The following figure shows the clock tree of HK32D010.

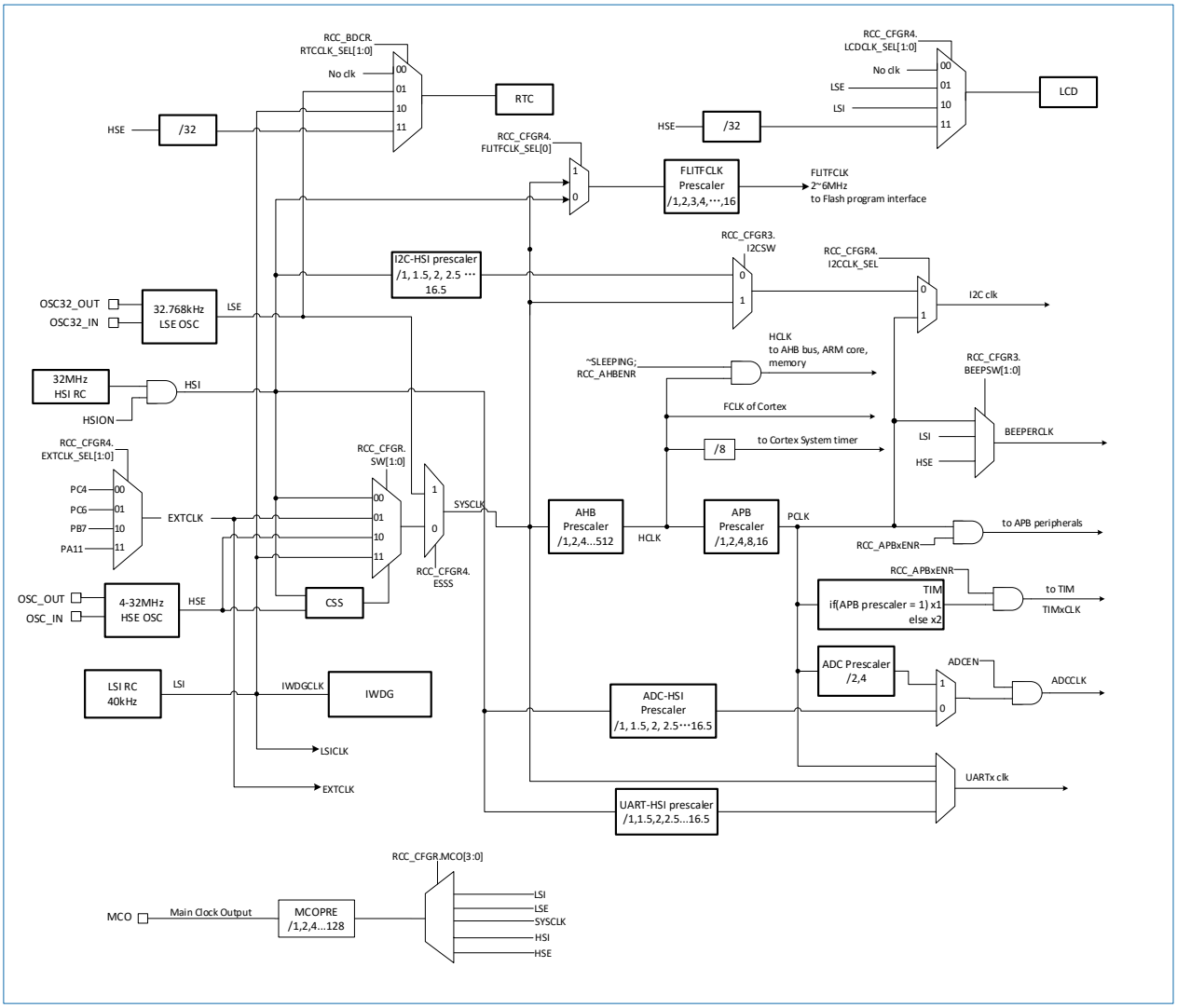

Figure 3-4 Clock tree of HK32D010

As Figure 3-4 shows, HK32D010 supports the following clock sources:

- High-speed external clock (HSE): 4 MHz to 32 MHz
- Low-speed external clock (LSE): 32.768 kHz
- High-speed internal clock (HSI): 32 MHz
- Low-speed internal clock (LSI): 40 kHz
- GPIO external input clock: 32 MHz (maximum value)

Each clock source can be enabled and disabled independently. The clock source not in use can be disabled to reduce power consumption. Multiple prescalers are available for the configuration of AHB and APB clock domains. The maximum clock frequency of AHB and APB clock domains is 32 MHz. The AHB clock (HCLK) divided by eight can drive the Cortex system timer (by configuring the Cortex SysTick configuration bit).

All peripheral clocks are driven by the clock (HCLK or PCLK) of the bus to which the peripheral is connected. However, there are some exceptions:

- The Flash programming interface clock (FLITFCLK) is driven by the HSI clock or SYSCLK (selected by using the software).
- The clock source of I2C is one of the following (selected by using the software):
  - SYSCLK
  - 32 MHz HSI divided by the I2C-HSI prescaler

- APB clock (PCLK)

- The FCLK of Cortex is provided by AHB clock (HCLK).
- The clock of AHB, ARM core, and memory is provided by the AHB clock (HCLK).
- The clock source of ADC is one of the following (selected by using the software):
  - APB clock (PCLK) divided by 2 or 4 by the ADC prescaler
  - 32 MHz HSI divided by the ADC-HSI prescaler
- The clock source of UART is one of the following (selected by using the software):
  - PCLK
  - SYSCLK
  - 32 MHz HSI divided by the UART-HSI prescaler
- The APB clock (PCLK) or the APB clock (PCLK) multiplied by two provides the timer clock. (The clock frequency is selected by using the software and implemented by hardware.)

The reset and clock controller (RCC) uses the AHB clock (HCLK) divided by eight as the external clock of the Cortex SysTick timer. You can set the SysTick control/status register to select HCLK/8 as the SysTick timer clock.

3.10 RTC

The real-time clock (RTC) has a set of continuously running counters and can provide the clock calendar function via software. In addition, the RTC provides the alarm interrupt and seconds interrupt which can be the wakeup sources in Stop mode. This RTC does not provide the back register and clock calibration functions.

The RTC can be clocked by HSE/32, LSE, or LSI. Its 32-bit programmable counter can work with the alarm register to realize long-term measurement and generate alarm events. The RTC has a 20-bit prescaler which is used to generate the time base clock. When the RTC is clocked by the 32.768 kHz crystal oscillator (LSE) and the prescaler register is configured as 0x7FFF, a 1-second time base is generated.

3.11 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. I/O alternate functions can be locked as needed to prevent unexpected writes to the I/O registers.

3.12 SYSCFG

The HK32D010 MCU has a set of configuration registers that provide the following functions:

- Remapping memory areas
- Managing the connections between external interrupts and GPIOs
- Managing the reliability feature of the system.

3.13 IOMUX

Some pins of the HK32D010 MCU support GPIO or IOMUX. You can configure the IOMUX register to assign an alternate function to a pin.

The following pins support IOMUX:

- NRST (alternate function: PA0)
- TIM3_CH1 (alternate function: HSI or LSI clock input)

3.14 Boot modes

The configuration of the option byte or the configuration of the option byte and Boot0 (PA7) pin determines the

boot mode. The boot modes include:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The system memory embeds the bootloader program that is programmed into the MCU during production. The bootloader program can reprogram the main Flash via the UART5 PA10/PA11 pins.

3.15 Interrupts and events

3.15.1 NVIC

HK32D010 incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 22 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities while maintaining the lowest interrupt latency.

- The closely coupled NVIC ensures low-latency interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

3.15.2 EXTI

The extended interrupt/event controller (EXTI) manages internal and external interrupts and events. It outputs event requests to the CPU, outputs interrupt requests to the interrupt controller, and outputs wakeup requests to the power supply control module.

EXTI can be categorized into edge-configurable EXTI and edge-fixed EXTI. Their differences are:

Edge-configurable EXTI:

- The trigger edge can be the rising edge or falling edge.
- The pending register maintains interrupt status.
- The software interrupt/event register EXTI_SWIER can be configured for the simulated generation of interrupts/events.

Edge-fixed EXTI:

- Only the rising edge is the trigger edge.
- The EXTI is used to wake up the core from Stop mode and it only operates in Stop mode.
- The interrupt status of edge-fixed EXTI is not recorded in the pending register but is provided by the corresponding IP.

The EXTI manages up to 20 internal and external interrupts/events. The interrupt or event of each input line can be masked independently.

The main features of EXTI include:

- Manages up to 20 interrupt/event requests
    - 18 edge-configurable EXTI lines
        - Configurable trigger edge: rising edge or falling edge

- Dedicated flag for the interrupt status bit
- Interrupts and events can be triggered by software.

◦ Two edge-fixed EXTI lines.

- Each interrupt line or event line can be triggered and masked independently.
- Detects external signals whose pulse width is shorter than the APB clock period.

3.16 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent RC oscillator (LSI). The RC oscillator is independent of the main clock, so it can operate in Stop mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use IWDG in window mode.

3.17 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.18 Timers

HK32D010 has two general-purpose timers and a basic timer. The following table describes the features of timers.

Table 3-1 Features of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	Break Input	Capture/ Compare Channels	Complementary Outputs
General-purpose timer	TIM3	16-bit	Up, down, up/down	1 to 65536	No	4	No
	TIM15	16-bit	Up, down, up/down	1 to 65536	Yes	2	1
Basic timer	TIM6	16-bit	Up, down	1 to 65536	No	No	No

3.18.1 General-purpose timer

HK32D010 integrates general-purpose timers TIM3 and TIM15.

- TIM3

TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. It has four independent channels. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output.

TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

- TIM15

TIM15 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. It has complementary outputs with programmable inserted dead-times. TIM15 has two channels for input capture, output compare, PWM output, and one-pulse mode output. In debug mode, the counter can be frozen.

3.18.2 Basic timer

HK32D010 integrates a basic timer TIM6.

TIM6 embeds a 16-bit up/down counter and a 16-bit prescaler. It is used to generate periodic CPU interrupt requests. In debug mode, the counter can be frozen.

3.18.3 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.19 ADC

The ADC of HK32D010 has the following features:

- A total of eight channels. Channels AIN0 to AIN5 are external channels connected to I/O pins. AIN6 is an internal channel connected to the internal reference voltage internal. AIN7 is an internal channel connected to the internal power management unit (PMU, only for the calibration of internal power supply voltage).
- Supports the differential pair input mode. AIN0 and AIN1, AIN2 and AIN3, AIN4 and AIN5 form three differential pairs. (When ADC is configured to the differential pair input mode, AIN6 and AIN7 are unavailable.)
- Supports only the 12-bit ADC sampling resolution.

3.20 COMP

HK32D010 incorporates a voltage comparator (COMP). The comparator can be used independently (through the specified GPIO). It can also be used:

- To wake up the MCU from low-power modes after being triggered by the analog signal.
- For analog signal conditioning.
- Together with the timer PWM output to form the cycle-by-cycle current control loop.

3.21 Beeper

An ultra-low-power 7-bit timer is embedded in the beeper. The operating clock of the timer can be configured to PCLK, LSI, or HSE. The timer adopts the down-counting mode and can output pulses at the clock source frequency divided by 16, 32, 64, or 128.

In Stop mode, the beeper keeps operating and can trigger ADC sampling periodically. The frequency at which ADC sampling is triggered is 1/1024 of the frequency of the pulse output by the beeper. For example, if the beeper outputs 1 kHz pulses, ADC sampling is triggered at a frequency of 1 kHz/1024 ≈ 0.98 Hz (at an interval of about 1.02s).

3.22 I2C bus

The I2C bus interface can work as a master or slave and supports the standard and fast modes. The I2C bus interface supports the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interface embeds hardware CRC generation/verification and supports SMBus V2.0/PMBus. The following table lists the I2C features:

Table 3-2 I2C features

I2C Feature	I2C
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast mode	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported

I2C Feature	I2C
Event management	Supported
Clock stretching	Supported
Software reset	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Wakeup from Stop mode	Supported

3.23 UART

HK32D010 has six built-in universal asynchronous receivers/transmitters (UART1/UART2/UART3/UART4/UART5/UART6). The following table lists the UART features:

Table 3-3 UART features

UART Mode/Feature	UART1/2/3/4/5/6
Data word length	7/8/9-bit
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported
Dual clock domains	Supported

3.24 SPI

A serial peripheral interface (SPI) is embedded in each HK32D010 MCU. The SPI interface supports full-duplex and half-duplex communication in master or slave mode. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4-bit to 16-bit. The following table lists the SPI features:

Table 3-4 SPI features

SPI Feature	SPI
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported
I2S mode	Not supported

3.25 LCD

HK32D010 incorporates the drive circuit of segment liquid crystal displays (LCDs) and can drive 8 × 24 or 4 × 28 pixels.

- Supports the static mode, 1/2, 1/3, 1/4, and 1/8 duty cycle.
- Supports 1/2, 1/3, and 1/4 bias.
- Programmable blinking frequency of 1, 2, 3, 4, 8, or all pixels.
- The double buffered memory allows LCD_RAM data to be updated at any time.
- Supports the display in low-power modes.
- Highly flexible frame rate control.
- Contrast configurable.
- Start of frame interrupt.

3.26 LED

The light-emitting diode (LED) module can drive the LED array. Based on the application scenarios, the LED array can be categorized into LED dot matrix or LED matrix.

- LED dot matrix
  - Drives up to 56 LED lighting diodes organized into 4 × 5, 5 × 6, 6 × 7, and 7 × 8 arrays

- Conduction time of a single LED lighting diode configurable: from 16 μs to 4,096 μs
- The 4 × 5 array can be started from LED0/LED3.
- The scanning is performed from PB0 to PB7 and can be started from any I/O in the PB0 – PB7 range.
- The LED dot matrix is unique, which means that its connection form cannot be modified.

- LED matrix
  - Drives the LED matrix of up to 8COM × 8SEG. The numbers of COMs and SEGs are configurable.
  - Conduction time of a single COM: configurable from 16 μs to 4096 μs
  - Duty cycle of the single COM conduction time: configurable from 1/8 to 1.
- The I/O status can be switched to high level, low level, or high impedance through automatic scanning. This way, the lighting of a single LED lighting diode can be independently controlled.
- The double-buffered memory allows the firmware to update the LED_DC register data at any time without impact on the LED display.
- Supports the one-shot scanning and continuous scanning modes.
- End of frame interrupt

3.27 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32D010 MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process of the security mechanism.

3.28 Debug port

Based on the ARM SWJ-DP embedded in HK32D010, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	5.5	V
V_{IN}	Input voltage on pins	–0.3	5.5	
$\|V_{SSX} – V_{SS}\|$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	105	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	30	
	Output current sourced by any I/O and control pin	30	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–55	130	°C
T_J	Maximum junction temperature	–55	130	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	32	
f_{PCLK2}	Internal APB2 clock frequency	-	32	
V_{DD}	Standard operating voltage	2.6	5.5	V
V_{REFP} (1)	Analog operating voltage	2.6	5.5	V

Symbol	Description	Min	Max	Unit
T	Operating temperature	–40	105	°C

(1). V_{REFP} can be lower than V_{DD}. For example, V_{DD} = 4.2 V, V_{REFP} = 3.3 V; V_{DD} = 3.3 V, V_{REFP} = 2.5 V.

4.2.2 BOR characteristics

Table 4-5 BOR characteristics

Symbol	Parameter	Level	Min	Typ	Max	Unit
VBOR (1)	BOR detection level selection (V_{DD} rising edge) (–40°C to 105°C)	V_{BOR1}	2.529	2.781	2.951	V
		V_{BOR2}	2.892	3.18	3.38	
		V_{BOR3}	3.269	3.59	3.802	
		V_{BOR4}	3.612	3.96	4.189	
		V_{BOR5}	3.971	4.361	4.608	
		V_{BOR6}	4.342	4.748	5.019	
		V_{BOR7}	4.711	5.246	5.451	
	BOR detection level selection (V_{DD} falling edge) (–40°C to 105°C)	V_{BOR1}	2.468	2.658	2.819	
		V_{BOR2}	2.847	3.017	3.246	
		V_{BOR3}	3.217	3.461	3.677	
		V_{BOR4}	3.588	3.863	4.095	
		V_{BOR5}	3.967	4.257	4.518	
		V_{BOR6}	4.339	4.652	4.927	
		V_{BOR7}	4.697	5.091	5.325	
$V_{BORhyst}$	BOR hysteresis	-	-	100	-	mV
t_{BORRST}(2)	Time for BOR to take effect after reaching the threshold	-	-	10	-	µs

(1). BOR is based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge	1.57	1.91	2.31	V
		Rising edge	1.80	2.06	2.56	V
$V_{PDRhyst}$	PDR hysteresis	-	-	100	-	mV
$t_{RSTTEMPO}$(2)	Reset duration	-	-	2	-	ms

(1). PDR and POR are based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	-	1.2	-	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition	Parameter	V_{DD} = 3.3 V			V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	–40°C	25°C	105°C	
Run mode	SYSCLK = **8 MHz (HSE)**; Except for Flash, SRAM, and RCC, all the other peripherals disabled; All I/Os configured in high impedance; Zero wait states to access Flash.	Current	1436	1494	1647	1500	1568	1732	µA
	SYSCLK = **32 MHz (HSI)**; Except for Flash, SRAM, and		3928	4095	4285	5615	5705	5839	µA

Mode	Condition	Parameter	V_{DD} = 3.3 V			V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	–40°C	25°C	105°C	
	RCC, all the other peripherals disabled; All I/Os configured in high impedance; One wait state to access Flash.								
	SYSCLK = **40 kHz (LSI)**; Except for Flash, SRAM, and RCC, all the other peripherals disabled; All I/Os configured in high impedance; Zero wait states to access Flash.		465	493	589	483	511	612	µA
	SYSCLK = **32.768 kHz (LSE)**; Except for Flash, SRAM, and RCC, all the other peripherals disabled; All I/Os configured in high impedance; Zero wait states to access Flash.		467	492	584	486	511	606	µA
Sleep mode 1	SYSCLK = **8 MHz (HSE)**; AHB/APB disabled; Core clock disabled; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; SRAM and peripheral data retained. Zero wait states to access Flash.	Current	673	736	899	677	755	926	µA
		Wakeup time	-	-	-	-	3.15	-	µs
Sleep mode 2	SYSCLK = **32 MHz (HSI)**; AHB/APB disabled; Core clock disabled; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; SRAM and peripheral data retained. One wait state to access Flash.	Current	1584	1681	1842	1487	1578	1741	µA
		Wakeup time	-	-	-	-	500	-	ns
Sleep mode 3	SYSCLK = **40 kHz (LSI)**; AHB/APB disabled; Core clock disabled; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; SRAM and peripheral data retained. Zero wait states to access Flash.	Current	305	352	462	315	363	478	µA
		Wakeup time	-	-	-	-	310	-	µs

Mode	Condition	Parameter	V_{DD} = 3.3 V			V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	–40°C	25°C	105°C	
Sleep mode 4	SYSCLK = 32.768 kHz (LSE); AHB/APB disabled; Core clock disabled; All I/Os configured in high impedance; Except for Flash, SRAM, and RCC, all the other peripherals disabled; SRAM and peripheral data retained. Zero wait states to access Flash.	Current	306	352	461	316	363	479	μA
		Wakeup time	-	-	-	-	825	-	μs
Stop mode	All clocks in the core domain stopped; HSI disabled, LSI oscillator enabled; LDO operating in normal mode; All I/Os configured in high impedance; All peripherals disabled.	Current	290.8	333.9	442.9	303.3	349.5	457.2	μA
		Wakeup time	-	-	-	-	6.1	-	μs
Low-power stop mode	All clocks stopped; HSI disabled, LSI oscillator enabled; LDO operating in low-power mode; All I/Os configured in high impedance; All peripherals disabled.	Current	1.75	3.62	37.96	3.48	5.41	43.83	μA
		Wakeup time	-	-	-	-	100	-	μs

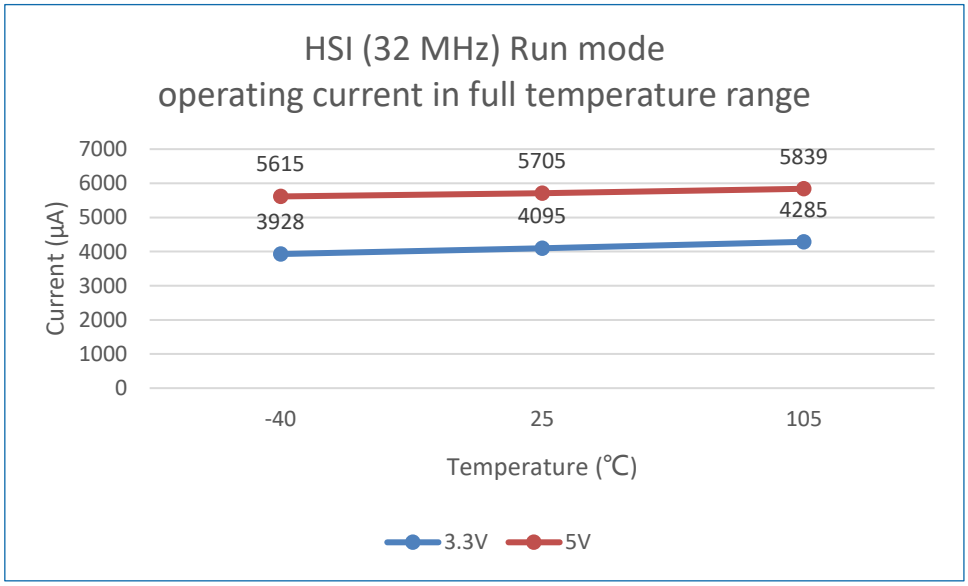

Figure 4-1 HSI (32 MHz) Run mode operating current in full temperature range

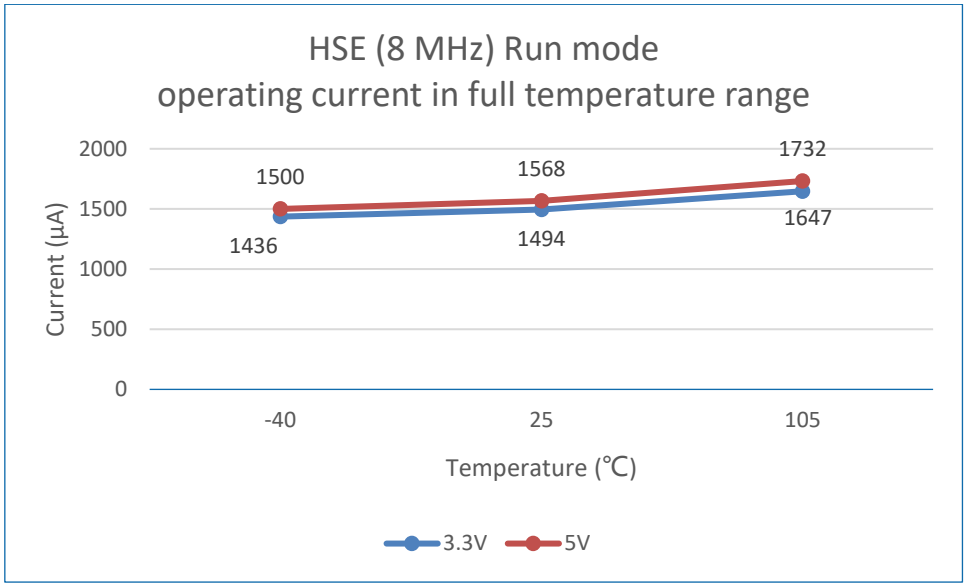

Figure 4-2 HSE (8 MHz) Run mode operating current in full temperature range

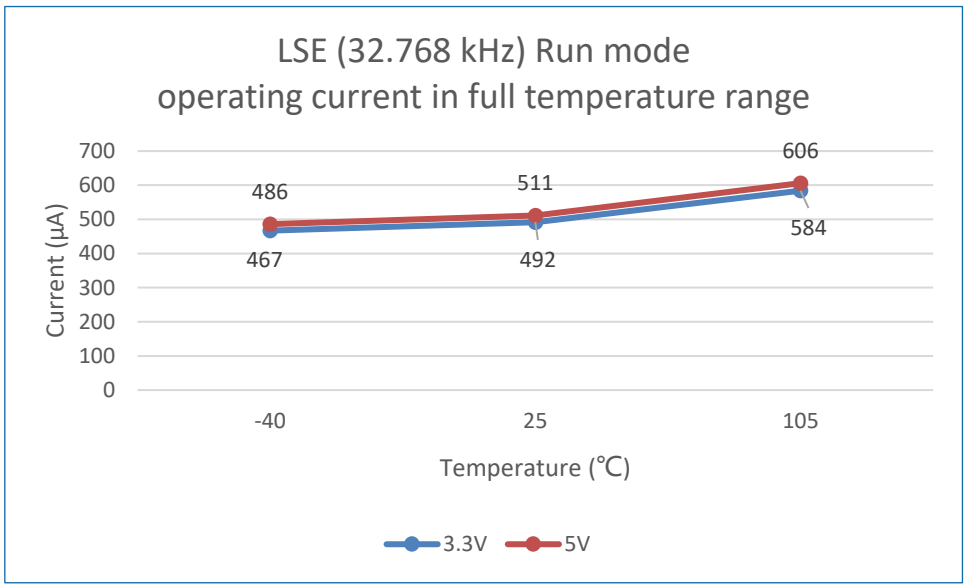

Figure 4-3 LSE (32.768 kHz) Run mode operating current in full temperature range

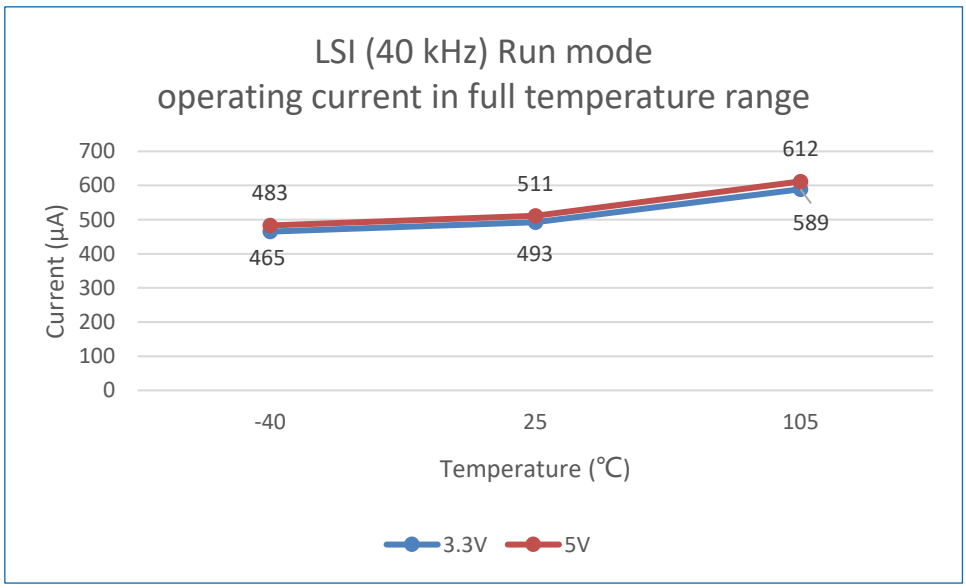

Figure 4-4 LSI (40 kHz) Run mode operating current in full temperature range

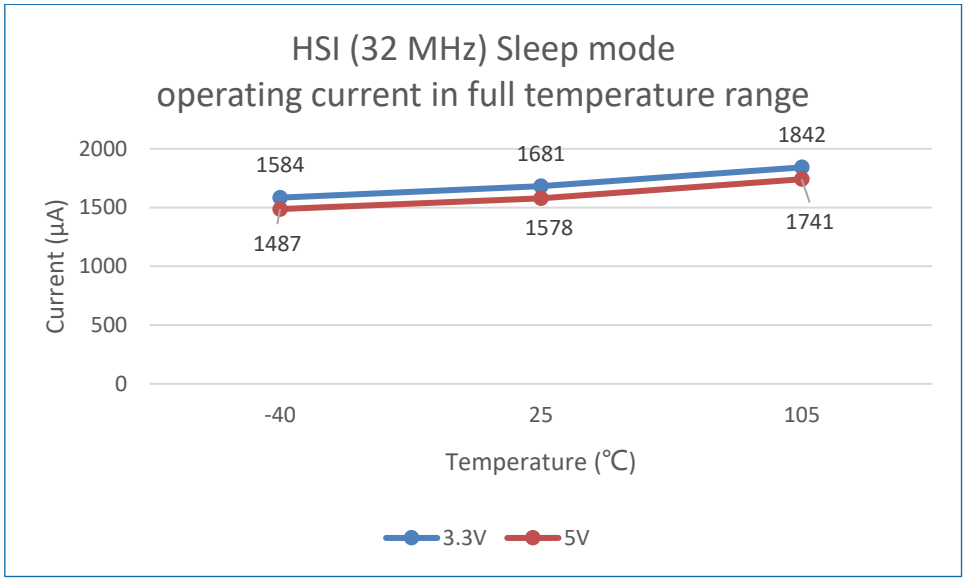

Figure 4-5 HSI (32 MHz) Sleep mode operating current in full temperature range

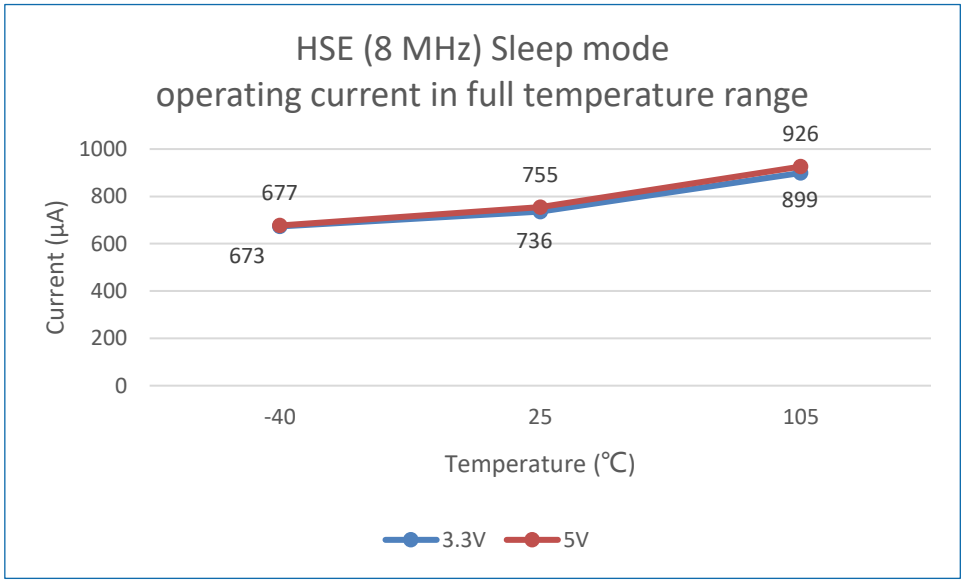

Figure 4-6 HSE (8 MHz) Sleep mode operating current in full temperature range

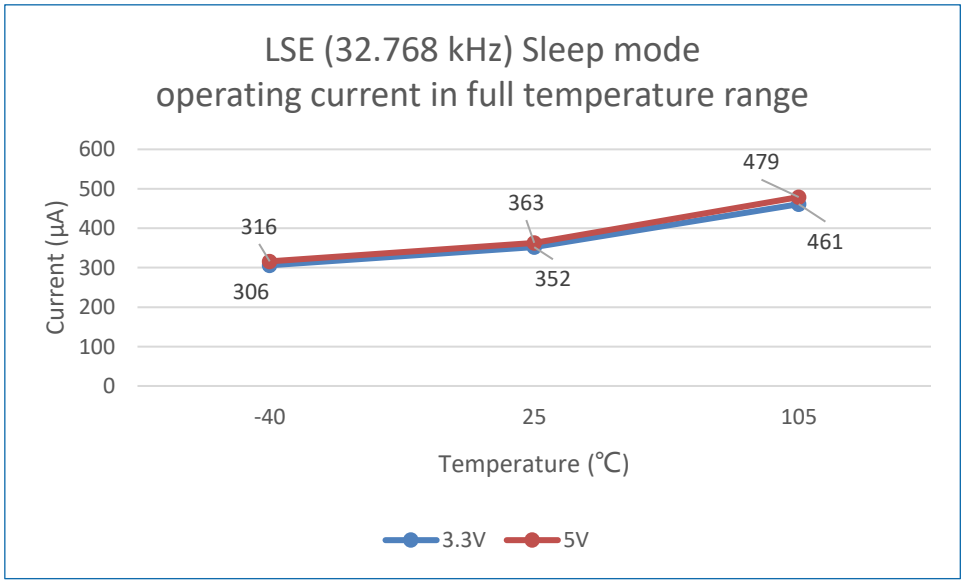

Figure 4-7 LSE (32.768 kHz) Sleep mode operating current in full temperature range

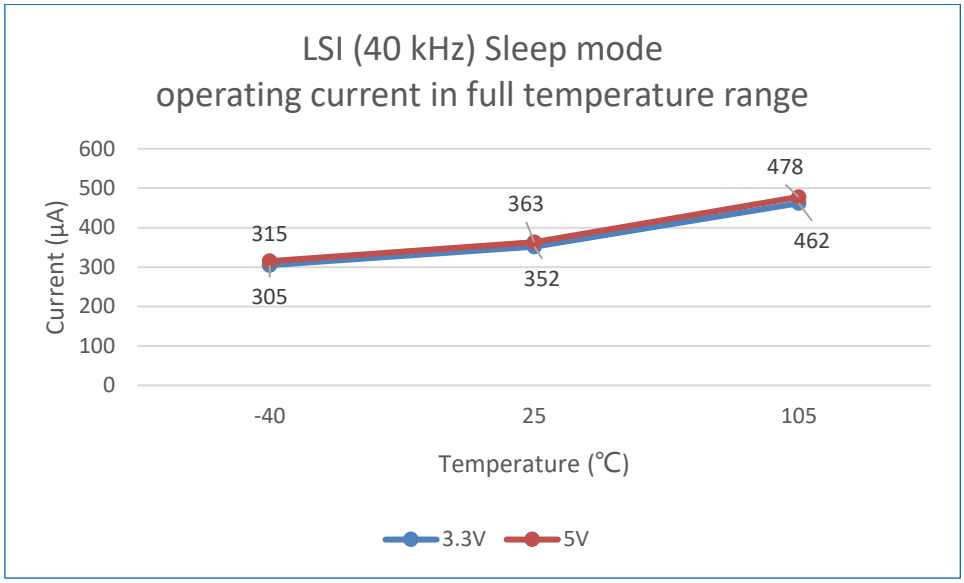

Figure 4-8 LSI (40 kHz) Sleep mode operating current in full temperature range

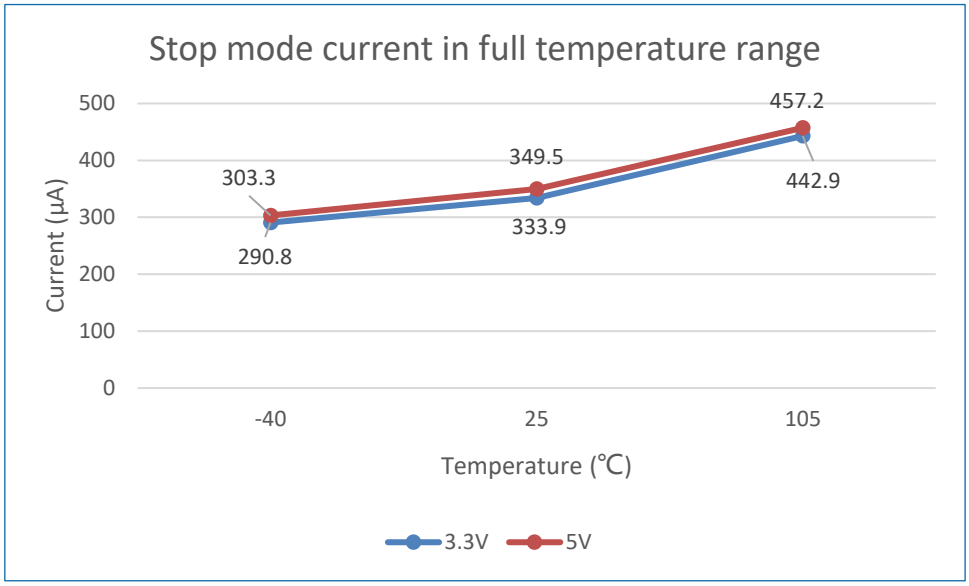

Figure 4-9 Stop mode current in full temperature range

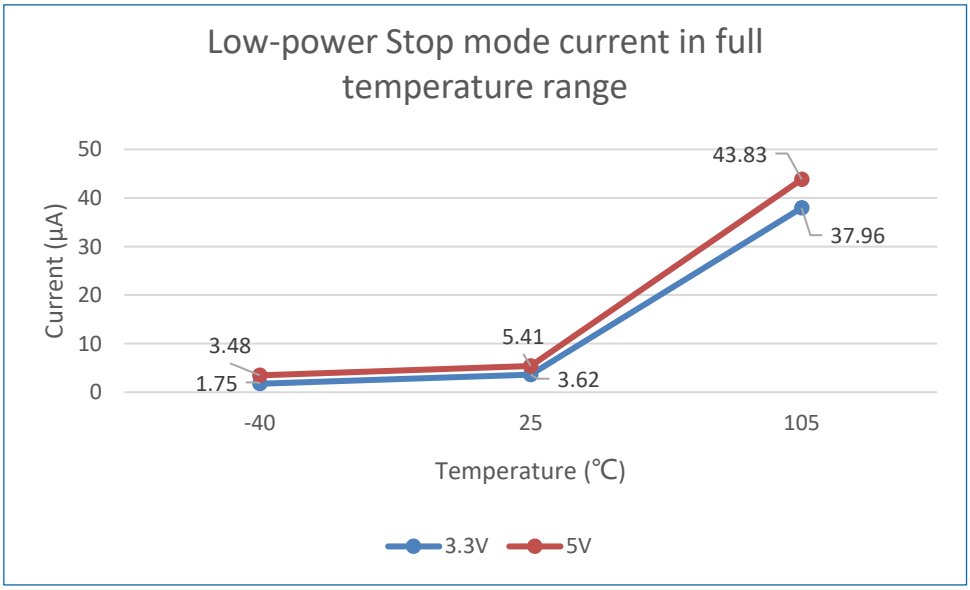

Figure 4-10 Low-power Stop mode current in full temperature range

4.2.6 HSE clock characteristics

Table 4-9 HSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
R_F(1)	Feedback resistor	-	-	370	-	kΩ
$T_{stb\ (HSE)}$(2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	0.2	1.1	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (R_S)		-	12	-	pF
$I_{DD\ (HSE)}$(1)	HSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12 pF	-	400	-	μA

(1). The value is guaranteed in design.

(2). $T_{stb\ (HSE)}$ refers to the time from HSE startup to the time when it outputs stable frequency signals.

HK32D010 integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

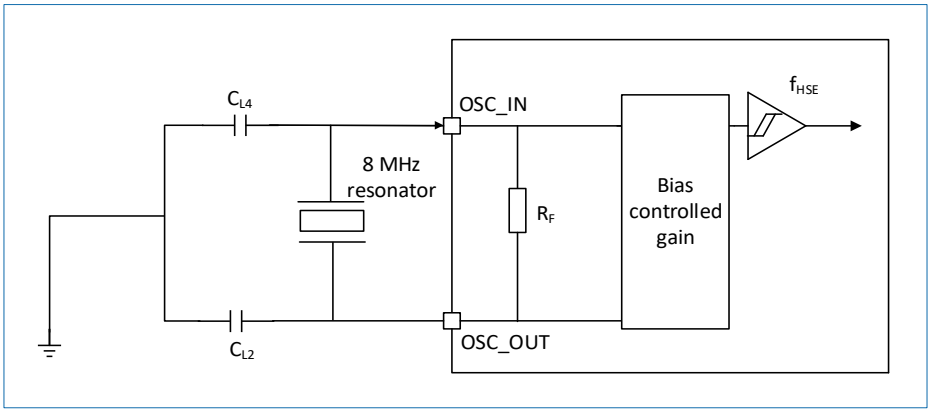

Figure 4-11 HSE negative feedback circuit

Alternatively, an HSE signal can be directly input from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-10 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	4	-	32	MHz
DuCy $_{(HSE)}$(1)	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.7 LSE clock characteristics

Table 4-11 LSE clock characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F(1)	Feedback resistor	-	-	10	-	MΩ
$T_{stb\ (LSE)}$(2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	1000	-	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12	-	pF
$I_{DD\ (LSE)}$(1)	LSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12 pF (AGC disabled)	-	700	-	nA

(1). The value is guaranteed in design.

(2). $T_{stb\ (LSE)}$ refers to the time from LSE startup to the time when it outputs stable frequency signals.

HK32D010 integrates an LSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

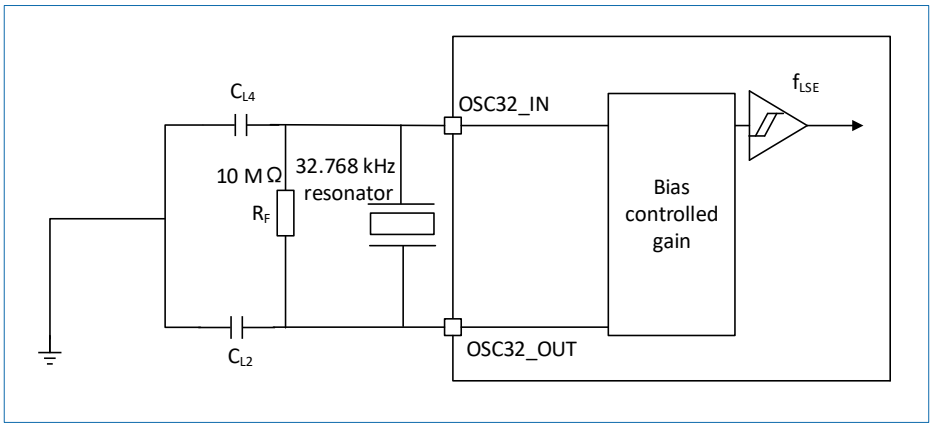

Figure 4-12 LSE negative feedback circuit

Alternatively, an LSE signal can be directly input from the OSC32_IN pin. The following table lists the requirements for this clock signal:

Table 4-12 Characteristics of the input LSE clock (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	-	32.768	-	kHz
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.8 HSI clock characteristics

Table 4-13 HSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	32	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-	45	-	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	–1	-	1	%
		Factory calibration: T_A = –40°C to +105°C	–0.5	-	2.6	
$T_{stb\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	7	9	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	32 MHz, V_{DD} = 3.3 V	-	48	60	µA

(1). The value is guaranteed in design.

4.2.9 LSI clock characteristics

Table 4-14 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	40	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	20	60	µs
$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	200	-	nA

(1). The value is guaranteed in design.

4.2.10 Flash memory characteristics

Table 4-15 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-word programming time	244		404	µs
T_{ERASE}	Page erase time	100		200	ms
	Mass erase time	100		200	ms
I_{DDPROG}	One-word	-	-	8	mA

Symbol	Parameter	Min	Typ	Max	Unit
	programming current				
$I_{DDERASE}$	Page/Mass erase current	-	-	9	mA
I_{DDREAD}	Read current@25 MHz	-		3	mA
N_{END}	Erasure endurance	10	-	-	Thousand cycles
t_{RET}	Data retention	10	-	-	Years

4.2.11 I/O pin input characteristics

Table 4-16 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	0.65 × V_{DD}	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	0.65 × V_{DD}	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V; 0 < V_{IN} < 3.3 V	-	5	-	nA
		V_{DD} = 3.3 V; V_{IN} = 5 V	-	5	-	nA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	33	-	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The value is guaranteed in design.

4.2.12 I/O pin output characteristics

Table 4-17 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	2.6 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}	-	-	V
V_{OL}	Output low level voltage	2.6 V ≤ V_{DD} ≤ 5.5 V	-	-	0.2 × V_{DD}	V

Table 4-18 I/O pin output current characteristics

Symbol	Parameter	Condition (V_{DD} = 5 V)	Min	Typ	Max	Unit
I_{OH}	Normal I/O sourced current when high level voltage is output	0.8 × V_{DD}; OSPEEDy[1:0] = 00	-	6.8	-	mA
		0.8 × V_{DD}; OSPEEDy[1:0] = 01	-	13.3	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 10	-	31.8	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 11	-	49.1	-	
I_{OL}	Normal I/O sunk current when low level voltage is output	0.2 × V_{DD}; OSPEEDy[1:0] = 00	-	17.3	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 01	-	34.8	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 10	-	67.2	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 11	-	110.7	-	
I_{OH_com}	High-current I/O sourced current (PB0–7) when high level voltage is output	0.8 × V_{DD}; OSPEEDy[1:0] = 00	-	6.7	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 01	-	13.1	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 10	-	31.2	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 11	-	47.7	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 00; (UHDRy = 1)	-	38.7	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 01; (UHDRy = 1)	-	42.1	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 10; (UHDRy = 1)	-	59.1	-	
		0.8 × V_{DD}; OSPEEDy[1:0] = 11; (UHDRy = 1)	-	74.1	-	
I_{OL_com}	High-current I/O sunk current (PB0–7) when low level voltage is output	0.2 × V_{DD}; OSPEEDy[1:0] = 00	-	17.7	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 01	-	35.1	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 10	-	68.3	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 11	-	113.8	-	
		0.2 × V_{DD};	-	142	-	

Symbol	Parameter	Condition (V_{DD} = 5 V)	Min	Typ	Max	Unit
		OSPEEDy[1:0] = 00; (UHDRy = 1)				
		0.2 × V_{DD}; OSPEEDy[1:0] = 01; (UHDRy = 1)	-	159.2	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 10; (UHDRy = 1)	-	185.4	-	
		0.2 × V_{DD}; OSPEEDy[1:0] = 11; (UHDRy = 1)	-	225.4	-	

4.2.13 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-19 NRST pin input characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{Noise}	Low level ignored duration	-	-	195	ns

4.2.14 TIM timer characteristics

Table 4-20 TIM characteristics (1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	32	$f_{TIMxCLK}/2$	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 32 MHz.

4.2.15 ADC characteristics

Table 4-21 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage when ADC is enabled	-	2.6	5	5.5	V
VREFP	Positive reference voltage	-	2.6	5	5.5	V
VREFN	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	-	14	MHz
f_S (1)	Sampling frequency	f_{ADC} = 14 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	VREFN	-	VREFP	V
R_{AIN} (1)	External input impedance	For details, see Table 4-22.				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(1)	Sample and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S(1)	Sampling time	f_{ADC} = 14 MHz	1.5	55.5	239.5	Cycles
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz 12-bit resolution	14	68	252	Cycles

(1). The value is guaranteed in design.

(2). The value is measured based on the ADC clock. The register access latency is not taken into account.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f_{ADC}} \times \boldsymbol{C_{ADC}} \times \ln(2^{N+2})} - \boldsymbol{R_{ADC}}$$

The value of N (resolution) is 12. The unit of f_{ADC} is Hz. The unit of C_{ADC} is F. The unit of R_{ADC} is Ω.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-22 Maximum input impedance values (f_{ADC} = 14 MHz)

Sampling Cycles Ts (Cycles)	Sampling Time tS (μs)	Maximum Input Impedance (kΩ)
1.5	0.11	1.21
7.5	0.54	10.05
13.5	0.96	18.88
28.5	2.04	40.97
41.5	2.96	60.12
55.5	3.96	80.74
71.5	5.11	104.30
239.5	17.11	351.72

Table 4-23 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	V_{DD} = V_{REFP} = 5 V, f_{ADC} = 14 MHz	-	2	LSB
EO	Offset error(2)		-	1	
EG	Gain error(3)		-	1	
ED	Differential linearity error(4)		-	1	
EL	Integral linearity error(5)		-	2	

(1) Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2) Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3) Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4) Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5) Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With the restricted V_{DDA}, frequency, and temperature range, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

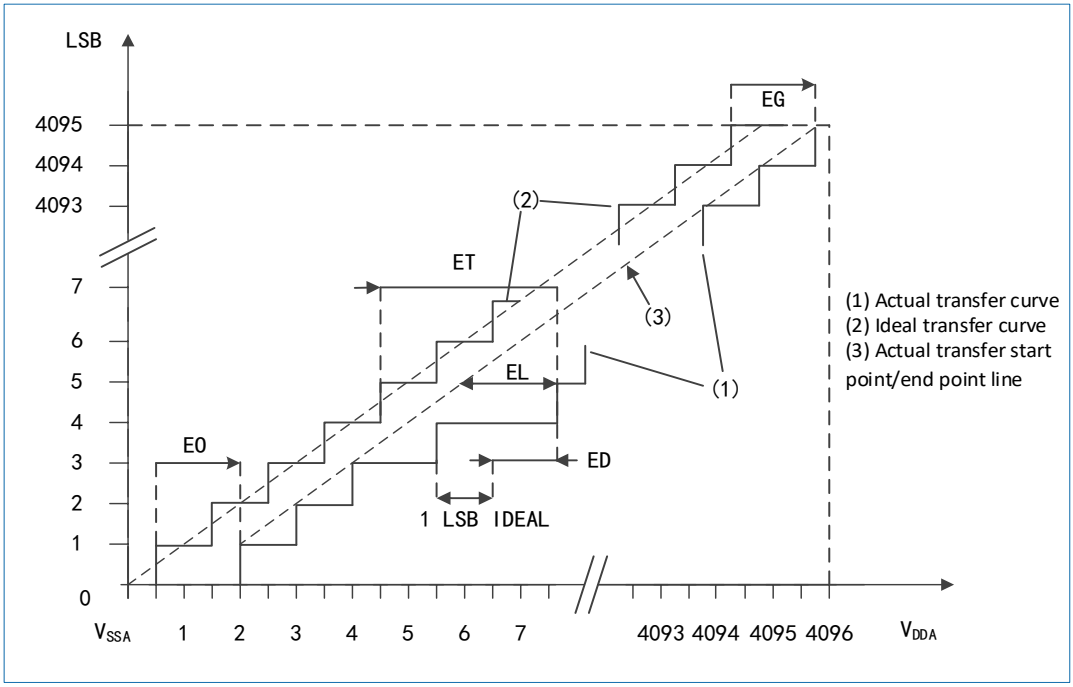

Figure 4-13 ADC accuracy characteristics

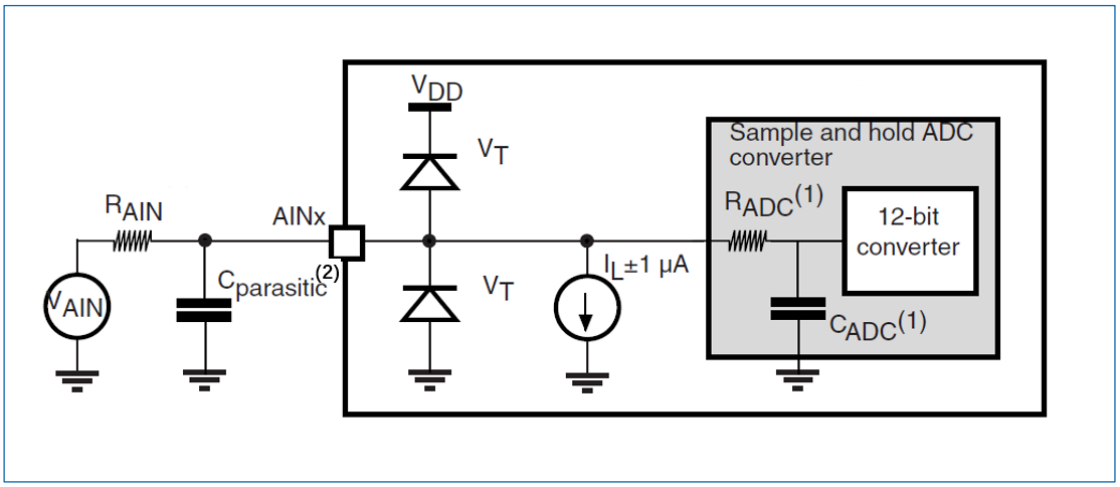

Figure 4-14 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-21.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

4.2.16 Voltage comparator (COMP) characteristics

Table 4-24 COMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Analog power supply voltage	-	2	5	5.5	V
V_{com}	Input common mode voltage	-	0.2	$V_{DD}/2$	$V_{DD} – 0.2$	V
V_{diff}	Input differential mode voltage	V_{DDA} = 5 V, V_{com} = 0 to V_{DD}, high power consumption	-	-	10.5	mV
	Input differential mode voltage	V_{DDA} = 5 V, V_{com} = 0 to V_{DD}, low power consumption	-	-	40	
V_{hy}	Hysteresis voltage	Level 1	-	6	-	mV
		Level 2	-	2	-	
		Level 3	-	9	-	
		Level 4	-	25	-	
I_{OP}	Operating current (V_{DD} = 5 V)	Low-power modes	-	39.7	-	µA
		High-power mode	-	4.1	-	
T_{dly}(1)	Output delay (no hysteresis)	High-power mode Rising edge	-	30	-	ns
		Low-power modes Rising edge	-	840	-	
		High-power mode Falling edge	-	41.2	-	
		Low-power modes Falling edge	-	524	-	

(1). The value is guaranteed in design.

4.2.17 LCD characteristics

Table 4-25 LCD controller characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{LCD}(1)	LCD supply voltage	-	2.6	-	5.5	V
$V_{contrast}$	$V_{contrast0}$	-	-	$(0.5 + 1 \times 0.0625) \times V_{LCD}$	-	V
	$V_{contrast1}$		-	$(0.5 + 2 \times 0.0625) \times V_{LCD}$	-	
	$V_{contrast2}$		-	$(0.5 + 3 \times 0.0625) \times V_{LCD}$	-	
	$V_{contrast3}$		-	$(0.5 + 4 \times 0.0625) \times V_{LCD}$	-	

Item	Description	Condition	Min	Typ	Max	Unit
	$V_{contrast4}$		-	$(0.5 + 5 \times 0.0625) \times V_{LCD}$	-	
	$V_{contrast5}$		-	$(0.5 + 6 \times 0.0625) \times V_{LCD}$	-	
	$V_{contrast6}$		-	$(0.5 + 7 \times 0.0625) \times V_{LCD}$	-	
	$V_{contrast7}$		-	$(0.5 + 8 \times 0.0625) \times V_{LCD}$	-	
RES	LCDRV drive equivalent resistor	Target = 56.25 kΩ	21	42	55	kΩ
		Target = 225 kΩ	84	153	220	
		Target = 900 kΩ	337	600	881	
I_{LCD}	Operating power consumption	-	8	32	121	μA
TEMP	Temperature range	-	0	25	85	°C

(1). $V_{LCD} = V_{DD}$.

5 Typical circuitry

5.1 Power supply scheme

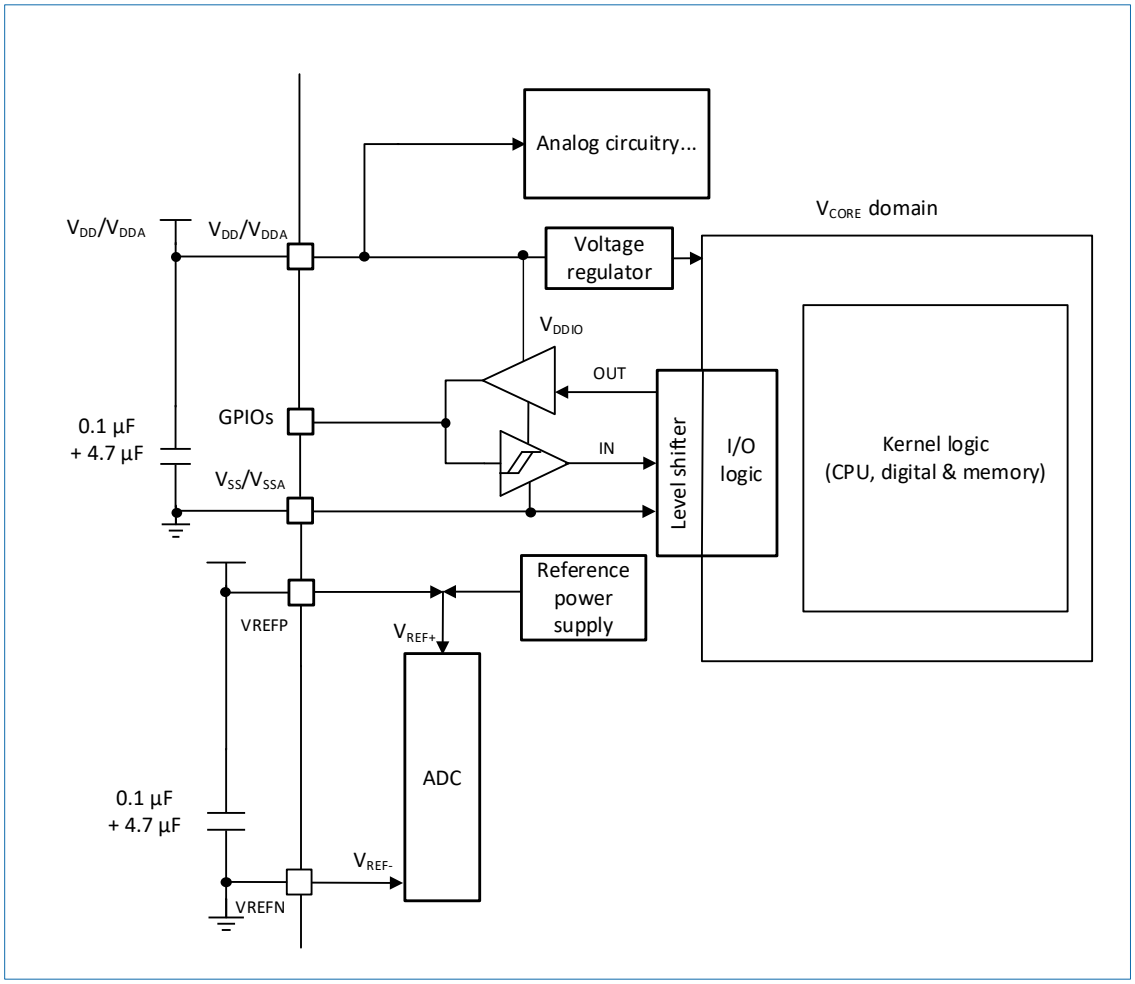

Figure 5-1 Power supply reference circuitry

6 Pinouts and pin descriptions

HK32D010 MCUs are delivered in LQFP32, LQFP44, and LQFP48 packages. This chapter describes the pinout and pin description of each package.

6.1 LQFP32

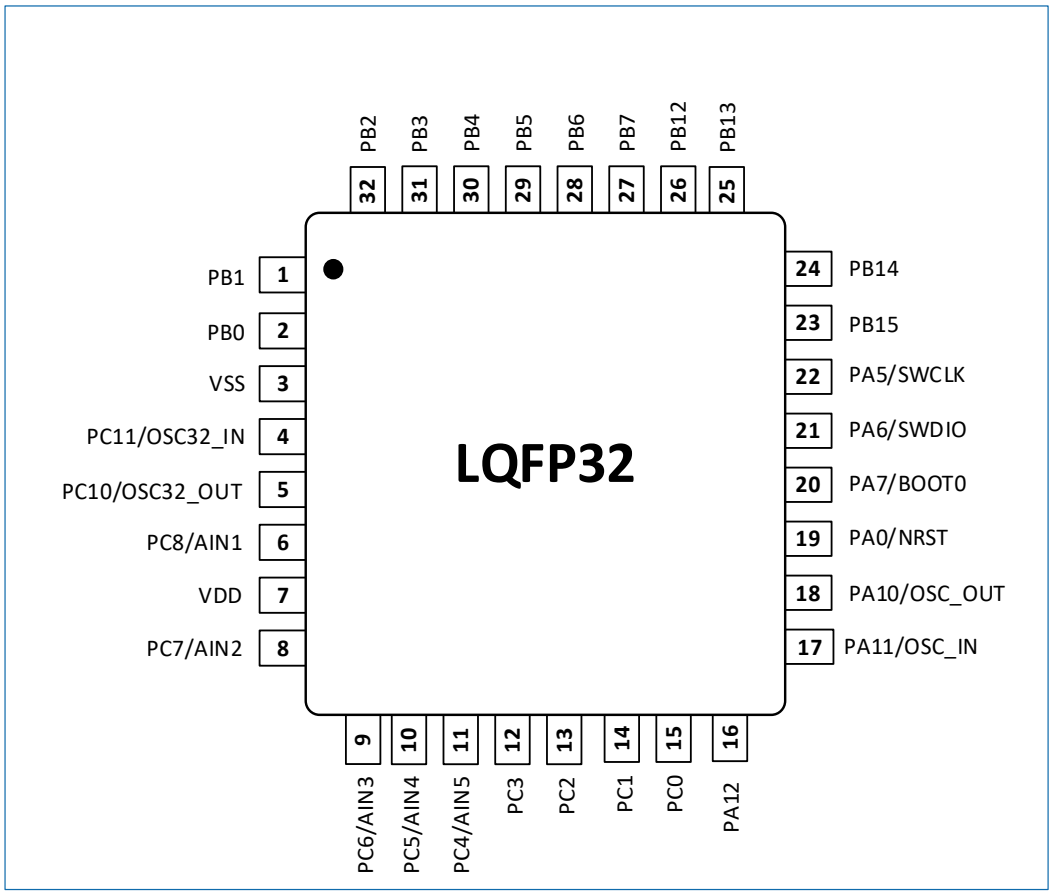

Figure 6-1 LQFP32 package pinout

6.2 LQFP44

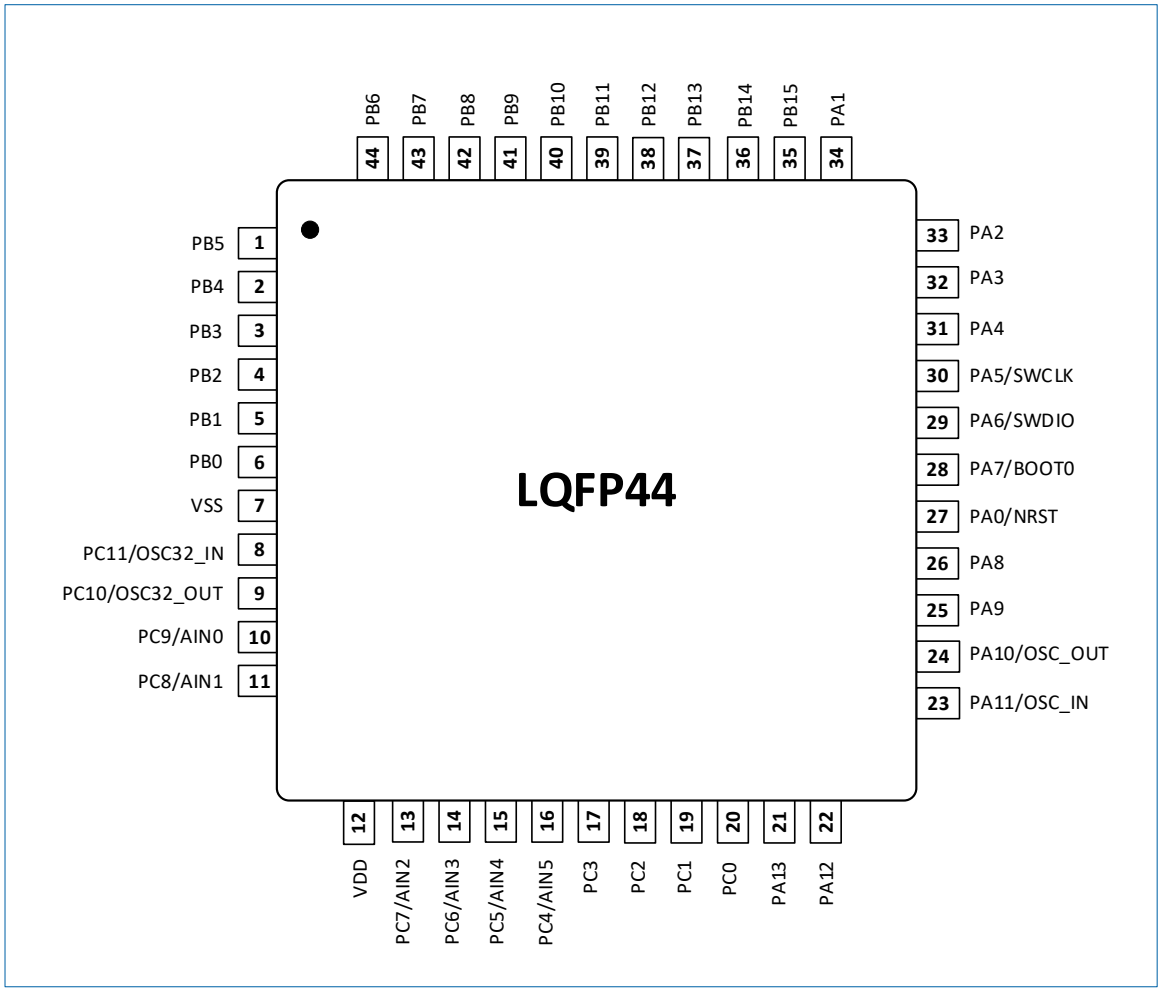

Figure 6-2 LQFP44 package pinout

6.3 LQFP48

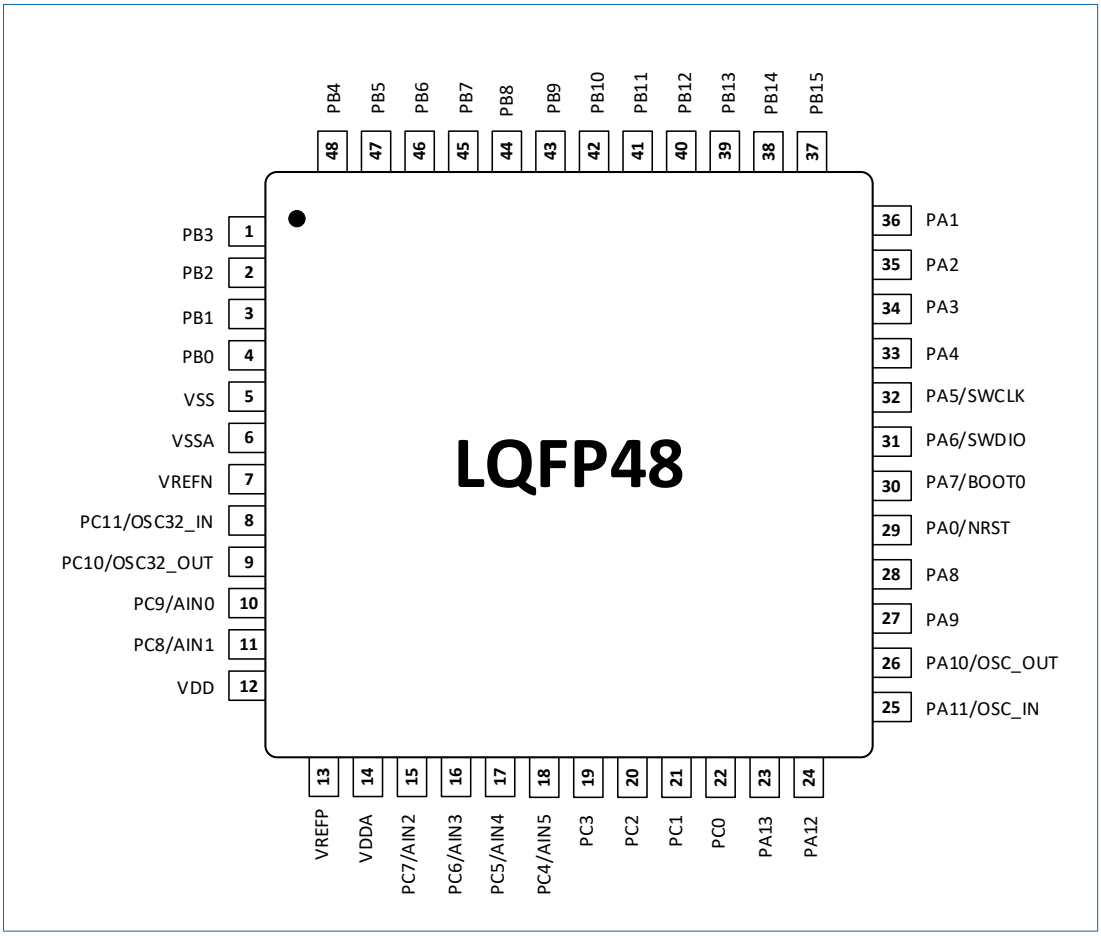

Figure 6-3 LQFP48 package pinout

6.4 Pin descriptions

Table 6-1 Pin description of each package

LQFP32	LQFP44	LQFP48	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
31	3	1	PB3	I/O	Yes	UART2_TX(2) UART4_RX(2) LED3/COML3	LCD_COM3 EXTI3
32	4	2	PB2	I/O	Yes	UART1_TX(2) UART2_RX(2) LED2/COML2	LCD_COM2 EXTI2
1	5	3	PB1	I/O	Yes	UART1_RX(2) UART3_TX(2) LED1/COML1	LCD_COM1 EXTI1
2	6	4	PB0	I/O	Yes	UART3_RX(2) UART6_TX(2) LED0/COML0	LCD_COM0 EXTI0
3	7	5	VSS	S	Digital power supply ground		
-	-	6	VSSA	S	Analog power supply		
-	-	7	VREFN	S	Reference power supply ground		
4	8	8	PC11	I/O	Yes	TIM3_ETR TIM15_BKIN UART5_TX(2) UART6_RX(2) LED_SEGL3 CM0_TXEV	OSC32_IN EXTI11
5	9	9	PC10	I/O	Yes	ADC_ETR TIM3_CH3	OSC32_OUT EXTI10

LQFP32	LQFP44	LQFP48	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
						I2C1_SMBA UART5_RX(2) UART6_TX(2) LED_SEGL2 CM0_TXEV	
-	10	10	PC9	I/O	Yes	SPI1_NSS(4) TIM3_CH2 TIM15_BKIN I2C1_SDA(3) UART3_RX(2) UART4_TX(2) LED_SEGL1 BEEPO	AIN0 EXTI9
6	11	11	PC8	I/O	Yes	SPI1_SCK(4) TIM3_CH1 TIM15_CH1 I2C1_SCL(3) UART3_TX(2) UART4_RX(2) LED_SEGL0 VCOM_O	AIN1 EXTI8
7	12	12	VDD	S	Digital power supply		
-	-	13	VREFP	S	Reference power supply		
-	-	14	VDDA	S	Analog power supply		
8	13	15	PC7	I/O	Yes	TIM3_CH4 TIM15_CH2 UART4_TX(2) UART5_RX(2) LED_SEGL7 CM0_TXEV	AIN2 EXTI7
9	14	16	PC6	I/O	Yes	TIM15_CH1N SPI1_MOSI UART3_TX(2) UART4_RX(2) LED_SEGL6	RCC_CKI1 AIN3 EXTI6
10	15	17	PC5	I/O	Yes	TIM15_BKIN SPI1_MISO I2C1_SMBA UART2_TX(2) UART3_RX(2) LED_SEGL5 CM0_TXEV	AIN4 EXTI5
11	16	18	PC4	I/O	Yes	TIM3_CH4 TIM15_CH1 UART2_RX(2) UART6_TX(2) LED_SEGL4	RCC_CKI0 AIN5 EXTI4
12	17	19	PC3	I/O	Yes	SPI1_NSS(4) TIM3_CH3 TIM15_CH2 I2C1_SDA(3) UART2_TX(2) UART3_RX(2) LED_SEGL3 RCC_MCO	LCD_SEG23 EXTI3
13	18	20	PC2	I/O	Yes	TIM15_BKIN SPI1_MOSI UART1_TX(2) UART2_RX(2) LED_SEGL2 CM0_TXEV	EXTI2
14	19	21	PC1	I/O	Yes	TIM15_CH1N SPI1_MISO	LCD_SEG15 EXTI1

LQFP32	LQFP44	LQFP48	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
						I2C1_SMBA UART1_RX(2) UART6_TX(2) LED_SEGL1 CM0_TXEV	
15	20	22	PC0	I/O	Yes	ADC_ETR SPI1_SCK(4) TIM3_CH2 I2C1_SCL(3) UART5_TX(2) UART6_RX(2) LED_SEGL0 BEEPO	LCD_SEG14 EXTI0
-	21	23	PA13	I/O	Yes	SPI1_NSS TIM3_CH1 TIM15_CH1N I2C1_SDA(3) UART3_TX(2) UART4_RX(2) LED_SEGL7 VCOM_O	LCD_SEG13 EXTI13
16	22	24	PA12	I/O	Yes	ADC_ETR SPI1_MISO TIM3_CH4 I2C1_SCL(3) UART4_TX(2) UART5_RX(2) LED_SEGL6 BEEPO	LCD_SEG12 EXTI12
17	23	25	PA11	I/O	Yes	SPI1_MOSI TIM3_ETR TIM15_CH1N I2C1_SMBA UART5_TX(2) UART6_RX(2) LED_SEGL7	RCC_CKI3 OSC_IN LCD_SEG11 EXTI11
18	24	26	PA10	I/O	Yes	ADC_ETR SPI1_SCK(4) TIM3_ETR I2C1_SMBA UART2_TX(2) UART5_RX(2) LED_SEGL6 CM0_TXEV	OSC_OUT LCD_SEG10 EXTI10
-	25	27	PA9	I/O	Yes	TIM15_CH1 SPI1_MOSI TIM3_CH3 I2C1_SCL(3) UART2_RX(2) UART1_TX(2) LED_SEGL5 RCC_MCO	LCD_SEG9 EXTI9
-	26	28	PA8	I/O	Yes	SPI1_MISO TIM3_CH2 TIM15_CH2 I2C1_SDA(3) UART1_RX(2) UART2_TX(2) LED_SEGL4 BEEPO	LCD_SEG8 EXTI8
19	27	29	PA0	I/O	Yes	SPI1_SCK(4) UART1_TX(2) UART2_RX(2)	NRST EXTI0

LQFP32	LQFP44	LQFP48	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
						LED_SEGL7	
20	28	30	PA7	I/O	Yes	ADC_ETR SPI1_MOSI UART1_RX(2) UART6_TX(2) LED_SEGL6	BOOT0 LCD_SEG22 EXTI7
21	29	31	PA6	I/O	Yes	SWDIO SPI1_MISO TIM3_ETR I2C1_SDA(3) UART1_TX(2) UART6_RX(2) LED_SEGL5 RCC_MCO	LCD_SEG21 EXTI6
-	30	32	PA5	I/O	Yes	SWCLK SPI1_SCK(4) TIM3_CH1 I2C1_SCL(3) UART1_RX(2) UART5_TX(2) LED_SEGL4 VCOM_O	LCD_SEG20 EXTI5
-	31	33	PA4	I/O	Yes	SPI1_NSS(4) TIM3_CH4 TIM15_CH1N I2C1_SDA(3) UART5_TX(2) UART6_RX(2) LED_SEGL3 BEEPO	LCD_SEG19 EXTI4
-	32	34	PA3	I/O	Yes	SPI1_MOSI TIM3_CH3 TIM15_BKIN I2C1_SCL(3) UART4_TX(2) UART5_RX(2) LED_SEGL2 RCC_MCO	LCD_SEG18 EXTI3
-	33	35	PA2	I/O	Yes	SPI1_MISO TIM3_CH2 TIM15_CH1 I2C1_SCL(3) UART3_TX(2) UART4_RX(2) LED_SEGL1 VCOM_O	LCD_SEG17 EXTI2
-	34	36	PA1	I/O	Yes	SPI1_SCK(4) TIM3_CH1 TIM15_CH2 I2C1_SDA(3) UART2_TX(2) UART3_RX(2) LED_SEGL0 BEEPO	LCD_SEG16 EXTI1
23	35	37	PB15	I/O	Yes	SPI1_NSS(4) TIM3_CH4 TIM15_CH1 I2C1_SCL(3) UART2_TX(2) UART4_RX(2) LED_SEGL7 RCC_MCO	LCD_SEG7 VCOMN EXTI15
24	36	38	PB14	I/O	Yes	SPI1_SCK(4)	LCD_SEG6

LQFP32	LQFP44	LQFP48	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
						TIM3_CH3 TIM15_CH2 I2C1_SDA(3) UART2_RX(2) UART3_TX(2) LED_SEGL6 BEEPO	VCOMP EXTI14
25	37	39	PB13	I/O	Yes	SPI1_MISO TIM3_CH2 TIM15_CH1N I2C1_SDA(3) UART1_TX(2) UART3_RX(2) LED_SEGL5 VCOM_O	LCD_SEG5 EXTI13
26	38	40	PB12	I/O	Yes	SPI1_MOSI TIM3_CH1 TIM15_BKIN I2C1_SCL(3) UART1_RX(2) UART4_TX(2) LED_SEGL4 VCOM_O	LCD_SEG4 EXTI12
-	39	41	PB11	I/O	Yes	TIM15_CH1N SPI1_SCK(4) TIM3_CH4 I2C1_SCL(3) UART2_RX(2) UART1_TX(2) LED_SEGL3 BEEPO	LCD_SEG3 EXTI11
-	40	42	PB10	I/O	Yes	SPI1_NSS(4) TIM3_CH3 TIM15_CH2 I2C1_SDA(3) UART3_TX(2) UART4_RX(2) LED_SEGL2 RCC_MCO	LCD_SEG2 EXTI10
-	41	43	PB9	I/O	Yes	TIM15_CH1 SPI1_MOSI TIM3_CH1 I2C1_SCL(3) UART3_RX(2) UART4_TX(2) LED_SEGL1 VCOM_O	LCD_SEG1 EXTI9
-	42	44	PB8	I/O	Yes	SPI1_MISO TIM3_CH2 TIM15_BKIN I2C1_SDA(3) UART1_RX(2) UART6_TX(2) LED_SEGL0 RCC_MCO	LCD_SEG0 EXTI8
27	43	45	PB7	I/O	Yes	ADC_ETR TIM3_CH4 UART6_RX(2) UART5_TX(2) LED7/COML7	RCC_CKI2 LCD_COM7 EXTI7
28	44	46	PB6	I/O	Yes	TIM3_CH3 TIM15_CH1 UART5_RX(2)	LCD_COM6 EXTI6

LQFP32	LQFP44	LQFP48	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
						UART6_TX(2) LED6/COML6 CM0_TXEV	
29	1	47	PB5	I/O	Yes	ADC_ETR TIM3_CH2 UART5_TX(2) UART6_RX(2) LED5/COML5	LCD_COM5 EXTI5
30	2	48	PB4	I/O	Yes	TIM3_CH1 TIM15_CH2 UART4_TX(2) UART5_RX(2) LED4/COML4	LCD_COM4 EXTI4

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). From UART1 to UART6, the RX and TX pins can be exchanged by setting the UART_CR2.SWAP bit.

(3). The SDA and SCL pins can be exchanged by setting the I2C_CR1.SWAP bit.

(4). The NSS and SCK pins can be exchanged by setting the SPI_PLUS.SWAPNS bit.

Note: Unless otherwise specified, all I/Os are configured in analog mode during and after resets by default.

6.5 Alternate function table

Table 6-2 Alternate function table

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	ADC_ETR	SPI1_SCK	TIM3_CH2	I2C1_SCL	UART6_RX	UART5_TX	LED_SEGL0	BEEPO
PC1	TIM15_CH1N	SPI1_MISO	-	I2C1_SMBA	UART1_RX	UART6_TX	LED_SEGL1	CM0_TXEV
PC2	TIM15_BKIN	SPI1_MOSI	-	-	UART2_RX	UART1_TX	LED_SEGL2	CM0_TXEV
PC3	TIM15_CH2	SPI1_NSS	TIM3_CH3	I2C1_SDA	UART3_RX	UART2_TX	LED_SEGL3	RCC_MCO
PC4	TIM15_CH1	-	TIM3_CH4	-	UART2_RX	UART6_TX	LED_SEGL4	-
PC5	TIM15_BKIN	SPI1_MISO	-	I2C1_SMBA	UART3_RX	UART2_TX	LED_SEGL5	CM0_TXEV
PC6	TIM15_CH1N	SPI1_MOSI	-	-	UART4_RX	UART3_TX	LED_SEGL6	-
PC7	TIM15_CH2	-	TIM3_CH4	-	UART5_RX	UART4_TX	LED_SEGL7	CM0_TXEV
PC8	TIM15_CH1	SPI1_SCK	TIM3_CH1	I2C1_SCL	UART4_RX	UART3_TX	LED_SEGL0	VCOM_O
PC9	TIM15_BKIN	SPI1_NSS	TIM3_CH2	I2C1_SDA	UART3_RX	UART4_TX	LED_SEGL1	BEEPO
PC10	ADC_ETR	-	TIM3_CH3	I2C1_SMBA	UART5_RX	UART6_TX	LED_SEGL2	CM0_TXEV
PC11	TIM15_BKIN	-	TIM3_ETR	-	UART6_RX	UART5_TX	LED_SEGL3	CM0_TXEV
PB0	-	-	-	-	UART3_RX	UART6_TX	LED0/COML0	-
PB1	-	-	-	-	UART1_RX	UART3_TX	LED1/COML1	-
PB2	-	-	-	-	UART2_RX	UART1_TX	LED2/COML2	-
PB3	-	-	-	-	UART4_RX	UART2_TX	LED3/COML3	-
PB4	TIM15_CH2	-	TIM3_CH1	-	UART5_RX	UART4_TX	LED4/COML4	-
PB5	ADC_ETR	-	TIM3_CH2	-	UART6_RX	UART5_TX	LED5/COML5	-
PB6	TIM15_CH1	-	TIM3_CH3	-	UART5_RX	UART6_TX	LED6/COML6	CM0_TXEV
PB7	ADC_ETR	-	TIM3_CH4	-	UART6_RX	UART5_TX	LED7/COML7	-
PB8	TIM15_BKIN	SPI1_MISO	TIM3_CH2	I2C1_SDA	UART1_RX	UART6_TX	LED_SEGL0	RCC_MCO
PB9	TIM15_CH1	SPI1_MOSI	TIM3_CH1	I2C1_SCL	UART3_RX	UART4_TX	LED_SEGL1	VCOM_O
PB10	TIM15_CH2	SPI1_NSS	TIM3_CH3	I2C1_SDA	UART4_RX	UART3_TX	LED_SEGL2	RCC_MCO
PB11	TIM15_CH1N	SPI1_SCK	TIM3_CH4	I2C1_SCL	UART2_RX	UART1_TX	LED_SEGL3	BEEPO
PB12	TIM15_BKIN	SPI1_MOSI	TIM3_CH1	I2C1_SCL	UART1_RX	UART4_TX	LED_SEGL4	VCOM_O
PB13	TIM15_CH1N	SPI1_MISO	TIM3_CH2	I2C1_SDA	UART3_RX	UART1_TX	LED_SEGL5	VCOM_O
PB14	TIM15_CH2	SPI1_SCK	TIM3_CH3	I2C1_SDA	UART2_RX	UART3_TX	LED_SEGL6	BEEPO
PB15	TIM15_CH1	SPI1_NSS	TIM3_CH4	I2C1_SCL	UART4_RX	UART2_TX	LED_SEGL7	RCC_MCO
PA0	-	SPI1_NSS	-	-	UART2_RX	UART1_TX	LED_SEGL7	-
PA1	TIM15_CH2	SPI1_SCK	TIM3_CH1	I2C1_SDA	UART3_RX	UART2_TX	LED_SEGL0	BEEPO
PA2	TIM15_CH1	SPI1_MISO	TIM3_CH2	I2C1_SCL	UART4_RX	UART3_TX	LED_SEGL1	VCOM_O
PA3	TIM15_BKIN	SPI1_MOSI	TIM3_CH3	I2C1_SCL	UART5_RX	UART4_TX	LED_SEGL2	RCC_MCO
PA4	TIM15_CH1N	SPI1_NSS	TIM3_CH4	I2C1_SDA	UART6_RX	UART5_TX	LED_SEGL3	BEEPO
PA5	SWCLK	SPI1_SCK	TIM3_CH1	I2C1_SCL	UART1_RX	UART5_TX	LED_SEGL4	VCOM_O
PA6	SWDIO	SPI1_MISO	TIM3_ETR	I2C1_SDA	UART6_RX	UART1_TX	LED_SEGL5	RCC_MCO
PA7	ADC_ETR	SPI1_MOSI	-	-	UART1_RX	UART6_TX	LED_SEGL6	-
PA8	TIM15_CH2	SPI1_MISO	TIM3_CH2	I2C1_SDA	UART1_RX	UART2_TX	LED_SEGL4	BEEPO
PA9	TIM15_CH1	SPI1_MOSI	TIM3_CH3	I2C1_SCL	UART2_RX	UART1_TX	LED_SEGL5	RCC_MCO
PA10	ADC_ETR	SPI1_SCK	TIM3_ETR	I2C1_SMBA	UART5_RX	UART2_TX	LED_SEGL6	CM0_TXEV
PA11	TIM15_CH1N	SPI1_MOSI	TIM3_ETR	I2C1_SMBA	UART6_RX	UART5_TX	LED_SEGL7	-

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA12	ADC_ETR	SPI1_MISO	TIM3_CH4	I2C1_SCL	UART5_RX	UART4_TX	LED_SEGL6	BEEPO
PA13	TIM15_CH1N	SPI1_NSS	TIM3_CH1	I2C1_SDA	UART4_RX	UART3_TX	LED_SEGL7	VCOM_O

7 Packages

7.1 Package outlines

7.1.1 LQFP32

LQFP32 is a 7 mm × 7 mm, 0.8 mm pitch package.

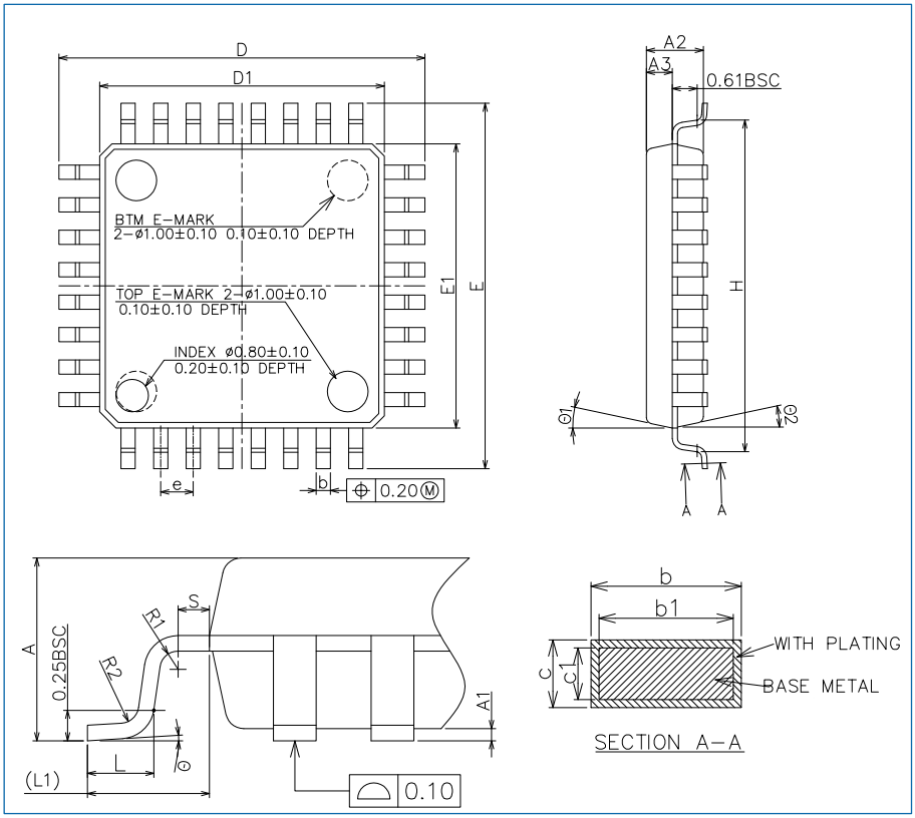

Figure 7-1 LQFP32 package outline

Table 7-1 LQFP32 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches)	Max (inches)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP44

LQFP44 is a 10 mm × 10 mm, 0.8 mm pitch package.

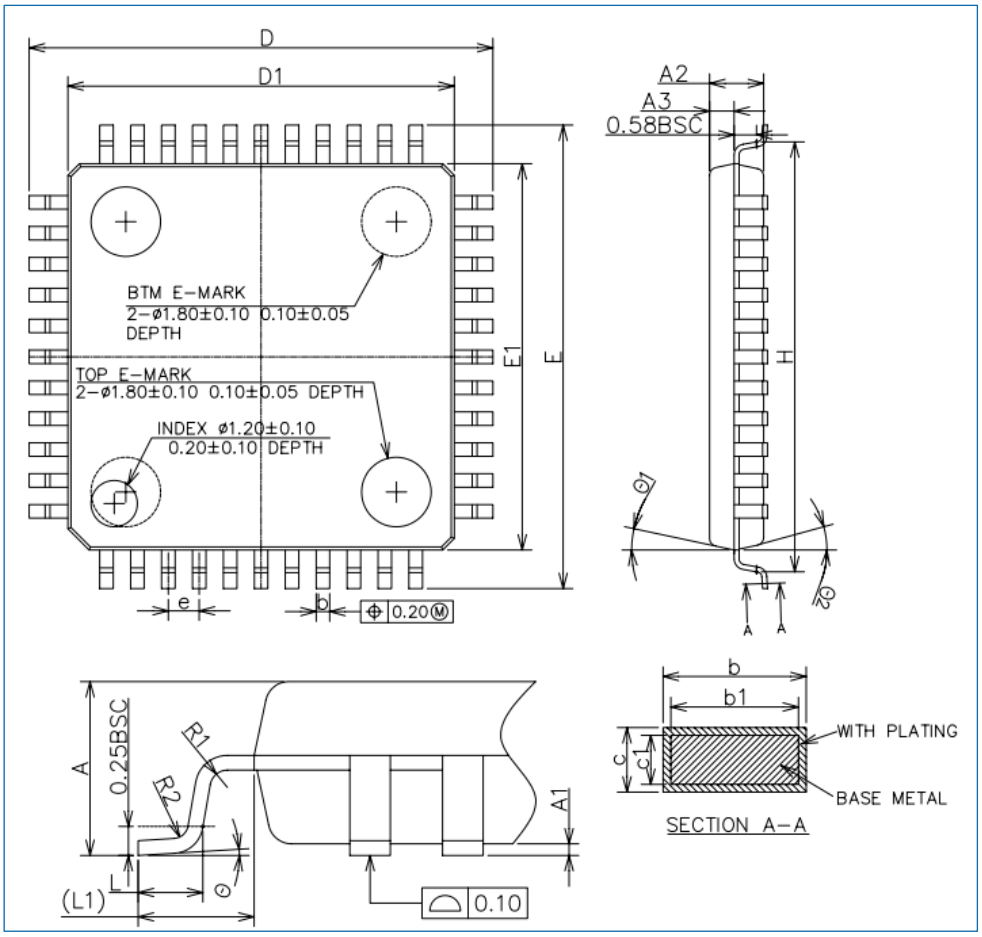

Figure 7-2 LQFP44 package outline

Table 7-2 LQFP44 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches)	Max (inches)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	11.95	12.00	12.05	0.4705	0.4724	0.4744
D1	9.9	10.00	10.10	0.3898	0.3937	0.3976
E	11.95	12.00	12.05	0.4705	0.4724	0.4744
E1	9.90	10.00	10.10	0.3898	0.3937	0.3976
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	11.09	11.13	11.17	0.4366	0.4382	0.4398
L	0.53	-	0.70	0.0209	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	-	0.15	-	-	0.0059	-
R2	-	0.13	-	-	0.0051	-
θ	0°	3.5°	7°	0.0079	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.3 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

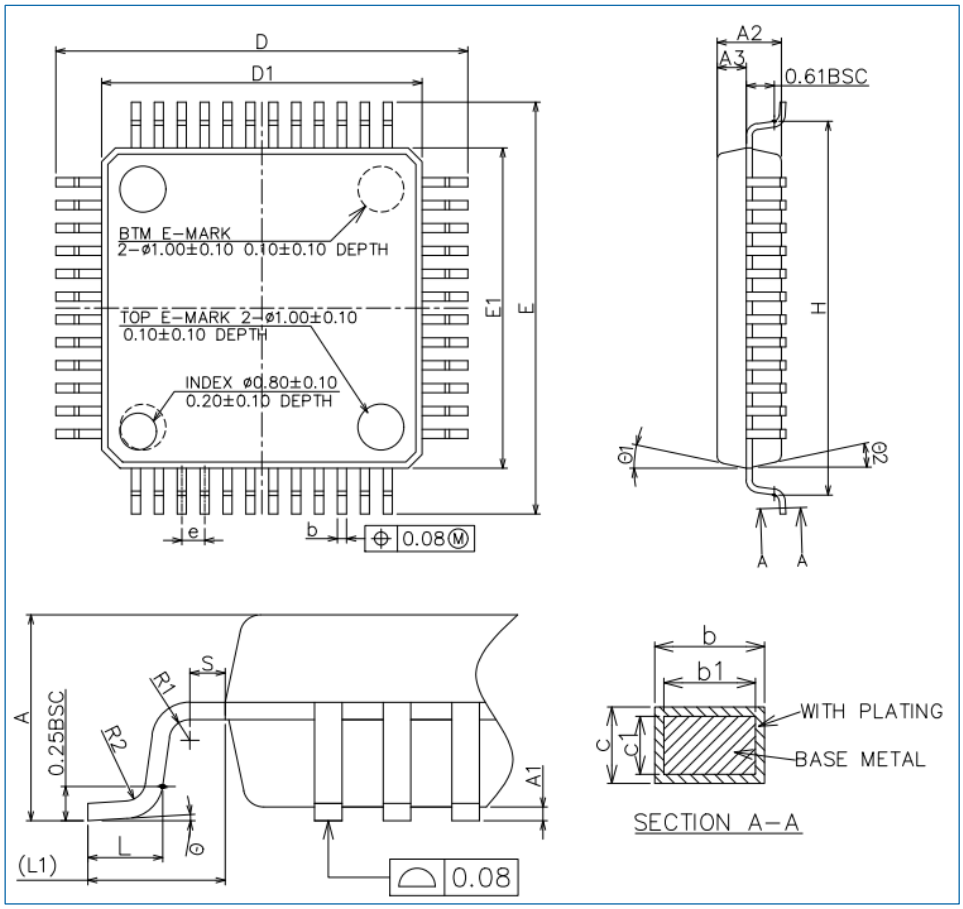

Figure 7-3 LQFP48 package outline

Table 7-3 LQFP48 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches)	Max (inches)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.18	-	0.27	0.0071	-	0.0106
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.40	0.50	0.60	0.0157	0.0197	0.0236
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.2	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-4 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP32 marking

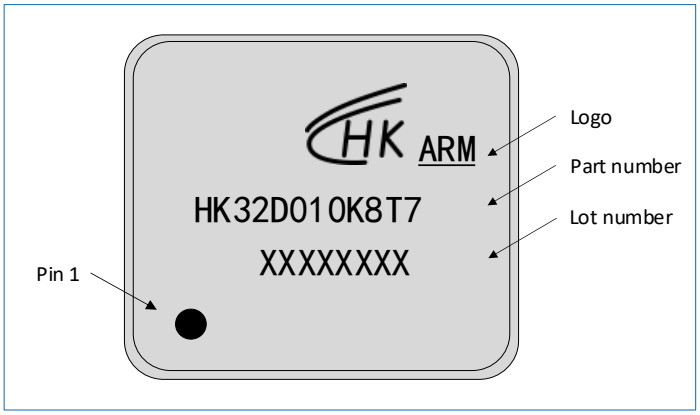

Figure 7-4 LQFP32 HK32D010K8T7 marking example

7.2.2 LQFP44 marking

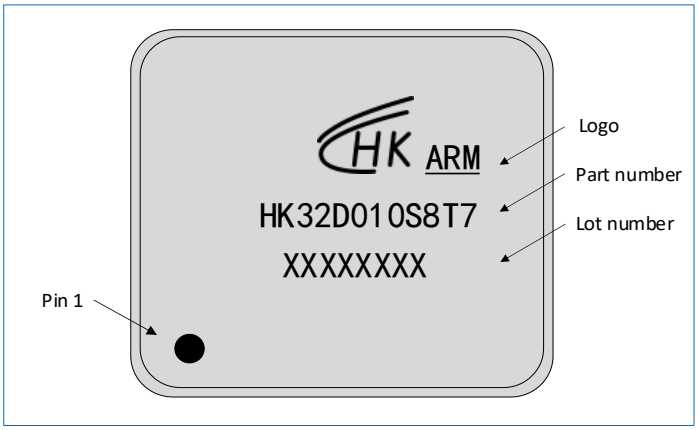

Figure 7-5 LQFP44 HK32D010S8T7 marking example

7.2.3 LQFP48 marking

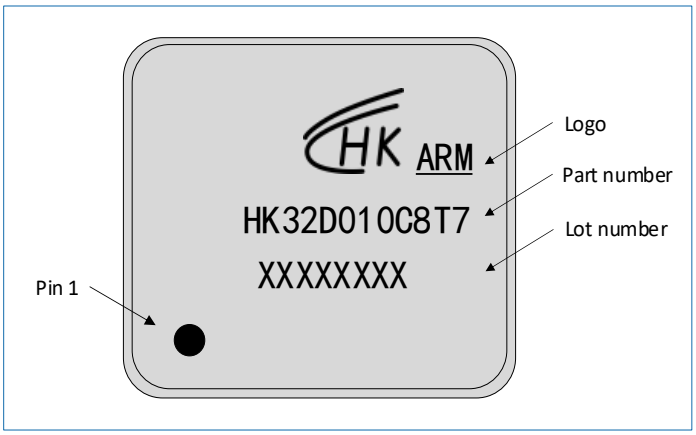

Figure 7-6 QFP48 HK32D010C8T7 marking example

8 Ordering information

8.1 Device numbering conventions

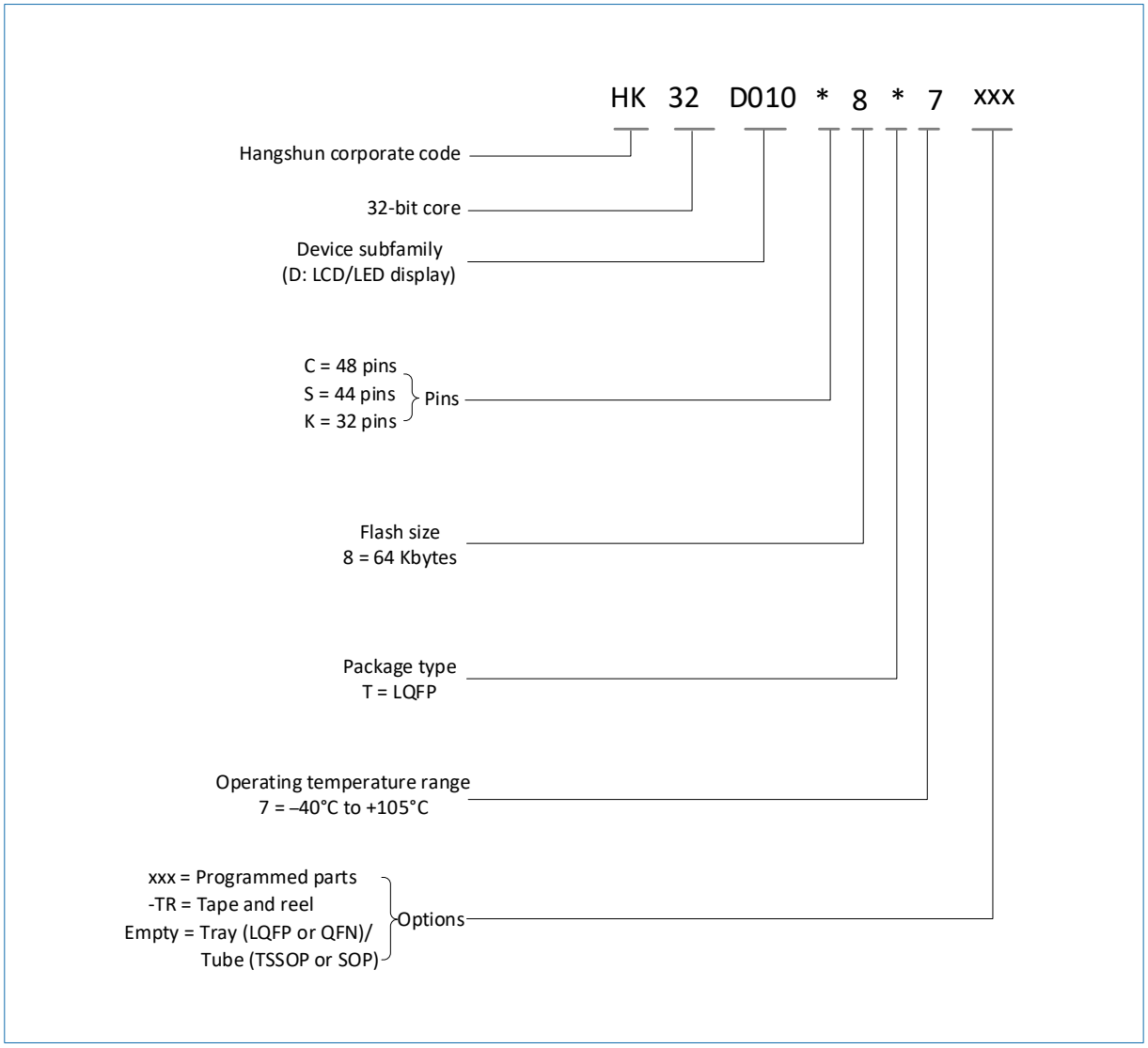

Figure 8-1 Device numbering conventions

8.2 Packaging information

Table 8-1 HK32D010 packaging information

Package	Part Number	Shipping Option	Remarks
LQFP32	HK32D010K8T7	Tray	
LQFP32	HK32D010K8T7-TR	Tape and reel	
LQFP44	HK32D010S8T7	Tray	
LQFP44	HK32D010S8T7-TR	Tape and reel	
LQFP48	HK32D010C8T7	Tray	
LQFP48	HK32D010C8T7-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CLU	Configurable Logic Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EMACC	Electric Motor Acceleration
EXTI	Extended Interrupt/Event Controller
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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