HK32C105 Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32C105 series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32C105.

Audience

This document is intended for:

- HK32C105 developers
- HK32C105 testers
- HK32C105 users

Release Notes

This document is applicable to HK32C105 series MCUs.

Revision History

Version	Date	Description
1.0	2023/07/21	The initial release.
1.1	2023/10/20	1. Updated Figure 3-3 Reset signal in section "3.7.1 System reset". 2. Updated the one-word programming time in Table 4-14 Flash memory characteristics.
1.2	2024/01/22	1. Updated Figure 3-3 Reset signal. 2. Changed the maximum prescaler factor of FLITFCLK from 9 to 16 in Figure 3-4 Clock tree. 3. Added a note for the pull-down resistor of Boot0 in section "6.4 Pin descriptions". 4. Added I2S functions and descriptions of switchable pin functions of UART and I2C in sections "6.4 Pin descriptions" and "6.5 Alternate function table". 5. Updated the figure and parameters in section "7.1.3 QFN32".

Contents

1 Introduction

This document is the datasheet for HK32C105 series MCUs. HK32C105 is a family of cost-effective general-purpose MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32C105S8T7 (LQFP44 package)
- HK32C105K8T7 (LQFP32 package)
- HK32C105K8U7 (QFN32 package)

For more details of HK32C105, see *HK32C105 User Manual*.

2 Product overview

This section describes the features and provides the device overview of HK32C105.

HK32C105 adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 64 MHz. It has a Flash memory of up to 64 Kbytes (including 61 Kbytes of main Flash and three Kbytes for bootloader area) and 10-Kbyte SRAM. You can configure the Flash controller register to remap interrupt vectors in the main Flash.

HK32C105 supports conventional Flash readout protection (RDP) Level 0, Level 1, Level 2.

To meet the security requirements of various applications, HK32C105 also supports cyclic redundancy check (CRC) which can be used to verify data accuracy and data integrity during data transmission and storage.

HK32C105 incorporates a wide selection of communication interfaces:

- 3 × UARTs of up to 12 Mbit/s

  The universal asynchronous receiver/transmitter (UART) supports the standard non-return-to-zero (NRZ) asynchronous serial data format and supports full-duplex communication. Each UART offers different baud rates by using its own baud rate generator and supports single-wire half-duplex communication and multiprocessor communication. In addition, the UART can work with direct memory access (DMA) to realize high-speed communication.

- 2 × high-speed SPIs/I2Ss of up to 18 Mbit/s

  The SPIs/I2Ss support the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, automatic CRC, and I2S protocol.

- 2 × high-speed I2Cs of up to 1 Mbit/s

  The I2Cs support the 1 Mbit/s, 400 kbit/s, and 100 kbit/s transmission rates, master/slave mode, multimaster mode, 7-bit/10-bit addressing, and SMBus protocol. The I2Cs can wake up the MCU from Stop mode when receiving data.

HK32C105 embeds a 16-bit advanced PWM timer (four PWM outputs in total, three of which have programmable inserted dead-times), a 32-bit and five 16-bit general-purpose PWM timers (up to four PWM outputs), and a basic timer.

HK32C105 also incorporates the analog circuitry: a 12-bit ADC (up to 24 analog signal input channels, differential pair input supported; sampling rate of up to 1.14 MSPS), a power-on reset (POR)/power-down reset (PDR) circuitry, a programmable voltage detector (PVD), and an internal reference voltage sampled by on-chip ADC.

HK32C105 integrates the division and square root hardware unit, which provides higher performance than software and faster responses to external events.

Except for the power pins, ground pins, NRST pin, and not connected (NC) pins, all the other pins of HK32C105 can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32C105 operates in the –40°C to +105°C temperature range, from a 2.6 V to 5.5 V power supply. It meets the environmental requirements of most applications.

With its diversified peripherals, HK32C105 is suitable for a wide range of applications:

- Programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Internet of Things (IoT) terminals, such as water meters, electricity meters, and gas meters
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots

- Smartwatches and fitness trackers
- Electronic toll collection (ETC)

2.1 Features

- CPU core
  - ARM® Cortex®-M0
  - Maximum frequency: 64 MHz
  - 24-bit SysTick timer
  - Supports the remapping of interrupt vectors (by configuring the Flash controller register)
- Operating voltage range
  - Main power supply V_{DD}: 2.6 V to 5.5 V
- Operating temperature range: –40°C to +105°C
- Typical operating current
  - Run mode: 1.46 mA@8 MHz; 7.31 mA@64 MHz
  - Sleep mode: 1.05 mA@8 MHz; 671 µA@32 kHz
  - Stop mode:
    - Low dropout regulator (LDO) full-speed: 128 µA@3.3 V
    - LDO low-power: 2.8 µA@3.3 V
- Memory
  - 64-Kbyte Flash
    - No wait states to access Flash when the CPU frequency is 24 MHz or lower
    - Separate read and write protection for Flash data
  - 10-Kbyte SRAM
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz
  - High-speed internal clock (HSI): 64 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL clock: 64 MHz (maximum value)
  - GPIO external input clock: 32 MHz (maximum value)
- Reset
  - External pin reset
  - Option byte loading (OBL) reset
  - IWDG and WWDG reset
  - POR/PDR
  - Software reset
  - Low-power mode reset
- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detected voltage
  - Rising edge and falling edge detection configurable
- GPIO

- Up to 34 GPIO pins
- Each GPIO pin can be used as an external interrupt input
- Provide the drive current of up to 40 mA

- Data communication interfaces
  - 3 × UARTs: each offers different baud rates by using its own baud rate generator and supports single-wire half-duplex communication and multiprocessor communication.
  - 2 × high-speed SPIs: support 4-bit to 16-bit programmable data frames, I2S multiplexed.
  - 2 × I2Cs: can operate in fast mode plus (1 MHz) and support SMBus and PMBus. Can wake up the MCU from Stop mode when receiving data.
- Timer and PWM generator
  - 1 × 16-bit advanced timer: with the break function and four PWM outputs in total, three of which are complementary PWM outputs with programmable inserted dead-times
  - 5 × 16-bit and 1 × 32-bit general-purpose timers: TIM2/TIM3/TIM14/TIM15/TIM16/TIM17
  - 1 × 16-bit basic timer: TIM6
- DMA controller (five-channel)
  - Can be triggered by the timer, ADC, SPI, I2C, or UART
- Division and square root (DVSQ) calculation unit
  - Supports 32-bit fixed point division, with the quotient and remainder calculated
  - Supports 32-bit fixed point high-precision root calculation
- On-chip analog circuitry
  - 1 × 12-bit SAR ADC (up to 24 analog input channels)
    - Maximum rate: 1.14 MSPS
    - Supports automatic continuous conversion and scan conversion
  - Internal reference voltage
- Temperature sensor
  - 9-bit temperature sensor, temperature sampling ranging from –40°C to 105°C
- RTC
  - Supports the alarm function
- Data security
  - Cyclic redundancy check (CRC) hardware implementation unit
- 96-bit unique ID (UID) of each MCU
- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Reliability
  - Passes HBM6500V/CDM2000V/LU800mA level tests.

2.2 Device overview

Table 2-1 HK32C105 series features

Feature		HK32C105S8T7	HK32C105K8T7	HK32C105K8U7
GPIO		34	25	25
Package		LQFP44	LQFP32	QFN32
Operating voltage		2.6 V – 5.5 V		
Operating temperature		–40°C to +105°C		
Memory	Flash	64-Kbyte		
	SRAM	10-Kbyte		
CPU	Core	Cortex®-M0		
	Frequency	64 MHz		
DMA		Five-channel (supports timer/ADC/SPI/I2C/UART)		
Division and square root (DVSQ) calculation unit		Supported		
Clock	LSI	40 kHz		
	HSI	64 MHz		
	PLL clock	64 MHz (maximum value)		
	HSE	4 MHz – 32 MHz		
	GPIO input clock	32 MHz (maximum value)		
Timer	Advanced timer	TIM1 (16-bit)		
	General-purpose timer	32-bit: TIM2 16-bit: TIM3/TIM14/TIM15/TIM16/TIM17		
	Basic timer	TIM6 (16-bit)		
	SysTick timer	Supported		
	RTC	Supported		
	IWDG	Supported		
	WWDG	Supported		
IRTIM		1		
Data comm.	UART	3		
	I2C	2		
	SPI (I2S)	2 (2)		
ADC	ADC (external channels)	1 (24)	1 (16)	1 (16)
	Reference selection	Internal reference voltage input		
	ADC sampling rate	1.14 MSPS		
	ADC accuracy	12-bit		
Temp. sensor	Accuracy	9-bit		
	Sampling range	–40°C to +105°C		
PVD		Supported		
CRC		Supported		
96-bit UID		Supported		

3 Function description

3.1 Block diagram

HK32C105 integrates a Flash memory of up to 64 Kbytes to store programs and data.

ARM® Cortex®-M0 is a 32-bit RISC processor, which provides an MCU platform featuring low cost, high performance, and ultra-low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With the ARM® Cortex®-M0 core embedded, the HK32C105 family is compatible with all ARM tools and software.

The following figure shows the block diagram of HK32C105S8T7 as an example:

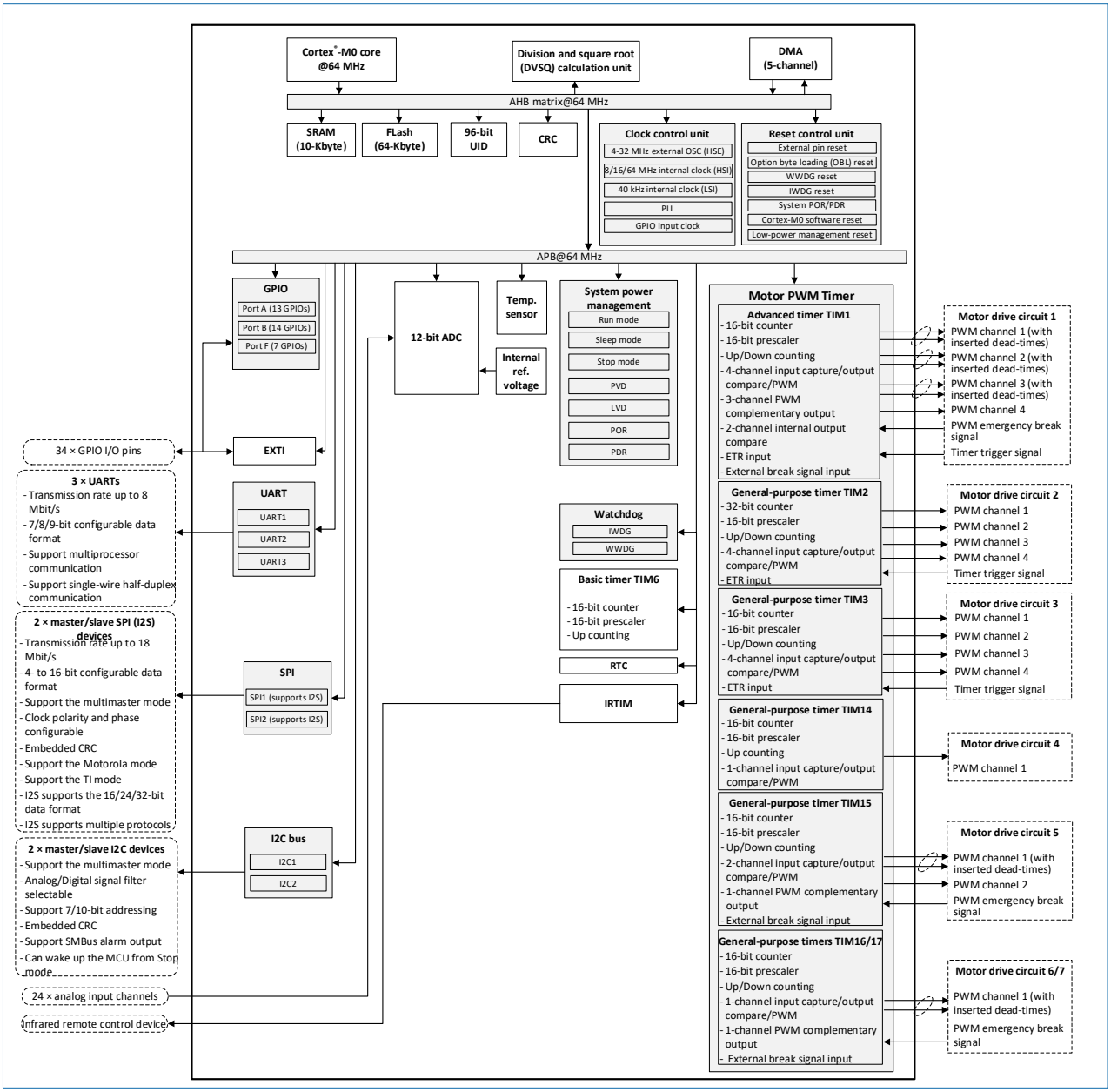

Figure 3-1 HK32C105S8T7 block diagram

3.2 Memory mapping

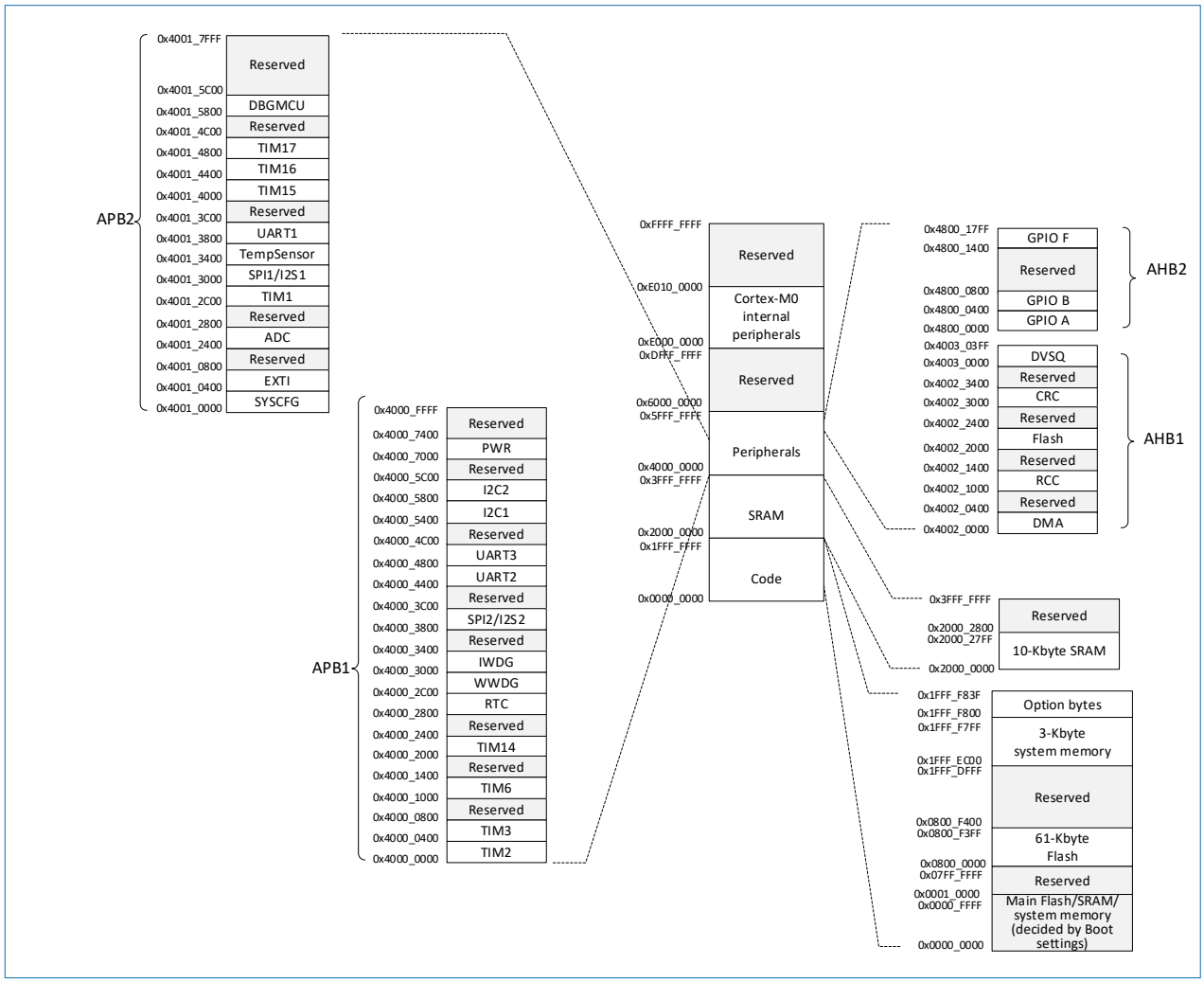

Figure 3-2 HK32C105 memory mapping

3.3 Memory

3.3.1 Flash

HK32C105 contains a 64-Kbyte Flash memory to store programs and data. The Flash memory comprises 61 Kbytes of main Flash and three Kbytes of bootloader area that can be used as the main Flash by configuring the option byte.

You can configure the Flash controller register to remap interrupt vectors in the 64-Kbyte space.

3.3.2 SRAM

HK32C105 integrates a 10-Kbyte SRAM that can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.4 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32C105 integrates a CRC hardware calculation unit. It is used to get a CRC code from an 8-, 16-, or 32-bit data word by using a generator polynomial.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with the reference signature that is generated at link time and stored at a specified memory location.

3.5 Power supply scheme

The V_{DD} ranging from 2.6 V to 5.5 V is the external power supply (no V_{BAT}) that supplies power to the digital circuitry, I/O pins, and internal voltage regulator of the MCU.

3.6 Power supply monitor

HK32C105 MCUs contain the POR/PDR circuitry. POR and PDR ensure that the internal logic is powered on as expected and the system can operate normally when the power supply exceeds 2.6 V. When V_{DD} is less than the POR/PDR/BOR threshold, the device is in the reset state and no external reset circuit is required.

The device incorporates a PVD which can monitor V_{DD} and V_{DDA} and compare them with the V_{PVD} threshold. The V_{PVD} threshold can be configured by using the software. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated, and the interrupt program sends a warning message. The PVD is enabled by setting the register.

3.7 Resets

3.7.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR. You can identify the reset source by checking reset status flags in the RCC_CSR register.

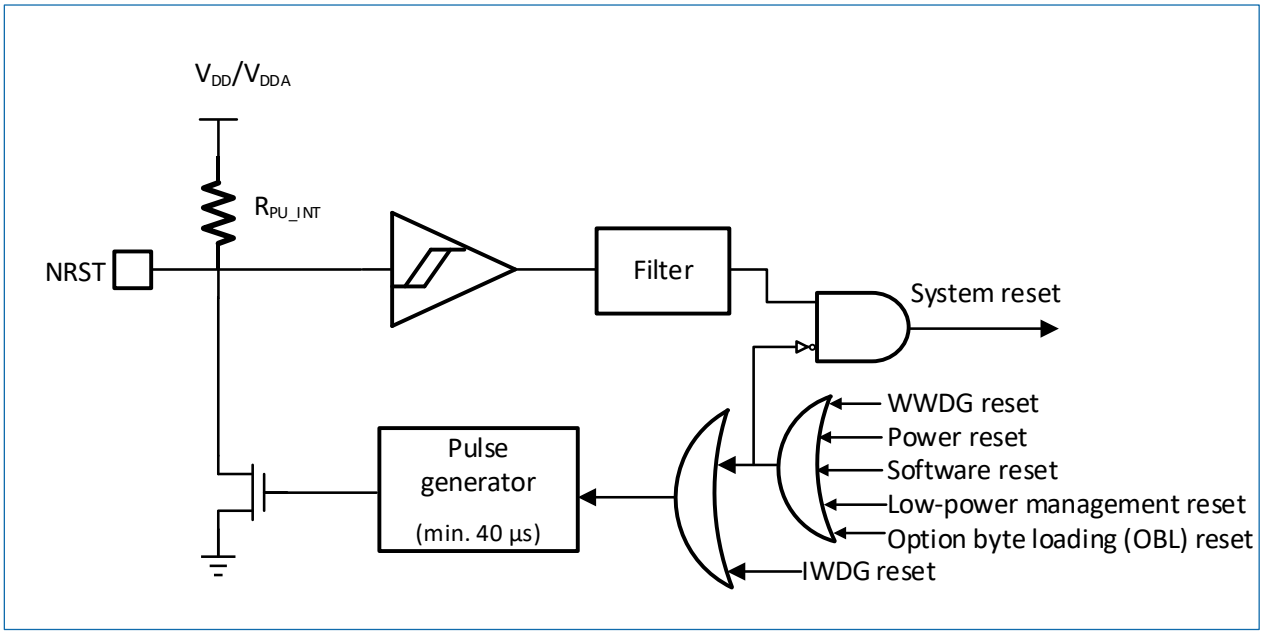

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Option byte loading (OBL) reset
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Power reset (POR/PDR)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset entry

vector is fixed on address 0x00000004. The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.7.2 Power reset

A power reset is generated when the following event occurs:

- Power-on reset (POR)/Power-down reset (PDR)

HK32C105 MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the 2.6 V threshold. When V_{DD} is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

3.7.3 Backup domain reset

When any of the following two events occurs, an exclusive reset of the backup domain is generated:

- Software reset triggered by the BDRST bit in the backup domain control register RCC_BDCR.
- V_{DD} (no V_{BAT}) is powered on after being powered off

3.8 Clocks and clock tree

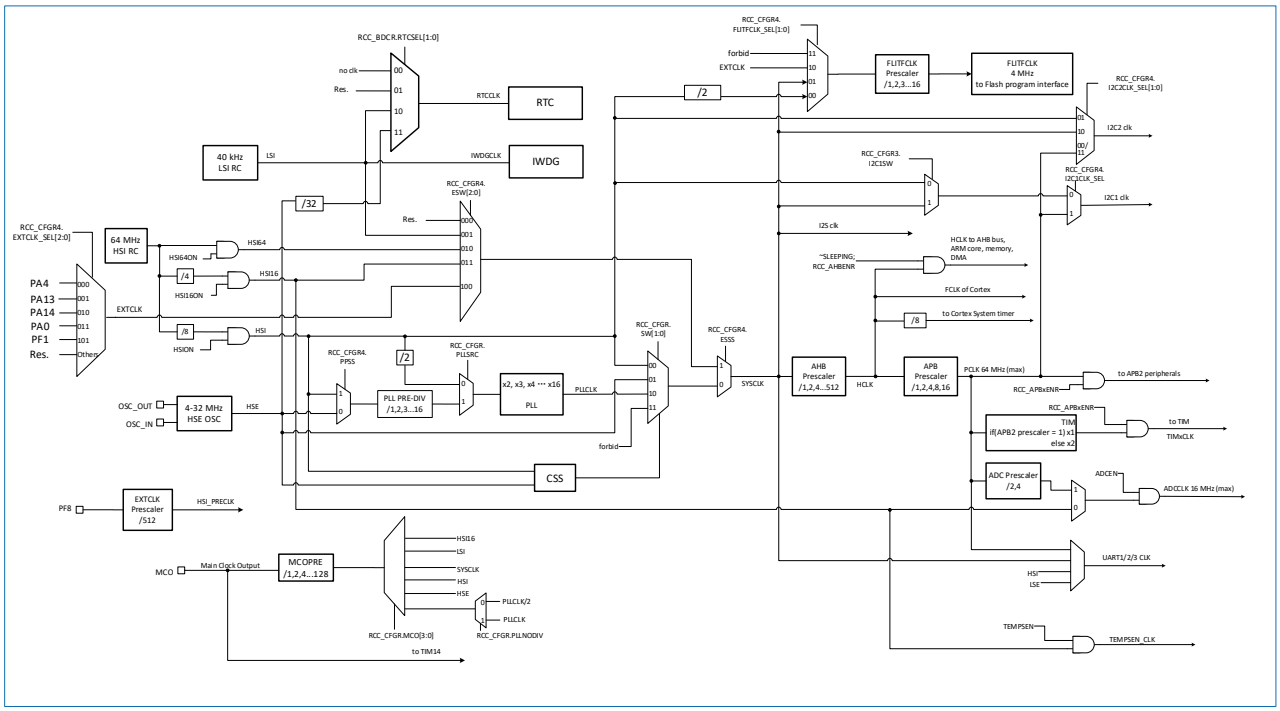

Figure 3-4 Clock tree

As the figure shows, HSI and HSI16 are generated by the same internal oscillator operating at 64 MHz. Therefore, when HSI or HSI16 is used, disabling the other clock cannot reduce power consumption. HSI/HSE can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI together with PLL to configure different system clock frequencies.

HK32C105 MCUs use SYSCLK as the CPU clock when they start. The internal oscillator outputs a 64 MHz clock. This 64 MHz clock divided by eight is the HSI that is used as the default system clock when the MCU is powered on.

HK32C105 provides more clock sources for the system clock and offers convenient, flexible, and diverse operating modes to customers. The following clocks can act as the system clock:

- High-speed external clock (HSE): 4 MHz to 32 MHz

- High-speed internal clock (HSI): 8 MHz (HSI)/16 MHz (HSI16)/64 MHz (HSI64)
- Low-speed internal clock (LSI): 40 kHz
- PLL clock: 64 MHz (maximum value)
- GPIO external input clock: 32 MHz (maximum value)

The clock frequency of the AHB and the APB domain can be configured by using several prescalers. The maximum clock frequency of the AHB can be 64 MHz. The maximum clock frequency of the APB domain can be 64 MHz.

The clock security system (CSS) supervises the HSE and switches to another clock source when it detects faults.

3.9 SYSCFG

The HK32C105 MCU has a set of system configuration registers. SYSCFG provides the following functions:

- Enable or disable the fast mode plus of I2C on some I/O ports.
- Remap some DMA trigger sources to other DMA channels.
- Remap the memory areas.
- Manage external interrupts connected to GPIOs.
- Manage the reliability feature of the system.

3.10 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by the digital and analog alternate functions. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed by performing a specific operation, which helps avoid unexpected writes to the I/O registers.

3.11 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram the Flash via UART1 PA9/PA10 or UART2 PA14/PA15.

3.12 Low-power modes

HK32C105 supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain are disabled. MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any external I/O pin or an RTC alarm.

3.13 Interrupts and events

3.13.1 NVIC

The nested vectored interrupt controller (NVIC) is closely connected with the CPU core interface, which ensures low-latency interrupt processing and efficient processing of late-arriving interrupts. NVIC manages all exceptions, including interrupts.

- 30 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines)
- Four programmable interrupt priorities (2-bit)
- Low latency in exception handling and interrupt processing
- Power management control
- Implementation of system control registers

3.13.2 EXTI

The extended interrupt/event controller (EXTI) manages internal and external interrupts and events. It outputs event requests to the CPU, outputs interrupt requests to the interrupt controller, and outputs wakeup requests to the power supply control module.

EXTI can be categorized into edge-configurable EXTI and edge-fixed EXTI. Their differences are:

Edge-configurable EXTI:

- The trigger edge can be the rising edge or falling edge.
- The pending register maintains interrupt status.
- The bits of software interrupt event register EXTI_SWIER can be written for the simulated generation of interrupts/events.

Edge-fixed EXTI:

- Only the rising edge is the trigger edge.
- The EXTI is used to wake up the core from Stop mode and it only operates in Stop mode.
- The interrupt status of edge-fixed EXTI is not recorded in the pending register but is provided by the corresponding IP.

The EXTI manages up to 21 interrupts/events. Each interrupt or event line can be masked and enabled independently.

3.14 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode. The IWDG can reset the system when a problem occurs or work as a free-running timer to provide timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the window register IWDG_WINR to use IWDG in window mode.

3.15 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.16 Timers

The HK32C105 MCU has an advanced timer, six general-purpose timers, and a basic timer. The following table describes the features of timers.

Table 3-1 Features of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced	TIM1	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	4	3
General-purpose	TIM2	32-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	No	4	No
	TIM3	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	No	4	No
	TIM14	16-bit	Up	Any integer from 1 to 65536	No	No	1	No
	TIM15	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	2	1
	TIM16	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	1	1
	TIM17	16-bit	Up, down, up/down	Any integer from 1 to 65536	Yes	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer from 1 to 65536	Yes	No	No	No

3.16.1 Advanced timer

HK32C105 integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

- 2-channel internal output compare

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If TIM1 is configured as a 16-bit PWM generator, it has full modulation capability (0–100%). Many functions of TIM1 are the same as those of general-purpose timers. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

3.16.2 General-purpose timer

HK32C105 integrates six general-purpose timers.

- TIM2 and TIM3

TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have four independent channels respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output.

TIM2 and TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14

  TIM14 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 has one channel for input capture, output compare, PWM output, and one-pulse mode output. In debug mode, the counter can be frozen. TIM14 cannot generate DMA requests.

- TIM15, TIM16, and TIM17

  TIM15, TIM16, and TIM17 are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler respectively. TIM15, TIM16, and TIM17 all have complementary outputs with programmable inserted dead-times and can generate independent DMA requests. TIM15 has two channels. TIM16 and TIM17 have one channel respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output. In debug mode, the counter can be frozen.

3.16.3 Basic timer

HK32C105 integrates a basic timer TIM6.

TIM6 embeds a 16-bit upcounter and a 16-bit prescaler. It is used to generate periodic CPU interrupt requests and can generate DMA requests. In debug mode, the counter can be frozen.

3.16.4 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.17 DMA

The general-purpose DMA controller (with five channels) manages the data transfer from memories to memories, from peripherals to memories, and from memories to peripherals. The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel has a dedicated hardware DMA request logic, and can also be triggered by software. The data size, source address, and destination address of each channel can be set by using the software. DMA can be used with the main peripherals, such as SPI, I2C, UART, TIMx, and ADC.

3.18 ADC

HK32C105 incorporates a 12-bit analog-to-digital converter (ADC) which has a total of 24 external channels and two internal channels. The A/D conversions on different channels can be performed in single, continuous, scan, or discontinuous mode. The oversampling function can reduce the CPU workload and increase the data width to up to 16-bit by handling multiple conversions and calculating the average value of multiple conversion results.

- The ADC conversion rate is 1.14 MSPS when its clock frequency is 16 MHz.
- The ADC can be served by the DMA controller.

- The events generated by general-purpose timers (TIM2/TIM3/TIM15) and advanced timer (TIM1) can be internally connected to the ADC start trigger so that A/D conversions can be triggered.

3.18.1 Internal reference voltage

The internal reference voltage V_{REFINT} provides a stable voltage output (bandgap voltage reference) for the ADC.

3.19 Temperature sensor

A 9-bit temperature sensor with a temperature sampling range from –40°C to +105°C is embedded in HK32C105. The temperature sensor automatically collects and outputs temperature sampling data.

3.20 IRTIM

An infrared interface (IRTIM) is embedded in HK32C105 MCUs. The IRTIM works with infrared LEDs to provide the remote control function. To generate infrared remote control signals, the IRTIM must be enabled and TIM16 channel 1 (TIM16_OC1) and TIM17 channel 1 (TIM17_OC1) must be configured.

The infrared receiver function can be implemented by setting TIM16 channel 1 and TIM17 channel 1 to the basic input capture mode.

3.21 I2C bus

Two I2C bus interfaces are embedded in HK32C105 MCUs. The I2C bus interfaces can operate in master or slave mode and support the following modes:

- Standard mode (up to 100 kHz)
- Fast mode (up to 400 kHz)
- Fast mode plus (up to 1 MHz)

The I2C bus interfaces support the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interfaces have embedded hardware CRC generation/verification.

The I2C interfaces provide hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, host notify protocol, hardware CRC (PEC) generation and verification, timeout verification, and ALERT protocol management.

The I2C interfaces have a clock independent of the CPU clock domain, so they can wake up the MCU from Stop mode when the address is matched.

Table 3-2 I2C features

I2C Feature	I2C1/I2C2
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast/Fast mode plus	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
DMA transmission	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

3.22 UART

Three universal asynchronous receivers/transmitters (UART1/UART2/UART3) are embedded in each HK32C105 MCU. They can communicate at up to 8 Mbit/s. The UARTs provide hardware management of multiprocessor

communication mode and single-wire half-duplex communication mode. The UARTs can be served by the DMA controller.

Table 3-3 UART1/UART2/UART3 features

UART Mode/Feature	UART1/UART2/UART3/
Data word length	7/8/9-bit
DMA transmission	Supported
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported

3.23 SPI/I2S

Two SPI interfaces operating at up to 18 Mbit/s are embedded in HK32C105 MCUs. The SPI interfaces support full-duplex and half-duplex communication in master or slave mode. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4-bit to 16-bit.

Table 3-4 SPI1/SPI2 features

SPI Feature	SPI1/SPI2
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
I2S mode	Supported
TI mode	Supported
DMA transmission	Supported

The standard I2S interfaces (with SPI multiplexed) provide four types of audio standards and can operate in master/slave half-duplex communication mode. The I2S interfaces have dedicated signals for data synchronization. The data format can be 16-bit, 24-bit, or 32-bit and the I2S interfaces can operate with 16- or 32-bit resolution. The I2S interfaces can be set to an audio sampling frequency from 8 kHz to 192 kHz by the 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components.

Table 3-5 I2S features

I2S Feature	I2S
Half-duplex mode	Supported
Master/Slave mode configurable	Supported
8-bit programmable linear prescaler	Supported
Data format programmable	Supported
Clock polarity programmable	Supported
I2S protocol	Supported
DMA transmission	Supported
Driving external audio components	Supported

3.24 RTC

The real-time clock (RTC) has an independent binary-coded decimal (BCD) timer/counter. The RTC has the following features:

- Displays of the sub-seconds, seconds, minutes, hours (12- or 24-hour format), day of the week, day of the month, month, and year in BCD
- Automatic adjustment to the days of different months: 28 days, 29 days (leap year), 30 days, and 31 days
- A programmable alarm capable of wakeup from Stop mode
- Correction of 1 to 32,767 RTC clock pulses during runtime for synchronization between RTC and the main clock
- Digital calibration circuit with 0.95 ppm accuracy for compensation of deviation in crystal oscillators
- A tamper detection pin with programmable filters. Wakeup from Stop mode when any tamper event is

detected.

- Reference clock detection: a more accurate secondary clock source (50 Hz or 60 Hz) that can be used to improve calendar accuracy

3.25 DVSQ calculation unit

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - Supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports the divide-by-zero interrupt and overflow interrupt.

3.26 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32C105 MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process of the security mechanism.

3.27 Debug port

Based on the ARM SWJ-DP embedded in HK32C105, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	5.5	V
V_{IN}	Input voltage on pins	–0.3	5.5	
$\lvert V_{SSX} – V_{SS} \rvert$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	105	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	30	
	Output current sourced by any I/O and control pin	30	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–55	130	°C
T_J	Maximum junction temperature	–45	110	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	64	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	64	
f_{PCLK2}	Internal APB2 clock frequency	-	64	
V_{DD}	Standard operating voltage	2.6	5.5	V
V_{DDA}(1)	Analog operating voltage	2.6	5.5	V
T	Operating temperature	–40	105	°C

(1). V_{DDA} can be lower than V_{DD}. For example, V_{DD} = 4.2 V, V_{DDA} = 3.3 V; V_{DD} = 3.3 V, V_{DDA} = 2.6 V.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (–40°C to 105°C)	Level 1	-	-	-	V
		Level 2	2.55	2.59	2.65	
		Level 3	2.94	3.00	3.05	
		Level 4	3.33	3.39	3.43	
		Level 5	3.72	3.77	3.84	
		Level 6	4.11	4.16	4.22	
		Level 7	4.49	4.55	4.61	
		Level 8	4.86	4.91	5.04	

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge	1.67	1.92	2.30	V
		Rising edge	1.82	2.08	2.53	V
$V_{PDRhyst}$	PDR hysteresis	-	150	160	160	mV
$t_{RSTTEMPO}$(2)	Reset duration	-	-	2	-	ms

(1). PDR and POR are based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	-	1.2	-	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Symbol	Mode	Condition	V_{DD} = 3.3 V			V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	–40°C	25°C	105°C	
I_{run}	Run mode	SYSCLK = 64 MHz; LSI and PVD enabled, other peripherals disabled; All I/Os configured in high impedance; Two wait states to access Flash.	6.86	7.31	7.43	6.91	7.39	7.54	mA
		SYSCLK = 8 MHz;	1.41	1.46	1.59	1.41	1.49	1.59	mA

Symbol	Mode	Condition	V_{DD} = 3.3 V			V_{DD} = 5 V			Unit
			–40°C	25°C	105°C	–40°C	25°C	105°C	
		LSI and PVD enabled, other peripherals disabled; All I/Os configured in high impedance; Zero wait states to access Flash.							
		SYSCLK = 40 kHz; All I/Os configured in high impedance; LSI and PVD enabled, other peripherals disabled; Zero wait states to access Flash.	0.63	0.68	0.8	0.64	0.68	0.83	mA
I_{Sleep1}	Sleep mode 1	SYSCLK = 64 MHz; AHB/APB enabled; All clocks in the core domain disabled, all peripherals disabled; All I/Os configured in high impedance; RAM and peripheral data retained.	3.45	3.71	3.90	3.49	3.78	3.91	mA
		Wakeup time	1.25	2.8	1.2	1.25	2.8	1.2	µs
I_{Sleep2}	Sleep mode 2	SYSCLK = 8 MHz; AHB/APB enabled; All clocks in the core domain disabled, all peripherals disabled; All I/Os configured in high impedance; RAM and peripheral data retained.	1.01	1.05	1.21	1.03	1.08	1.2	mA
		Wakeup time	6.5	6.5	6.6	6.5	6.5	6.6	µs
I_{Sleep3}	Sleep mode 3	SYSCLK = 40 kHz; AHB/APB enabled; All clocks in the core domain disabled, all peripherals disabled; All I/Os configured in high impedance; RAM and peripheral data retained.	615	671	773	623	682	784	µA
		Wakeup time	0.7	1.6	0.68	0.7	1.6	0.68	ms
I_{Stop}	Stop mode	All clocks in the core domain stopped, HSI oscillator and HSE oscillator disabled, LSI oscillator enabled, all peripherals disabled; LDO operating in normal power mode; All I/Os configured in high impedance; Backup registers retained; CPU, RAM, and peripheral data retained.	119	128	162	123	132	260	µA
		Wakeup time	18	30	19	18	30	19	µs
I_{LPstop}	Low-power stop mode	All clocks in the core domain stopped, HSI oscillator and HSE oscillator disabled, LSI oscillator enabled; LDO operating in low-power mode, all peripherals disabled; All I/Os configured in high impedance; Backup registers retained; CPU, RAM, and peripheral data retained.	1.9	2.8	15	3.2	4.6	17.9	µA
		Wakeup time	220	240	220	220	240	220	µs

4.2.6 HSE clock characteristics

Table 4-9 HSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
R_F(1)	Feedback resistor	-	-	2	-	MΩ
$T_{stb\ (HSE)}$(2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	0.2	1.1	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (R_S)	-	-	12	-	pF
$I_{DD\ (HSE)}$(1)	HSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12 pF	-	365	-	μA

(1). The value is guaranteed in design;

(2). $T_{stb\ (HSE)}$ refers to the time from HSE startup to the time when it outputs stable frequency signals.

HK32C105 integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

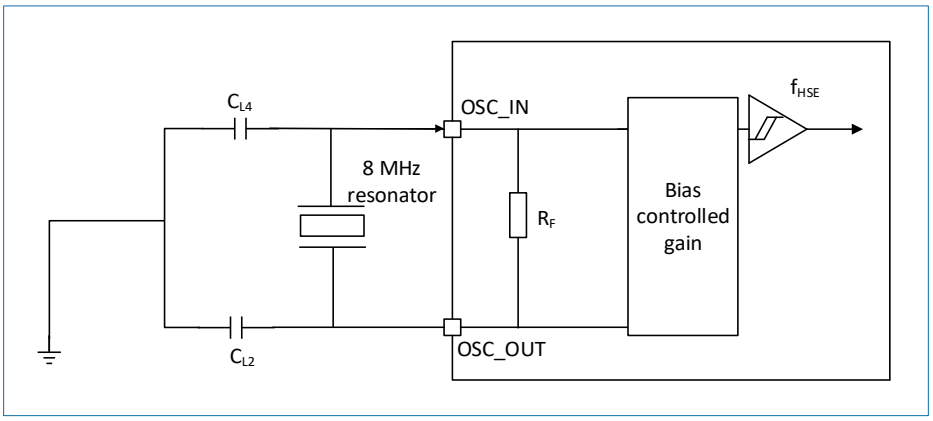

Figure 4-1 HSE negative feedback circuit

Alternatively, an HSE signal can be directly input from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-10 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	4	-	32	MHz
DuCy $_{(HSE)}$(1)	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.7 HSI clock characteristics

Table 4-11 HSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	64	-	MHz
DuCy$_{(HSI)}$(1)	Duty cycle	-	45	-	55	%
ACC$_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	–1	-	1	%
		Factory calibration: T_A = -40°C to +105°C	–1.2	-	1.5	
$T_{stb\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	5	8	μs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	8 MHz, V_{DD} = 3.3 V	-	160	195	μA

(1). The value is guaranteed in design.

4.2.8 LSI clock characteristics

Table 4-12 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	32	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	20	60	μs
$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	250	-	nA

(1). The value is guaranteed in design.

4.2.9 PLL characteristics

Table 4-13 PLL characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	-	80	MHz
	Input clock duty cycle	45	-	55	%
f_{PLL_OUT}	Output clock frequency	6	-	64	MHz
t_{LOCK}	PLL lock time	-	60	150	μs

(1). The value is guaranteed in design.

4.2.10 Flash memory characteristics

Table 4-14 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-word programming time	244		404	μs
T_{ERASE}	Page erase time	100		200	ms
	Mass erase time	100		200	ms
I_{DDPROG}	One-word programming current	-	-	8	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	9	mA
I_{DDREAD}	Read current@25 MHz	-		3	mA
N_{END}	Erasure endurance	100	-	-	Thousand cycles
t_{RET}	Data retention	10	-	-	Years

4.2.11 I/O pin input characteristics

Table 4-15 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	0.65 × V_{DD}	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	0.65 × V_{DD}	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	-	0.2 × V_{DD}	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V; 0 < V_{IN} < 3.3 V	-	-	10	nA
		V_{DD} = 3.3 V; V_{IN} = 5 V	-	-	270	nA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	33	-	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The value is guaranteed in design.

4.2.12 I/O pin output characteristics

Table 4-16 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	2.6 V ≤ V_{DD} ≤ 5.5 V	0.8 × V_{DD}			V
V_{OL}	Output low level voltage	2.6 V ≤ V_{DD} ≤ 5.5 V			0.2 × V_{DD}	V

4.2.13 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-17 NRST pin input characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{Noise}	Low level ignored duration	-	-	70	ns

4.2.14 TIM timer characteristics

Table 4-18 TIM characteristics (1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency	-	$f_{TIMxCLK}$/2	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 64 MHz.

4.2.15 ADC characteristics

Table 4-19 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when ADC is enabled	-	2.6	5	5.5	V
V_{REFP}	Positive reference voltage	-	2.6	5	5.5	V
V_{REFN}	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	16	28	MHz
f_S (1)	Sampling frequency	f_{ADC} = 16 MHz	-	1.14	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 16 MHz	-	-	941	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	V_{REFN}	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	For details, see Table 4-20.				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	2	kΩ
C_{ADC}(1)	Sample and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S(1)	Sampling time	f_{ADC} = 16 MHz	1.5	-	239.5	Cycles
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz 12-bit resolution	14	-	252	Cycles

(1). The value is guaranteed in design.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f}_{ADC} \times \boldsymbol{C}_{ADC} \times \ln(2^{N+2})} - \boldsymbol{R}_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-20 Maximum input impedance values (f_{ADC} = 16 MHz)

Sampling Cycles Ts (Cycles)	Sampling Time tS (μs)	Maximum Input Impedance (kΩ)
1.5	0.09	0
7.5	0.47	7.66
13.5	0.84	15.39
28.5	1.78	34.71
41.5	2.59	51.46
55.5	3.47	69.49
71.5	4.47	90.10
239.5	14.97	306.50

Table 4-21 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	SCLK = 64 MHz, ADCCLK = 16 MHz, input impedance < 1 kΩ, V_{DD} = 3.3 V, after ADC calibration	–3 to 0	–4 to 1	LSB
EO	Offset error(2)		1.5	0.5 to 1.5	
EG	Gain error(3)		1	–2 to 1	
ED	Differential linearity error(4)		–1 to 1	–2 to 1	
EL	Integral linearity error(5)		–1 to 1	–2 to 1	

(1). ET: total unadjusted error, the maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). EO: offset error, the deviation between the first actual conversion and the first ideal conversion.

(3). EG: gain error, the deviation between the last ideal conversion and the last actual conversion.

(4). ED: differential linearity error, the maximum deviation between the actual step and the ideal step.

(5). EL: integral linearity error, the maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With restricted V_{DDA}, frequency, and temperature ranges, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

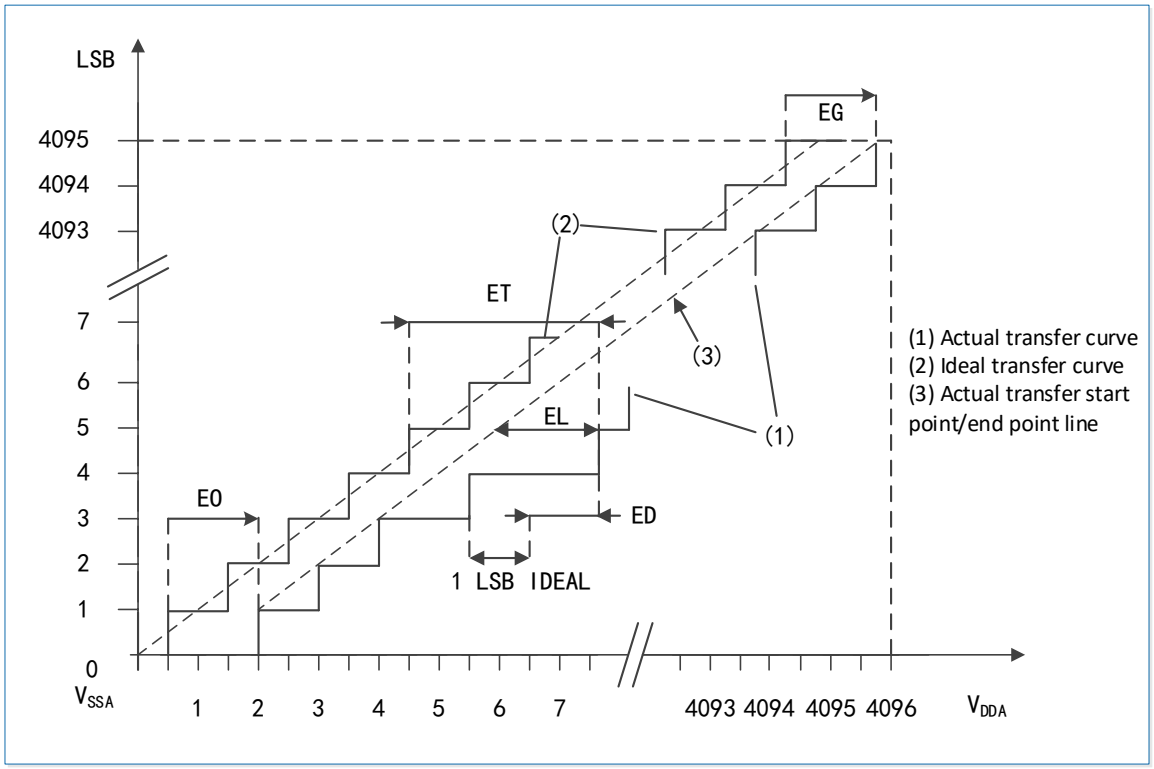

Figure 4-2 ADC accuracy characteristics

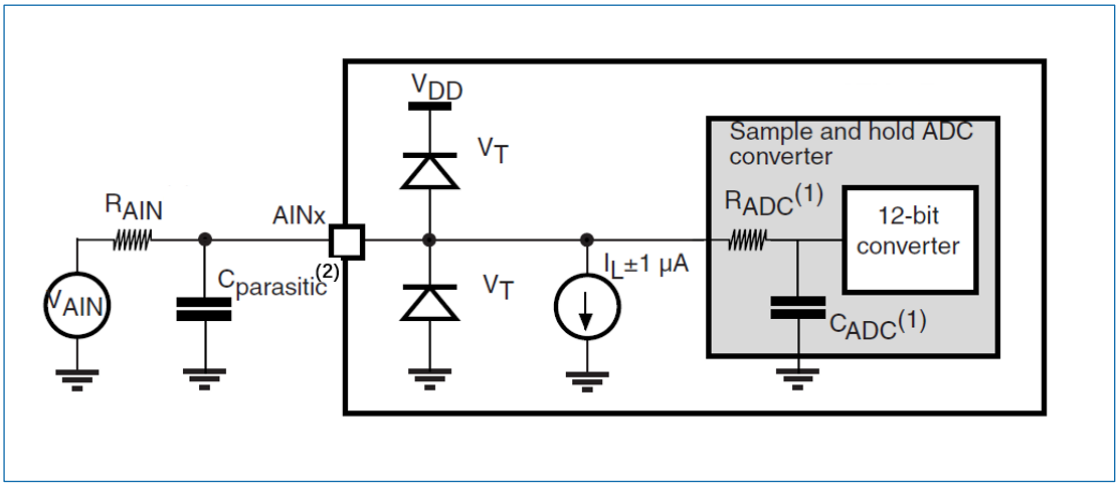

Figure 4-3 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-19.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

4.2.16 Temperature sensor characteristics

Table 4-22 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L	Temperature sensor linearity error	–20°C to 80°C TS_CLK ≤ 4 MHz	-	-	±5.2	°C
		–40°C to 105°C TS_CLK ≤ 4 MHz	-	-	±10	
T_{EN}	Startup time	20°C	-	-	1.5	µs
Ts	Temperature sampling time	Temperature sampling is completed once.	32			Cycles
Tcal	Calibration time	Calibration is completed once.	29			Cycles
PSRR	DC power supply rejection ratio	-	-	0.32	-	°C/V
Avg_Slope	Temperature sensor slope	-	-	1.81	-	LSB/°C
I_{stb_LV}	Power consumption in low-voltage Standby mode	-	0.065	0.146	26.51	nA
I_{stb_HV}	Power consumption in high-voltage Standby mode	-	0.254	0.689	87.33	nA
I_{act_LV}	Power consumption in low-voltage temperature measurement	-	95.59	124.0	453.3	nA
I_{act_HV}	Power consumption in high-voltage temperature measurement	-	0.468	0.731	1.200	mA

5 Typical circuitry

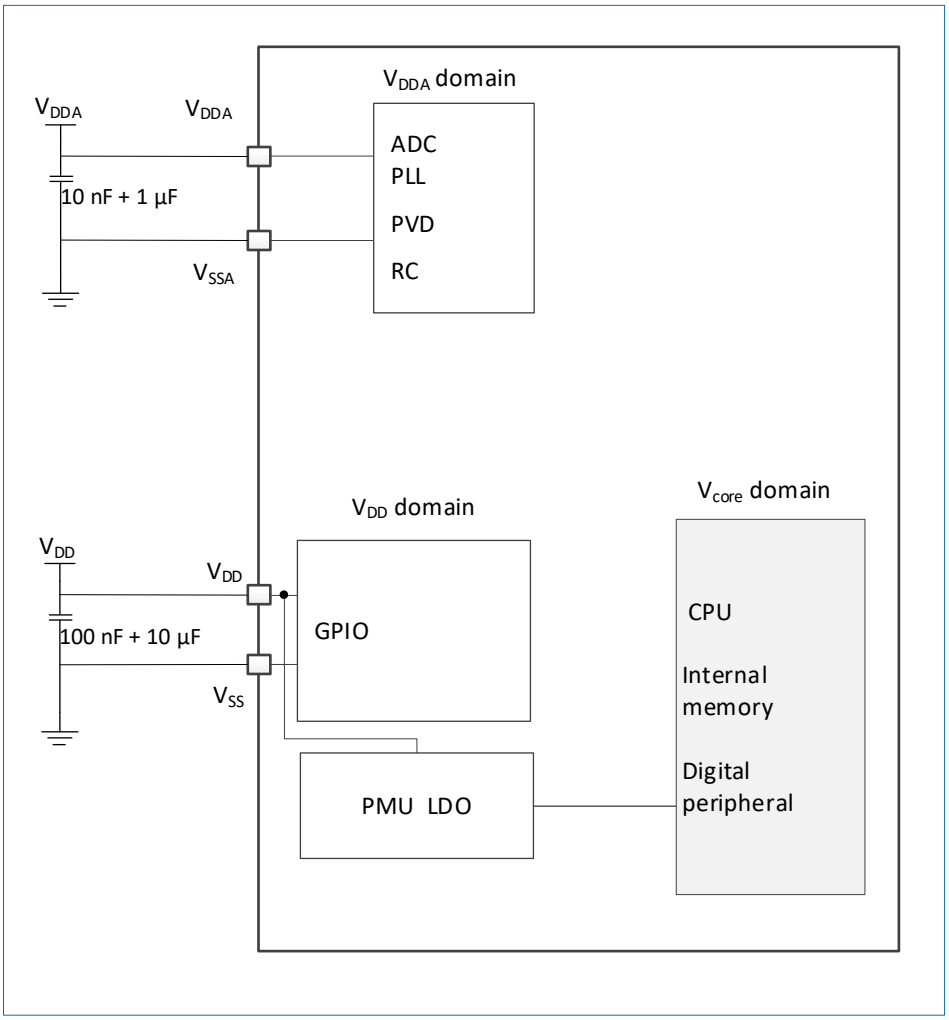

Figure 5-1 Power supply block diagram

6 Pinouts and pin descriptions

HK32C105 MCUs are delivered in LQFP44, LQFP32, and QFN32 packages. This chapter describes the pinout and pin description of each package.

6.1 LQFP44

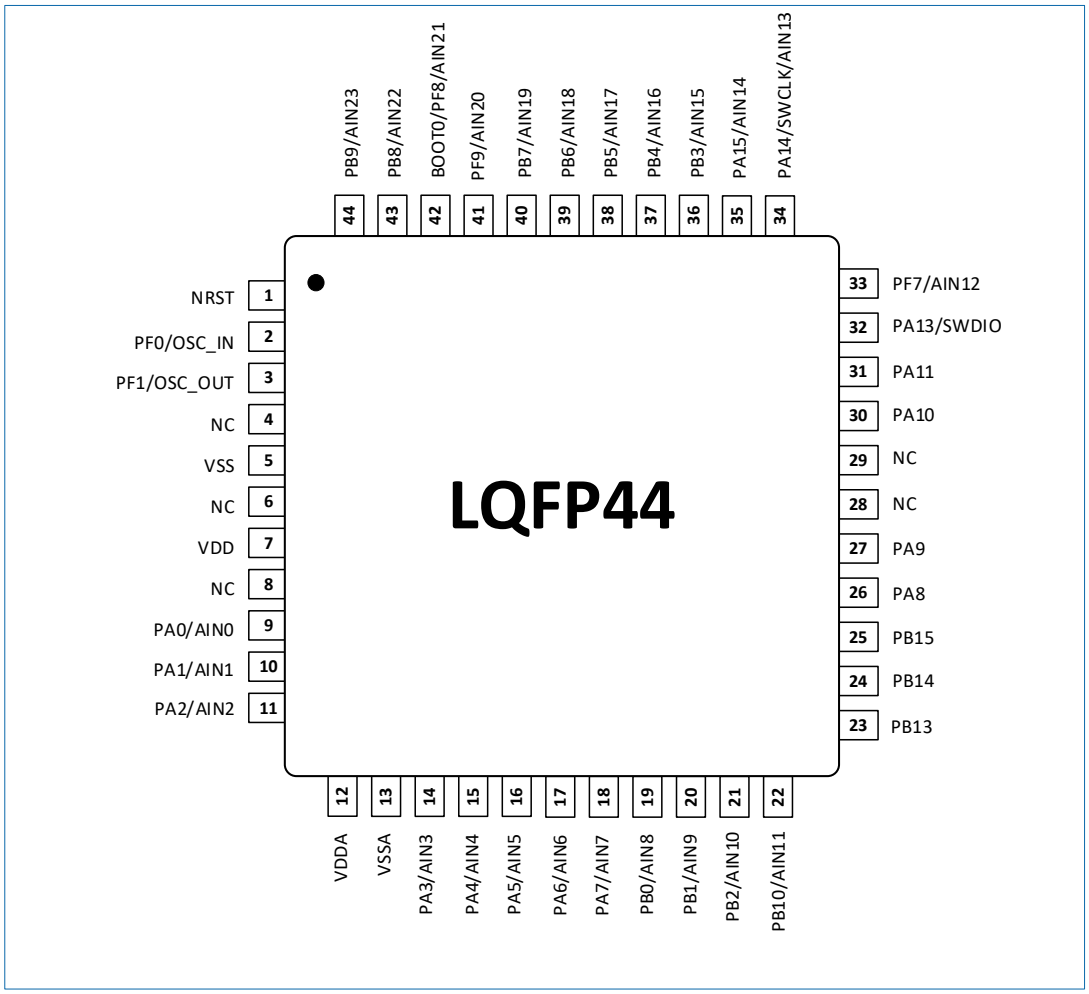

Figure 6-1 LQFP44 package pinout

6.2 LQFP32

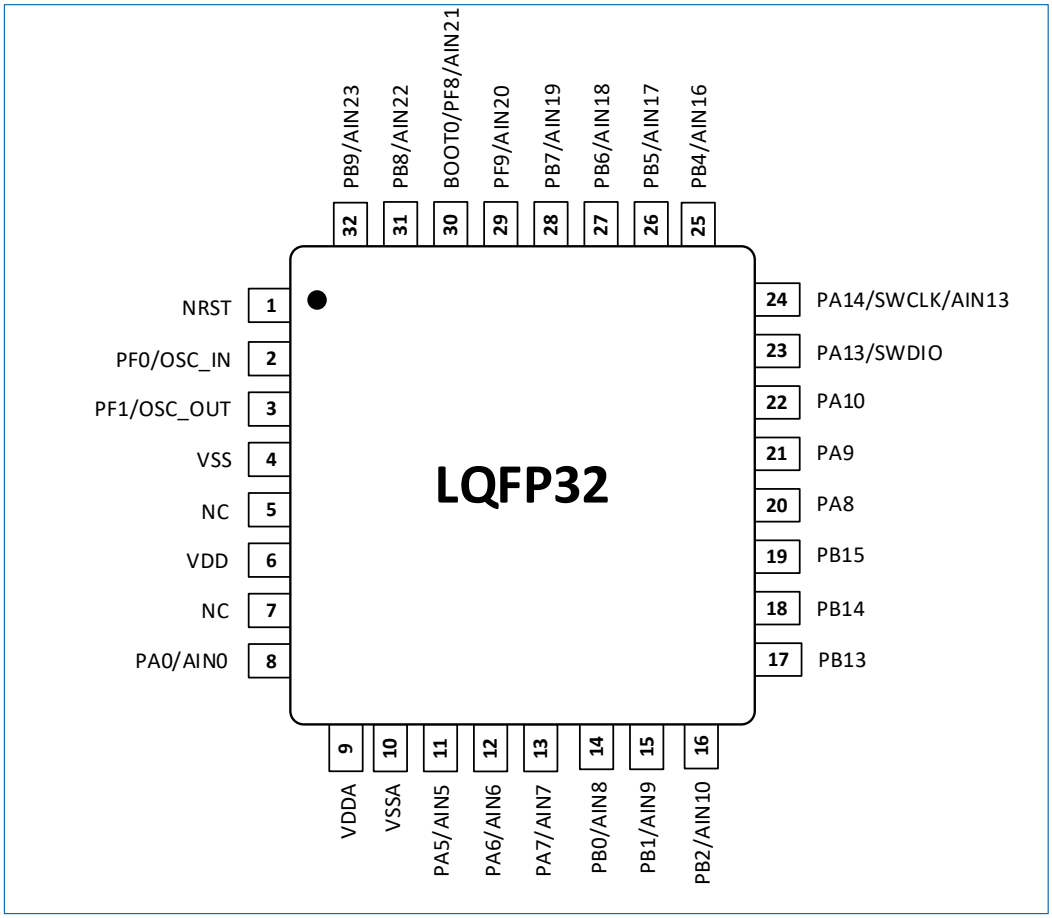

Figure 6-2 LQFP32 package pinout

6.3 QFN32

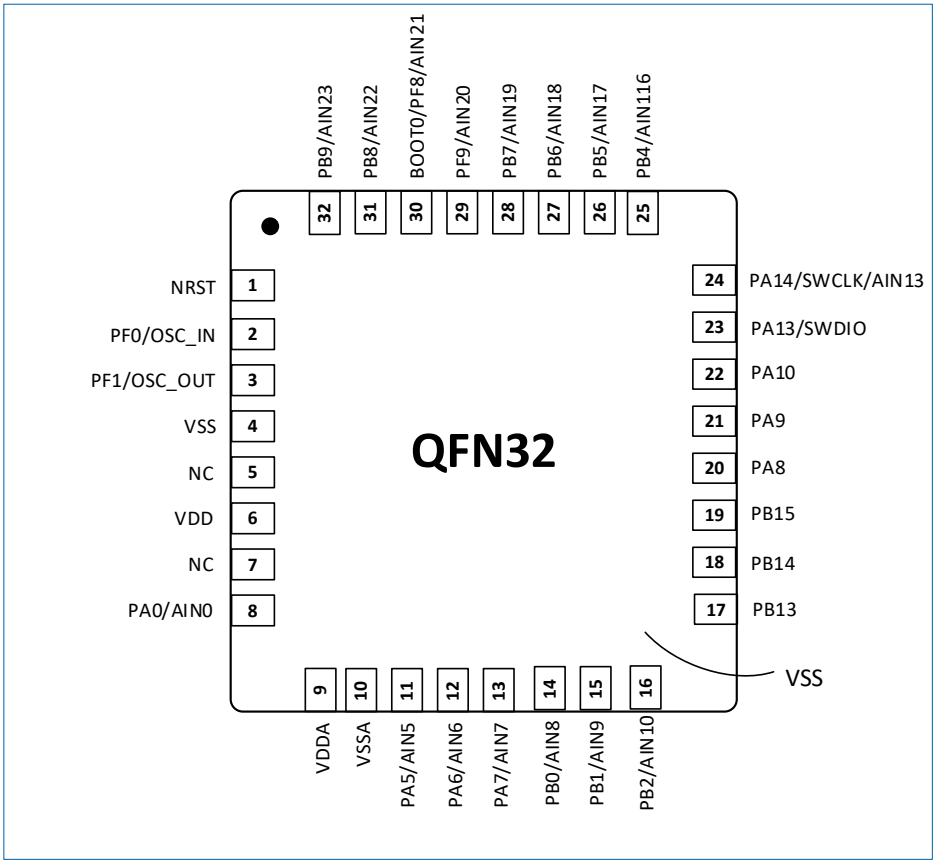

Figure 6-3 QFN32 package pinout

6.4 Pin descriptions

Table 6-1 Pin descriptions

LQFP44	LQFP32	QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-Tolerant(3)	Alternate Function	Additional Function
-	-	0	VSS/VSSA	S	-	Digital/Analog ground (Pin 0 is the thermal pad on the QFN package bottom.)	
1	1	1	NRST	I/O	FT	-	NRST
2	2	2	PF0/OSC_IN (PF0)	I/O	-	TIM14_CH1 I2C1_SDA/I2C1_SCL	EXTI0 OSC_IN HSE_CKI
3	3	3	PF1/OSC_OUT (PF1)	I/O	-	TIM3_CH1 I2C1_SCL/I2C1_SDA	EXTI1 OSC_OUT CKI_6
4	-	-	NC(2)	-	-	-	
5	4	4	VSS	S	-	Digital ground	
6	5	5	NC	-	-	-	
7	6	6	VDD	S	-	Digital power supply	
8	7	7	NC	-	-	-	
9	8	8	PA0/AIN0 (PA0)	I/O	FT	TIM2_CH1_ETR UART1_RX/UART1_TX(5)	EXTI0 AIN0 CKI_4 RTC_TAMP2
10	-	-	PA1/AIN1 (PA1)	I/O	FT	CM0_TXEV TIM2_CH2 UART1_TX/UART1_RX	EXTI1 AIN1

LQFP44	LQFP32	QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-Tolerant(3)	Alternate Function	Additional Function
						TIM15_CH1N	
11	-	-	PA2/AIN2 (PA2)	I/O	FT	SPI2_MISO/I2S2_MCK TIM15_CH1 UART1_TX/UART1_RX TIM2_CH3 UART2_TX/UART2_RX	EXTI2 AIN2
12	9	9	VDDA	S	-	Analog power supply	
13	10	10	VSSA	S	-	Analog ground	
14	-	-	PA3/AIN3 (PA3)	I/O	FT	TIM15_CH2 UART1_RX/UART1_TX TIM2_CH4 UART2_RX/UART2_TX I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA	EXTI3 AIN3
15	-	-	PA4/AIN4 (PA4)	I/O	FT	SPI1_NSS/I2S1_WS TIM14_CH1 I2C1_SDA/I2C1_SCL I2C2_SDA/I2C2_SCL	EXTI4 AIN4 CKI_1
16	11	11	PA5/AIN5 (PA5)	I/O	FT	SPI1_SCK/I2S1_CK TIM2_CH1_ETR I2C1_SDA/I2C1_SCL UART1_TX/UART1_RX I2C2_SDA/I2C2_SCL	EXTI5 AIN5
17	12	12	PA6/AIN6 (PA6)	I/O	FT	SPI1_MISO/I2S1_MCK TIM3_CH1 TIM1_BKIN I2C1_SCL/I2C1_SDA TIM16_CH1 CM0_TXEV	EXTI6 AIN6
18	13	13	PA7/AIN7 (PA7)	I/O	FT	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM1_CH1N IRTIM_IROUT TIM14_CH1 TIM17_CH1 CM0_TXEV RCC_MCO	EXTI7 AIN7
19	14	14	PB0/AIN8 (PB0)	I/O	FT	CM0_TXEV TIM3_CH3 TIM1_CH2N SPI1_NSS/I2S1_WS	EXTI0 AIN8
20	15	15	PB1/AIN9 (PB1)	I/O	FT	TIM14_CH1 TIM3_CH4 TIM1_CH3N SPI1_MOSI/I2S1_SD SPI2_MOSI/I2S2_SD	EXTI1 AIN9
21	16	16	PB2/AIN10 (PB2)	I/O	FT	TIM1_ETR SPI1_MISO/I2S1_MCK SPI2_MISO/I2S2_MCK I2C1_SDA/I2C1_SCL I2C2_SDA/I2C2_SCL I2C2_SMBA	EXTI2 AIN10
22	-	-	PB10/AIN11 (PB10)	I/O	FT	SPI1_SCK/I2S1_CK I2C1_SCL/I2C1_SDA TIM2_CH3 I2C2_SCL/I2C2_SDA TIM1_CH3 SPI2_SCK/I2S2_CK	EXTI10 AIN11

LQFP44	LQFP32	QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-Tolerant(3)	Alternate Function	Additional Function
						UART3_TX/UART3_RX	
23	17	17	PB13	I/O	FT	SPI1_SCK/I2S1_CK TIM1_CH1N SPI2_MOSI/I2S2_SD I2C2_SCL/I2C2_SDA	EXTI13
24	18	18	PB14	I/O	FT	SPI1_MISO/I2S1_MCK TIM15_CH1 TIM1_CH2N TIM3_CH1 UART1_TX/UART1_RX I2C2_SDA/I2C2_SCL SPI2_MISO/I2S2_MCK	EXTI14
25	19	19	PB15	I/O	FT	SPI1_MOSI/I2S1_SD TIM15_CH2 TIM1_CH3N TIM15_CH1N UART1_RX/UART1_TX TIM2_CH1_ETR SPI2_MOSI/I2S2_SD	EXTI15 RTC_REFIN
26	20	20	PA8	I/O	FT	RCC_MCO TIM3_CH1 TIM1_CH1 CM0_TXEV IRTIM_IROUT SPI1_SCK/I2S1_CK I2C1_SDA/I2C1_SCL I2C2_SDA/I2C2_SCL	EXTI8
27	21	21	PA9	I/O	FT	TIM15_BKIN UART1_TX/UART1_RX TIM1_CH2 SPI1_MISO/I2S1_MCK I2C1_SCL/I2C1_SDA RCC_MCO SPI2_MOSI/I2S2_SD UART3_RX/UART3_TX I2C2_SCL/I2C2_SDA TIM14_CH1	EXTI9 RCC_MCO
28	-	-	NC	-	-	-	
29	-	-	NC	-	-	-	
30	22	22	PA10	I/O	FT	TIM17_BKIN UART1_RX TIM1_CH3 SPI1_MOSI/I2S1_SD I2C1_SDA/I2C1_SCL TIM15_CH1 SPI2_SCK/I2S2_CK UART3_TX/UART3_RX I2C2_SDA/I2C2_SCL	EXTI10
31	-	-	PA11	I/O	FT	CM0_TXEV UART1_TX/UART1_RX TIM1_CH4 TIM16_CH1 SPI1_MOSI/I2S1_SD I2C2_SCL/I2C2_SDA SPI2_MISO/I2S2_MCK	EXTI11
32	23	23	PA13/SWDIO (SWDIO)	I/O	FT	SWDIO IRTIM_IROUT TIM2_CH1_ETR TIM17_CH1	EXTI13 SWDIO CKI_2

LQFP44	LQFP32	QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-Tolerant(3)	Alternate Function	Additional Function
						SPI1_SCK/I2S1_CK SPI2_MOSI/I2S2_SD I2C1_SCL/I2C1_SDA I2C2_SCL/I2C2_SDA	
33	-	-	PF7/AIN12 (PF7)	I/O	FT	TIM1_CH2 I2C1_SDA/I2C1_SCL I2C2_SDA/I2C2_SCL	EXTI7 AIN12
34	24	24	PA14/SWCLK/AIN13 (SWCLK)	I/O	FT	SWCLK UART1_TX/UART1_RX TIM1_CH1 I2C1_SDA/I2C1_SCL I2C2_SDA/I2C2_SCL SPI2_MISO/I2S2_MCK UART3_TX/UART3_RX UART2_TX/UART2_RX	EXTI14 AIN13 SWCLK CKI_3
35	-	-	PA15/AIN14 (PA15)	I/O	FT	SPI1_NSS/I2S1_WS UART1_RX/UART1_TX TIM2_CH1_ETR CM0_TXEV I2C1_SCL/I2C1_SDA SPI2_MOSI/I2S2_SD UART2_RX/UART2_TX	EXTI15 AIN14
36	-	-	PB3/AIN15 (PB3)	I/O	FT	SPI1_SCK/I2S1_CK CM0_TXEV TIM2_CH2 SPI2_MISO/I2S2_MCK UART1_TX/UART1_RX I2C1_SDA/I2C1_SCL RCC_MCO	EXTI3 AIN15
37	25	25	PB4/AIN16 (PB4)	I/O	FT	SPI1_MISO/I2S1_MCK TIM3_CH1 CM0_TXEV TIM1_BKIN IRTIM_IROUT TIM17_BKIN SPI2_SCK/I2S2_CK I2C1_SCL/I2C1_SDA RCC_MCO	EXTI4 AIN16
38	26	26	PB5/AIN17 (PB5)	I/O	FT	SPI1_MOSI/I2S1_SD TIM3_CH2 TIM16_BKIN I2C1_SMBA TIM1_CH1 SPI2_SCK/I2S2_CK I2C2_SCL/I2C2_SDA UART1_RX/UART1_TX UART2_RX/UART2_TX UART3_RX/UART3_TX	EXTI5 AIN17
39	27	27	PB6/AIN18 (PB6)	I/O	FT	UART1_TX/UART1_RX I2C1_SCL/I2C1_SDA TIM16_CH1N TIM2_CH3 TIM3_CH1	EXTI6 AIN18
40	28	28	PB7/AIN19 (PB7)	I/O	FT	UART1_RX/UART1_TX I2C1_SDA/I2C1_SCL TIM17_CH1N TIM2_CH2	EXTI7 AIN19
41	29	29	PF9/AIN20 (PF9)	I/O	FT	TIM1_CH3 TIM2_CH1_ETR	EXTI9 AIN20

LQFP44	LQFP32	QFN32	Pin Name (default function after resets)	Pin Type(1)	5 V-Tolerant(3)	Alternate Function	Additional Function
						IRTIM_IROUT	
42	30	30	PF8/BOOT0/AIN21 (BOOT0(4))	I/O	FT	TIM1_CH2 TIM14_CH1 SPI2_SCK/I2S2_CK I2C2_SCL/I2C2_SDA UART2_RX/UART2_TX UART3_TX/UART3_RX	EXTI8 BOOT0 AIN21
43	31	31	PB8/AIN22 (PB8)	I/O	FT	TIM1_CH1 I2C1_SCL/I2C1_SDA TIM16_CH1 UART2_TX/UART2_RX UART3_RX/UART3_TX	EXTI8 AIN22
44	32	32	PB9/AIN23 (PB9)	I/O	FT	IRTIM_IROUT I2C1_SDA/I2C1_SCL TIM17_CH1 CM0_TXEV TIM1_CH4 SPI2_NSS/I2S1_WS	EXTI9 AIN23

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). NC: not connected.

(3). FT: 5 V-tolerant.

(4). By default, the Boot0 pin has a 50 kΩ pull-down resistor.

(5). The RX and TX pin functions of UART1/2/3 can be exchanged by using the software, so do the SDA and SCL pin functions of I2C1/2.

Note:

- Unless otherwise specified, all I/Os are configured in input floating mode during and after resets.
- For details about alternate functions, see section "6.5 Alternate function table".

6.5 Alternate function table

Table 6-2 Alternate function table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10~AF14	AF15
PA0	-	-	TIM2_CH1_ETR	-	UART1_RX/ UART1_TX (1)	-	-	-	-	-	-	-
PA1	CM0_TXEV	-	TIM2_CH2	-	UART1_TX/ UART1_RX (1)	TIM15_CH1N	-	-	-	-	-	-
PA2	TIM15_CH1	UART1_TX/ UART1_RX	TIM2_CH3	UART2_TX/ UART2_RX	-	-	-	-	-	-	-	-
PA3	TIM15_CH2	UART1_RX/ UART1_TX	TIM2_CH4	UART2_RX/ UART2_TX	-	I2C1_SCL/ I2C1_SDA (1)	I2C2_SCL/ I2C2_SDA	-	-	-	-	-
PA4	SPI1_NSS/ I2S1_WS	-	-	-	TIM14_CH1	I2C1_SDA/ I2C1_SCL (1)	I2C2_SDA/ I2C2_SCL	-	-	-	-	-
PA5	SPI1_SCK/ I2S1_CK	-	TIM2_CH1_ETR	I2C1_SDA/ I2C1_SCL	UART1_TX	-	I2C2_SDA/ I2C2_SCL	-	-	-	-	-
PA6	SPI1_MISO/ SPI1_MCK	TIM3_CH1	TIM1_BKIN	I2C1_SCL/ I2C1_SDA	-	TIM16_CH1	CM0_TXEV	-	-	-	-	-
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	IRTIM_IROUT	TIM14_CH1	TIM17_CH1	CM0_TXEV	-	-	-	-	RCC_MCO
PA8	RCC_MCO	TIM3_CH1	TIM1_CH1	CM0_TXEV	IRTIM_IROUT	SPI1_SCK/ I2S1_CK	I2C1_SDA/ I2C1_SCL	I2C2_SDA/ I2C2_SCL	-	-	-	-
PA9	TIM15_BKIN	UART1_TX/ UART1_RX	TIM1_CH2	SPI1_MISO/ SPI1_MCK	I2C1_SCL/ I2C1_SDA	RCC_MCO	SPI2_MOSI/ I2S2_SD	UART3_RX/ UART3_TX	I2C2_SCL/ I2C2_SDA	TIM14_CH1	-	-
PA10	TIM17_BKIN	UART1_RX/ UART1_TX	TIM1_CH3	SPI1_MOSI/ I2S1_SD	I2C1_SDA/ I2C1_SCL	TIM15_CH1	SPI2_SCK/ I2S2_CK	UART3_TX/ UART3_RX	I2C2_SDA/ I2C2_SCL	-	-	-
PA11	CM0_TXEV	UART1_TX/ UART1_RX	TIM1_CH4	TIM16_CH1	SPI1_MOSI/ I2S1_SD	I2C2_SCL/ I2C2_SDA	SPI2_MISO/ SPI2_MCK	-	-	-	-	-
PA13	SWDIO	IRTIM_IROUT	TIM2_CH1_ETR	TIM17_CH1	SPI1_SCK/ I2S1_CK	SPI2_MOSI/ I2S2_SD	I2C1_SCL/ I2C1_SDA	I2C2_SCL/ I2C2_SDA	-	-	-	-
PA14	SWCLK	UART1_TX/ UART1_RX	TIM1_CH1	I2C1_SDA/ I2C1_SCL	I2C2_SDA/ I2C2_SCL	SPI2_MISO/ SPI2_MCK	UART3_TX/ UART3_RX	UART2_TX/ UART2_RX	-	-	-	-
PA15	SPI1_NSS/ I2S1_WS	UART1_RX/ UART1_TX	TIM2_CH1_ETR	CM0_TXEV	I2C1_SCL/ I2C1_SDA	SPI2_MOSI/ I2S2_SD	-	UART2_RX/ UART2_TX	-	-	-	-
PB0	CM0_TXEV	TIM3_CH3	TIM1_CH2N	SPI1_NSS/ I2S1_WS	-	-	-	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	SPI1_MOSI/ I2S1_SD	SPI2_MOSI/ I2S2_SD	-	-	-	-	-	-	-
PB2	TIM1_ETR	-	-	SPI1_MISO/ SPI1_MCK	SPI2_MISO/ SPI2_MCK	I2C1_SDA/ I2C1_SCL	I2C2_SDA/ I2C2_SCL	-	-	-	-	I2C2_SMBA
PB3	SPI1_SCK/ I2S1_CK	CM0_TXEV	TIM2_CH2	SPI2_MISO/ SPI2_MCK	UART1_TX/ UART1_RX	I2C1_SDA/ I2C1_SCL	RCC_MCO	-	-	-	-	-
PB4	SPI1_MISO/ SPI1_MCK	TIM3_CH1	CM0_TXEV	TIM1_BKIN	IRTIM_IROUT	TIM17_BKIN	SPI2_SCK/ I2S2_CK	I2C1_SCL/ I2C1_SDA	-	-	-	RCC_MCO
PB5	SPI1_MOSI/	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	TIM1_CH1	SPI2_SCK/	I2C2_SCL/	UART1_RX/	UART2_RX/	UART3_RX/	-	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10~AF14	AF15
	I2S1_SD					I2S2_CK	I2C2_SDA	UART1_TX	UART2_TX	UART3_TX		
PB6	UART1_TX/ UART1_RX	I2C1_SCL/ I2C1_SDA	TIM16_CH1N	TIM2_CH3	TIM3_CH1	-	-	-	-	-	-	-
PB7	UART1_RX/ UART1_TX	I2C1_SDA/ I2C1_SCL	TIM17_CH1N	TIM2_CH2	-	-	-	-	-	-	-	-
PB8	TIM1_CH1	I2C1_SCL/ I2C1_SDA	TIM16_CH1	-	-	UART2_TX/ UART2_RX	UART3_RX/ UART3_TX	-	-	-	-	-
PB9	IRTIM_IROUT	I2C1_SDA/ I2C1_SCL	TIM17_CH1	CM0_TXEV	TIM1_CH4	SPI2_NSS/ I2S2_WS	-	-	-	-	-	-
PB10	SPI1_SCK/ I2S1_CK	I2C1_SCL/ I2C1_SDA	TIM2_CH3	I2C2_SCL/ I2C2_SDA	TIM1_CH3	SPI2_SCK/ I2S2_CK	UART3_TX/ UART3_RX	-	-	-	-	-
PB13	SPI1_SCK/ I2S1_CK	-	TIM1_CH1N	SPI2_MOSI/ I2S2_SD	-	I2C2_SCL/ I2C2_SDA	-	-	-	-	-	-
PB14	SPI1_MISO/ SPI1_MCK	TIM15_CH1	TIM1_CH2N	TIM3_CH1	UART1_TX/ UART1_RX	I2C2_SDA/ I2C2_SCL	SPI2_MISO/ SPI2_MCK	-	-	-	-	-
PB15	SPI1_MOSI/ I2S1_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	UART1_RX/ UART1_TX	TIM2_CH1_ETR	SPI2_MOSI/ I2S2_SD	-	-	-	-	-
PF0	TIM14_CH1	I2C1_SDA/ I2C1_SCL	-	-	-	-	-	-	-	-	-	-
PF1	TIM3_CH1	I2C1_SCL/ I2C1_SDA	-	-	-	-	-	-	-	-	-	-
PF7	TIM1_CH2	I2C1_SDA/ I2C1_SCL	I2C2_SDA/ I2C2_SCL	-	-	-	-	-	-	-	-	-
PF8	TIM1_CH2	TIM14_CH1	SPI2_SCK/ I2S2_CK	I2C2_SCL/ I2C2_SDA	UART2_RX/ UART2_TX	UART3_TX/ UART3_RX	-	-	-	-	-	-
PF9	TIM1_CH3	TIM2_CH1_ETR	IRTIM_IROUT	-	-	-	-	-	-	-	-	-

(1). The functions of UART1/2/3 RX and TX pins can be exchanged by using the software, so do the functions of I2C1/2 SDA and SCL pins.

7 Packages

7.1 Package outlines

7.1.1 LQFP44

LQFP44 is a 10 mm × 10 mm, 0.8 mm pitch package.

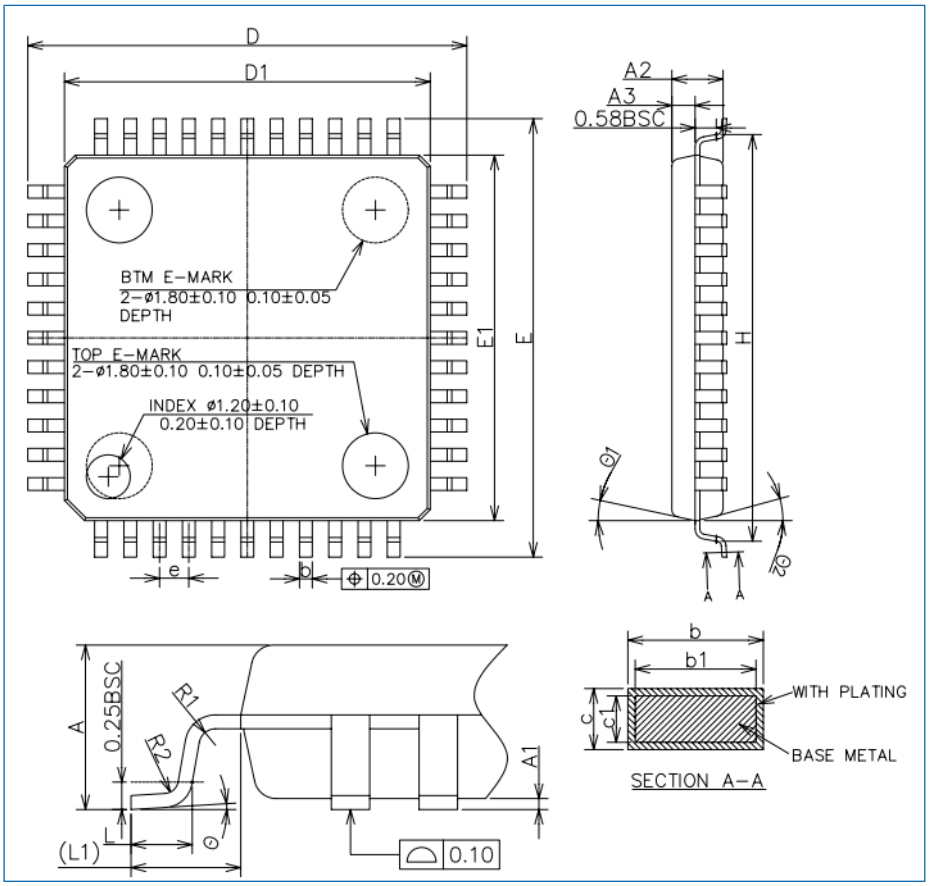

Figure 7-1 LQFP44 package outline

Table 7-1 LQFP44 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches) (1)	Max (inches) (1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	11.95	12.00	12.05	0.4705	0.4724	0.4744
D1	9.9	10.00	10.10	0.3898	0.3937	0.3976
E	11.95	12.00	12.05	0.4705	0.4724	0.4744
E1	9.90	10.00	10.10	0.3898	0.3937	0.3976
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	11.09	11.13	11.17	0.4366	0.4382	0.4398
L	0.53	-	0.70	0.0209	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	-	0.15	-	-	0.0059	-
R2	-	0.13	-	-	0.0051	-
θ	0°	3.5°	7°	0.0079	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP32

LQFP32 is a 7 mm × 7 mm, 0.8 mm pitch package.

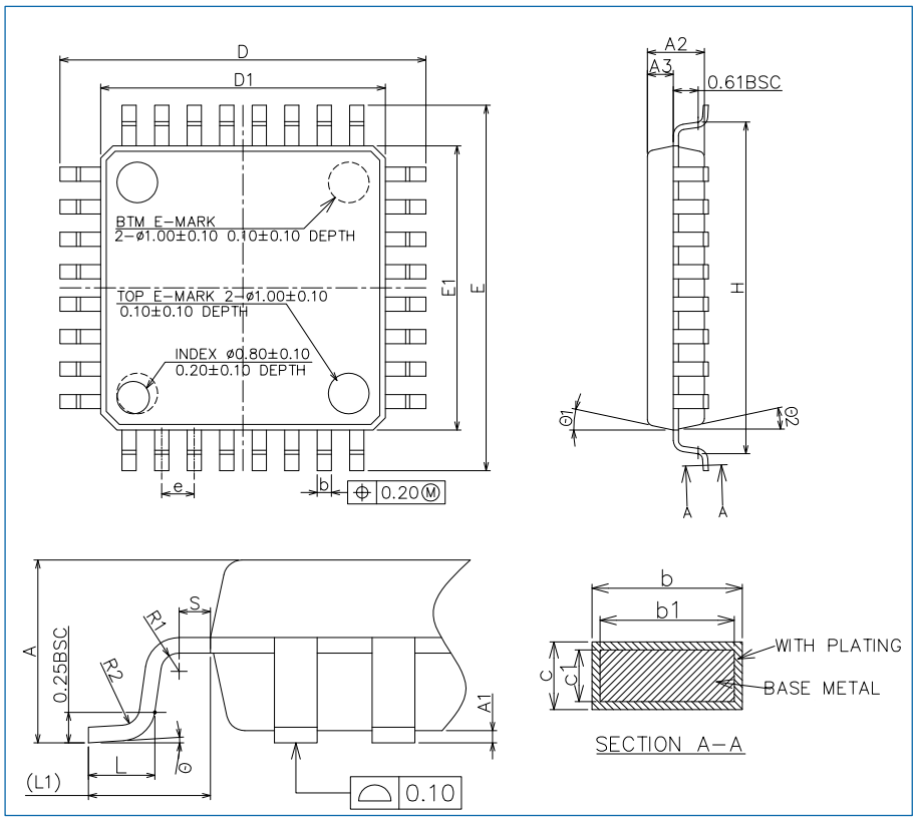

Figure 7-2 LQFP32 package outline

Table 7-2 LQFP32 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)	Min (inches) (1)	Typ (inches) (1)	Max (inches) (1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.3 QFN32

QFN32 is a 5 mm × 5 mm, 0.5 mm pitch package.

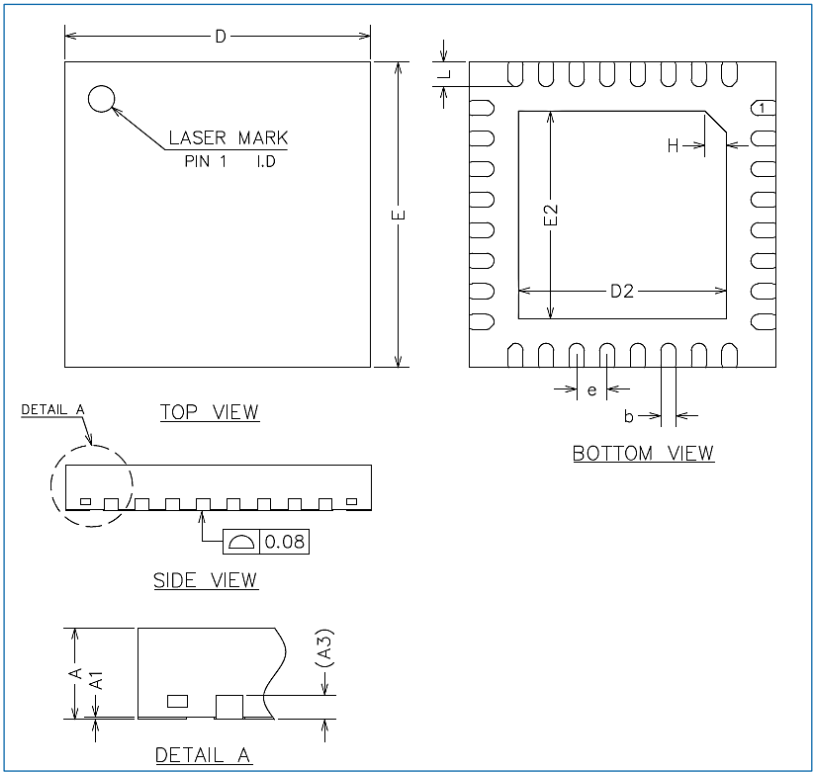

Figure 7-3 QFN32 package outline

Table 7-3 QFN32 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20REF(1)		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
e	0.40	0.50	0.60
H	0.35REF		
L	0.30	0.40	0.50

(1). REF indicates a reference value.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-4 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP44 marking

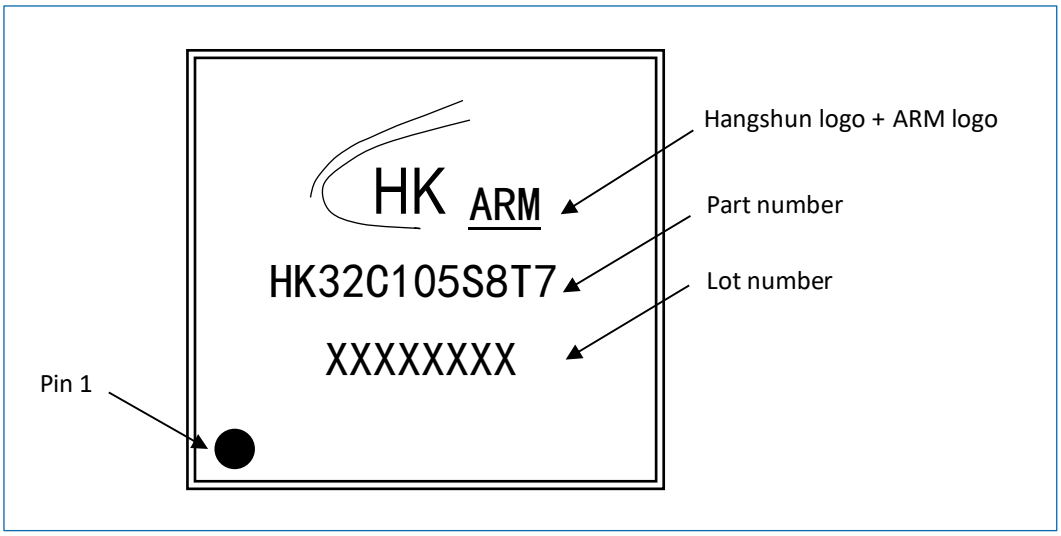

Figure 7-4 LQFP44 marking example

7.2.2 LQFP32 marking

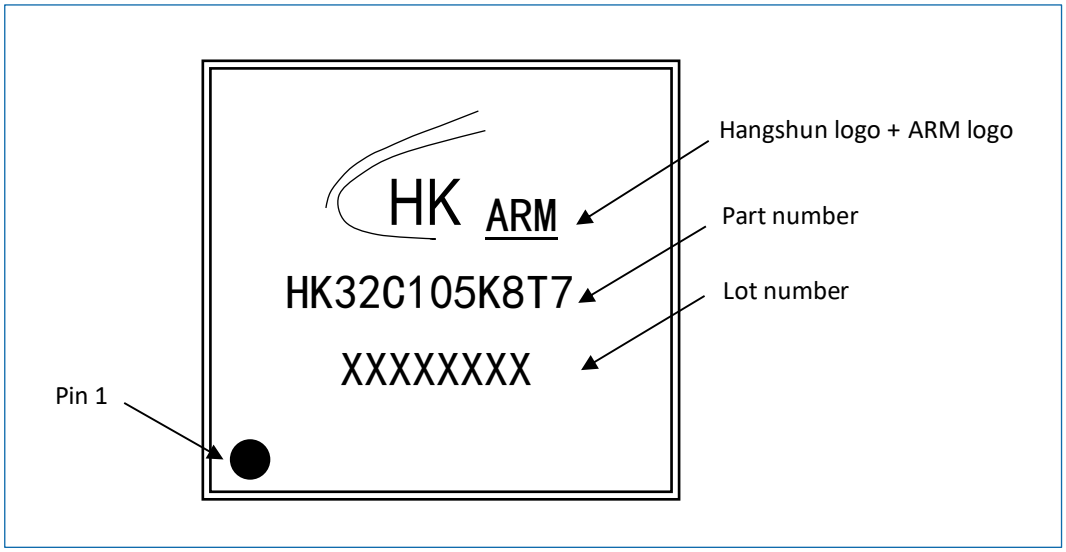

Figure 7-5 LQFP32 marking example

7.2.3 QFN32 marking

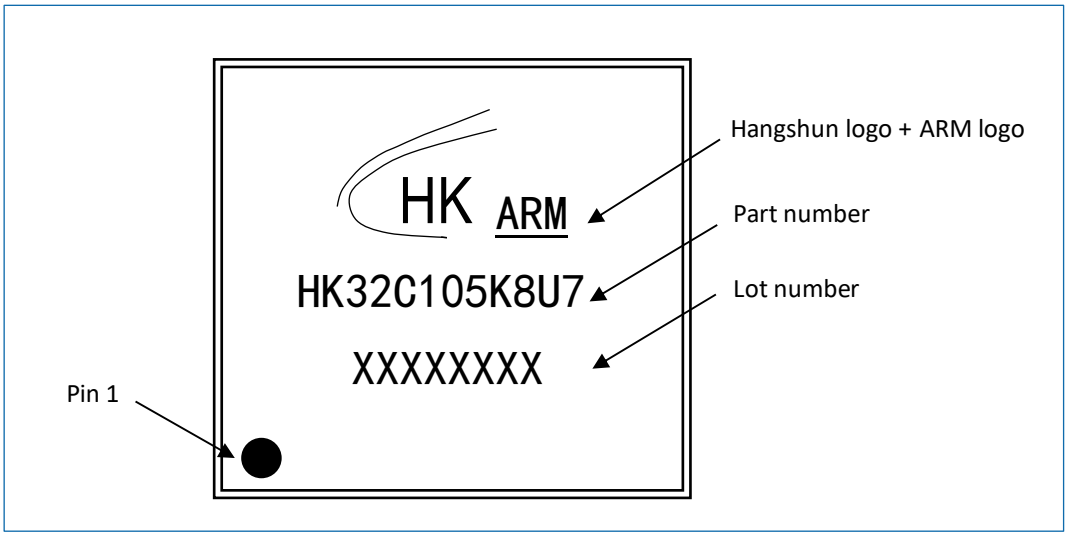

Figure 7-6 QFN32 marking example

8 Ordering information

8.1 Device numbering conventions

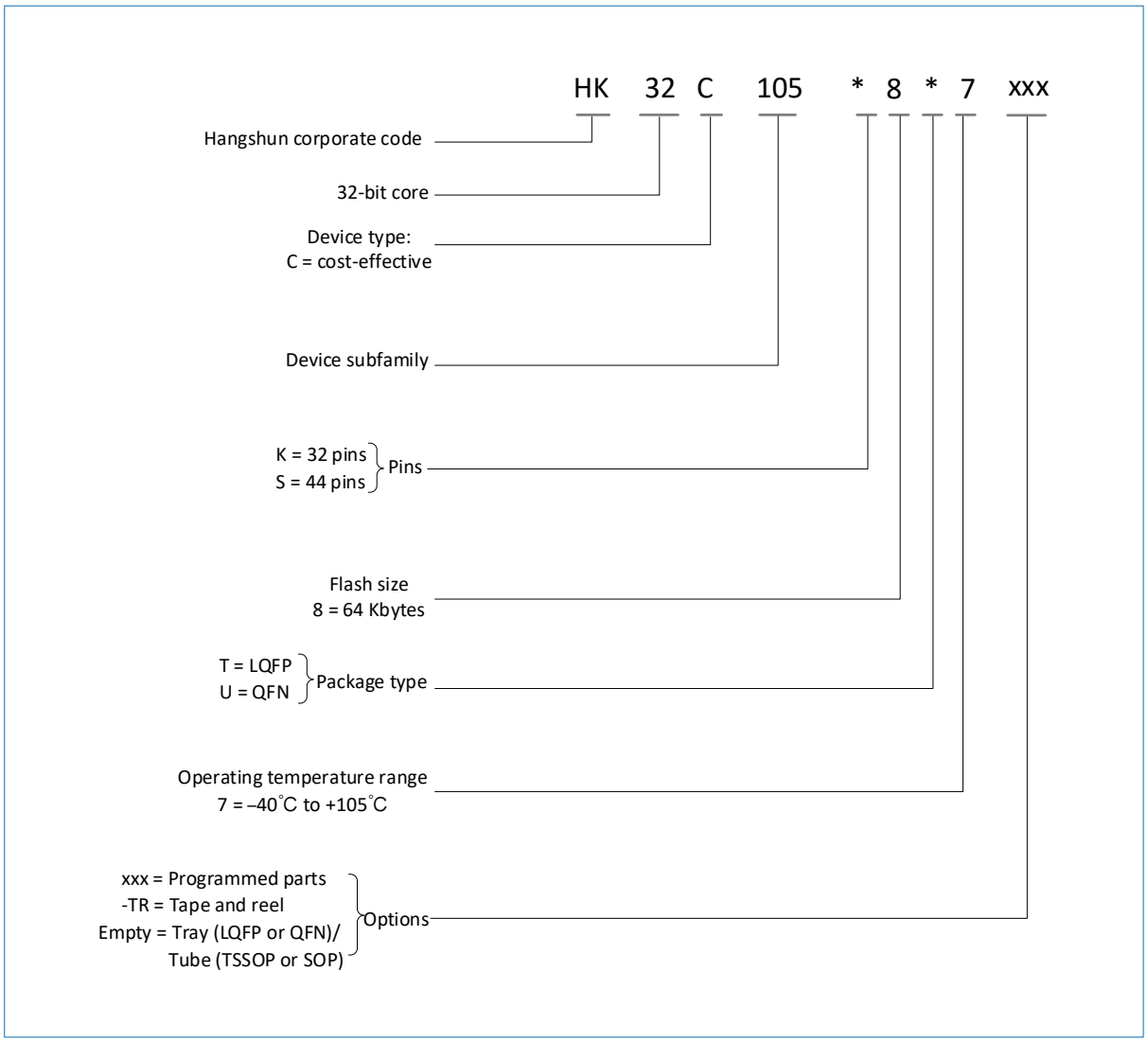

Figure 8-1 Device numbering conventions

8.2 Packaging information

Table 8-1 HK32C105 packaging information

Package	Part Number	Shipping Option	Remarks
LQFP44	HK32C105S8T7	Tray	
LQFP44	HK32C105S8T7-TR	Tape and reel	
LQFP32	HK32C105K8T7	Tray	
LQFP32	HK32C105K8T7-TR	Tape and reel	
QFN32	HK32C105K8U7	Tray	
QFN32	HK32C105K8U7-TR	Tape and reel	

9 Acronyms and glossary

9.1 Acronyms

Term	Full Name
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOR	Brown-out Reset
GPIO	General-purpose Input/Output
HSI	High-speed Internal (clock signal)
IAP	In-application Programming
ICP	In-circuit Programming
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
OBL	Option Byte Loading
PGA	Programmable Gain Amplifier
SWD	Serial Wire Debug

9.2 Glossary

Name	Description
Byte	One byte equals 8 bits of data.
Half word	One half word equals 16 bits of data or instructions.
Option byte	The option byte is the MCU configuration bytes stored in Flash.
Word	One word equals 32 bits of data or instructions.

10 Legal and contact information


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