HK32AUTO39A-3A Datasheet

Version: 1.2

Release Date: 2023-11-08

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32AUTO39A-3A series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32AUTO39A-3A.

Audience

This document is intended for:

- HK32AUTO39A-3A developers
- HK32AUTO39A-3A testers
- HK32AUTO39A-3A users

Release Notes

This document is applicable to HK32AUTO39A-3A series MCUs.

Revision History

Version	Date	Description
1.0	2023/10/13	The initial release.
1.1	2023/10/27	1. Changed the abbreviation of voltage comparator from VC to COMP. 2. Deleted the option byte loading reset from Figure 3-3 Reset circuitry. 3. Updated the alternate function description in section "6.4 Pin description".
1.2	2023/11/08	Updated the operating temperature in Table 2-1 HK32AUTO39A-3A series features.

Contents

1 Introduction

This document is the datasheet for HK32AUTO39A-3A series MCUs. HK32AUTO39A-3A is a family of automotive MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32AUTO39A-3ACET7 (LQFP48)
- HK32AUTO39A-3ACET3 (LQFP48)
- HK32AUTO39A-3ARET3 (LQFP64)
- HK32AUTO39A-3AVET3 (LQFP100)

For more details of HK32AUTO39A-3A, see *HK32AUTO39A-3A User Manual*.

2 Product overview

HK32AUTO39A-3A adopts the ARM® Cortex®-M3 core operating at a maximum frequency of 120 MHz and provides 1-Kbyte L1 cache for instructions. Hangshun's proprietary coprocessing arithmetic logic unit (COALU) embedded in HK32AUTO39A-3A can realize the effect of most arithmetic instructions supported by ARM® Cortex®-M4, including the calculation of 32-bit single-precision floating-point numbers. Additionally, COALU supports a variety of 32-bit and 64-bit customized arithmetic operations.

HK32AUTO39A-3A embeds large-capacity memories, including 527 Kbytes of Flash, 64 Kbytes of SRAM, 32 Kbytes of core-coupled SRAM, and 1 Kbyte of cache. Up to 1 Gbyte of external static memory can be connected to HK32AUTO39A-3A via the flexible static memory controller (FSMC) module. 256 Mbytes of the external static memory are used to store instructions and can be used by the internal 1-Kbyte cache for instructions. Additionally, 256 Mbytes of NOR Flash memory can be connected to HK32AUTO39A-3A via the quad serial peripheral interface (QSPI) module. The NOR Flash memory is used to store instructions and can be used by the internal 1-Kbyte cache for instructions.

HK32AUTO39A-3A incorporates the advanced encryption standard (AES) module, hash module, and true random number generator (TRNG), which are used for data encryption, data decryption, and digital signatures. The built-in cyclic redundancy check (CRC) module is used to check data integrity.

With its embedded digital camera memory interface (DCMI), four thin film transistor (TFT) interfaces, and two direct memory access (DMA) modules (12 DMA channels in total), HK32AUTO39A-3A MCUs provide a solution for capturing, processing, and displaying digital images and videos.

The serial audio interface (SAI) embedded in HK32AUTO39A-3A ensures its compliance with most audio interface protocols.

HK32AUTO39A-3A has up to two 16-bit advanced pulse width modulation (PWM) timers (eight PWM output channels in total, six of which have complementary PWM outputs with programmable inserted dead-times), four 16-bit general-purpose PWM timers (16 PWM output channels in total), and two 16-bit basic timers. The two advanced timers are connected to the embedded four voltage comparators (COMPs) on chip. In motor solutions, additional voltage comparators and related circuitry on the circuit board are not required.

HK32AUTO39A-3A provides an independent V_{BAT} power domain. When the main V_{DD} power supply is powered off, the real-time clock (RTC) can be powered from V_{BAT}.

HK32AUTO39A-3A integrates various analog circuits: three 12-bit ADCs (a total of 25 analog signal input channels: two channels for weak drive signal inputs and one channel for 5 V high-voltage signal inputs), two 12-bit DACs, one temperature sensor, one 0.8 V internal reference voltage, one low voltage detector (LVD), one power-on reset (POR)/power-down reset (PDR) circuit, and one V_{BAT} resistor voltage divider (the output of the divider is connected to the ADC on the chip).

HK32AUTO39A-3A supports multiple power consumption modes. In the lowest-power consumption mode, the typical leakage current is less than 100 nA.

HK32AUTO39A-3A MCUs are delivered in 48-pin, 64-pin, and 100-pin packages. The peripherals vary based on the package type.

HK32AUTO39A-3A has diverse peripherals and is suitable for automotive electronics applications.

2.1 Features

- ARM® Cortex®-M3 core
  - Maximum frequency: 120 MHz
  - 24-bit SysTick timer
- Operating voltage range
  - Main power supply (V_{DD}): 2.0 V to 3.6 V; backup power supply (V_{BAT}): 1.8 V to 3.6 V

- When the main power supply V_{DD} is powered off, the RTC can be powered from V_{BAT}.
- When the main power supply V_{DD} is powered off, V_{BAT} supplies power to 86-byte backup registers.

- V_{DD} typical operating current
  - Dynamic power consumption in Run mode: 19.34 mA@120 MHz@3.3 V
  - Static power consumption in Sleep mode: 5.65 mA@120 MHz@3.3 V (Wakeup time: one clock period)
  - Static power consumption in Stop mode:
    - LDO operating at full speed: 303 µA@3.3 V
    - LDO in the low-power state: 89.47 µA@3.3 V (Wakeup time: 10 µs)
  - Static power consumption in Standby mode: 3.36 µA@3.3 V (Wakeup time: 150 µs)
  - Static power consumption in Shutdown mode: 0.09 µA@3.3 V (Wakeup time: 200 µs)
- V_{BAT} typical operating current (V_{DD} powered off)
  - V_{BAT} power consumption: 2.67 µA @3.3 V (RTC enabled)
  - V_{BAT} power consumption: 2.19 µA@3.3 V (RTC disabled, backup registers retained)
- Coprocessing arithmetic logic unit (COALU)
  - Realizes the same effect as most of the arithmetic instructions supported by ARM® Cortex®-M4
  - Calculation of 32-bit single-precision floating-point numbers
  - A variety of 32-bit and 64-bit customized arithmetic operations
- DMA controller
  - Two independent DMA controllers: DMA1 and DMA2
  - DMA1 provides seven channels
  - DMA2 provides five channels
  - Can be triggered by the timer, ADC, SPI, I2C, or USART
- Memory
  - 527-Kbyte Flash memory, including the 512-Kbyte main Flash and 15-Kbyte information block. When the CPU frequency is 24 MHz or lower, there are no wait states to access Flash. The security protection function provides separate read and write protection for Flash code.
  - 1-Kbyte cache for storing CPU instructions
  - 64-Kbyte SRAM and 32-Kbyte CCM SRAM
  - 1 Gbyte of external memory (NOR/PSRAM/NAND/PC Card) via the FSMC module, of which 256 Mbytes are used to store instructions and can be used by the internal cache
  - 256 Mbytes of external NOR Flash memory via the QSPI module. The NOR Flash memory is used to store instructions and can be used by the internal cache.
  - Embedded encryption and decryption functions for instructions. Instructions are stored as ciphertext on internal and external memories.
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): 56 MHz/28 MHz/8 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL output clock: 120 MHz (maximum value)
- Reset
  - External pin reset

- Power reset
- Software reset
- IWDG reset and WWDG reset
- Low-power management reset

- Encryption
  - True random number generator (TRNG)
  - 128/192/256-bit AES
  - Hash (SHA-256)
  - CRC32
- Data communication interface
  - 6 × USARTs
  - 3 × SPIs (support the I2S protocol)
  - 2 × I2C
  - 1 × SDIO
  - 2 × CAN 2.0A/2.0B
  - 1 x full-speed (FS) USB
- Audio and video interface
  - 1 × digital camera interface (DCMI)
  - 4 × TFT interfaces
  - 1 × SAI, including two independent audio protocol processing modules
- Timer and PWM generator
  - Advanced PWM timers: TIM1/TIM8 (six complementary PWM output channels with programmable inserted dead-times)
  - General-purpose PWM timers: TIM2/TIM3/TIM4/TIM5 (16-bit timers)
  - Basic timers: TIM6/TIM7 (support CPU interrupts, DMA requests, and DAC conversion trigger)
- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detecting voltage
  - Rising edge and falling edge detection configurable
- On-chip analog peripherals
  - 3 × 12-bit 1 MSPS ADCs (sharing 25 analog input channels: two channels for weak drive signal inputs, one channel for 5 V high-voltage signal input); dual-ADC mode, sampling rate up to 2 MSPS
  - 2 × 12-bit DACs
  - 1 × temperature sensor
  - 1 × 0.8 V internal reference voltage
  - 1 × V_{BAT} resistor voltage divider (the output of the divider is connected to the ADC on the chip for monitoring V_{BAT} voltage)
  - 4 × voltage comparators (connected to two on-chip advanced PWM timers. In motor solutions, additional voltage comparators and related circuitry on the circuit board are not required.)
- UID
  - Each HK32AUTO39A-3A MCU provides a 96-bit UID.
- Debug and trace port
  - Dual-wire SW-DP

- Five-wire JTAG
- ARM® CoreSight™ debug components (DWT, FPB, ITM, TPIU)
- Single-wire asynchronous trace data output interface (TRACESWO)
- Four-wire synchronous trace data output interface (TRACEDO[3:0], TRACECKO)
- Customized DBGMCU debug controller (the low-power mode simulation control, debug peripheral clock control, and allocation of debug and trace interfaces)

- General-purpose input/output (GPIO)
  - 51 GPIOs in the 64-pin package/80 GPIOs in the 100-pin package
  - Each GPIO can be used as an external interrupt input
  - Built-in switchable pull-up/pull-down resistors
  - Support open-drain output
  - Support Schmitt hysteresis input
  - Configurable output drive capacity: ultra-high/high/medium/low
  - Provide up to 40 mA drive current
- Clock-calendar function provided by RTC counter in cooperation with software
- Reliability
  - Passed HBM3000V/CDM500V/MM200V/LU200mA level tests.
- Temperature range
  - Operating temperature range: –40°C to 105°C
    - HK32AUTO39A-3ACET7
  - Operating temperature range: –40°C to 125°C
    - HK32AUTO39A-3ACET3
    - HK32AUTO39A-3ARET3
    - HK32AUTO39A-3AVET3

2.2 Device overview

Table 2-1 HK32AUTO39A-3A series features

Part Number		HK32AUTO39A-3ACET7	HK32AUTO39A-3ACET3	HK32AUTO39A-3ARET3	HK32AUTO39A-3AVET3
Operating voltage		2.0 V – 3.6 V			
Backup power supply		1.8 V – 3.6 V			
Operating temperature		–40°C to 105°C	–40°C to 125°C		
CPU	Core	Cortex®-M3			
	Frequency (MHz)	120			
Package		LQFP48	LQFP48	LQFP64	LQFP100
GPIO		37	37	51	80
Memory (Kbyte)	Flash	527(1)	527(1)	527(1)	527(1)
	SRAM	64			
	Cache	1			
	CCM SRAM	32			

Part Number		HK32AUTO39A-3ACET7	HK32AUTO39A-3ACET3	HK32AUTO39A-3ARET3	HK32AUTO39A-3AVET3
DMA (Channels)		DMA1 (7 channels) + DMA2 (5 channels)			
Timer	Advanced timer (16-bit)	1	1	2	2
	General-purpose timer (16-bit)	4			
	Basic timer (16-bit)	2			
	SysTick timer	1			
	RTC	1			
	IWDG	1			
	WWDG	1			
Peripheral comm. interface	USART	6			
	I2C	2			
	SPI/I2S	3/3			
	QSPI	1			
	CAN	2			
	USB	1			
	FSMC	-(2)	-	-	1
	TFT (Interfaces)	-	-	-	1 (4)
	SDIO	-	-	1	1
Audio and video interface	DCMI	-	-	1	1
	SAI	1			
Coprocessing arithmetic logic unit (COALU)		1			
CRC		1			
Encryption	TRNG	1			
	AES	1			
	Hash	1			
ADC	ADC (Channels)	ADC1 (13) + ADC2 (12) + ADC3 (11)	ADC1 (13) + ADC2 (12) + ADC3 (11)	ADC1 (19) + ADC2 (18) + ADC3 (15)	ADC1 (19) + ADC2 (18) + ADC3 (15)
	Sampling rate	1 MSPS			
	Accuracy	Up to 12-bit			
Temperature sensor		1			
DAC (Channels)		1 (2)			
Voltage comparator (COMP)		2	2	4	4

Part Number	HK32AUTO39A-3ACET7	HK32AUTO39A-3ACET3	HK32AUTO39A-3ARET3	HK32AUTO39A-3AVET3
Programmable voltage detector (PVD)	1			
96-bit UID	1			

Note:

(1). The 527-Kbyte Flash comprises 512-Kbyte main Flash and 15-Kbyte information block.

(2). The hyphen (-) indicates that the feature is not supported.

3 Function description

3.1 Block diagram

ARM® Cortex®-M3 is a 32-bit RISC processor that provides an MCU platform featuring low power consumption and high performance. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M3 core, the HK32AUTO39A-3A family is compatible with ARM tools and software.

The block diagram of HK32AUTO39A-3AVET3 is as follows:

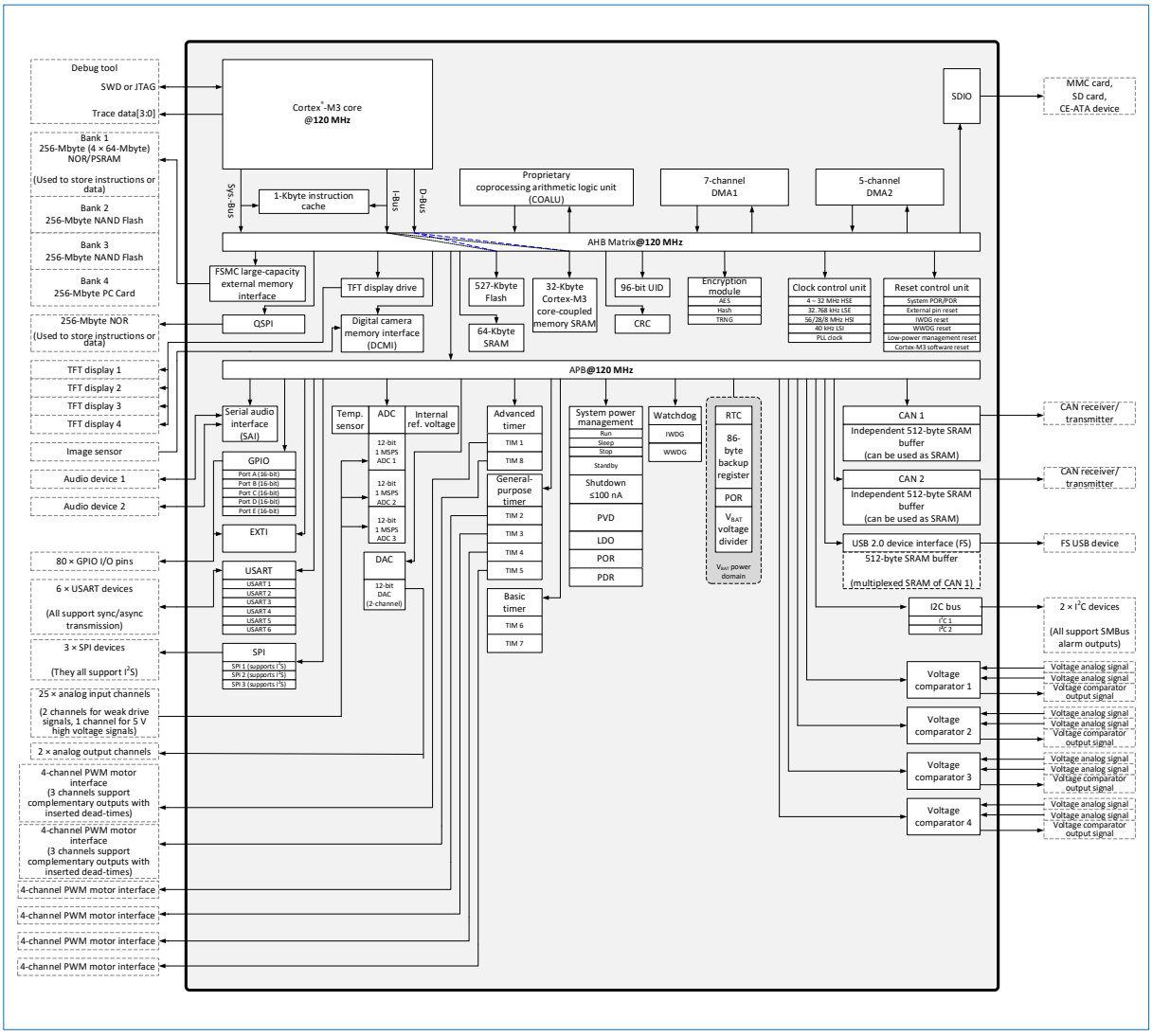

Figure 3-1 HK32AUTO39A-3AVET3 block diagram

3.2 Memory mapping

The memory mapping of HK32AUTO39A-3AVET3 is as follows:

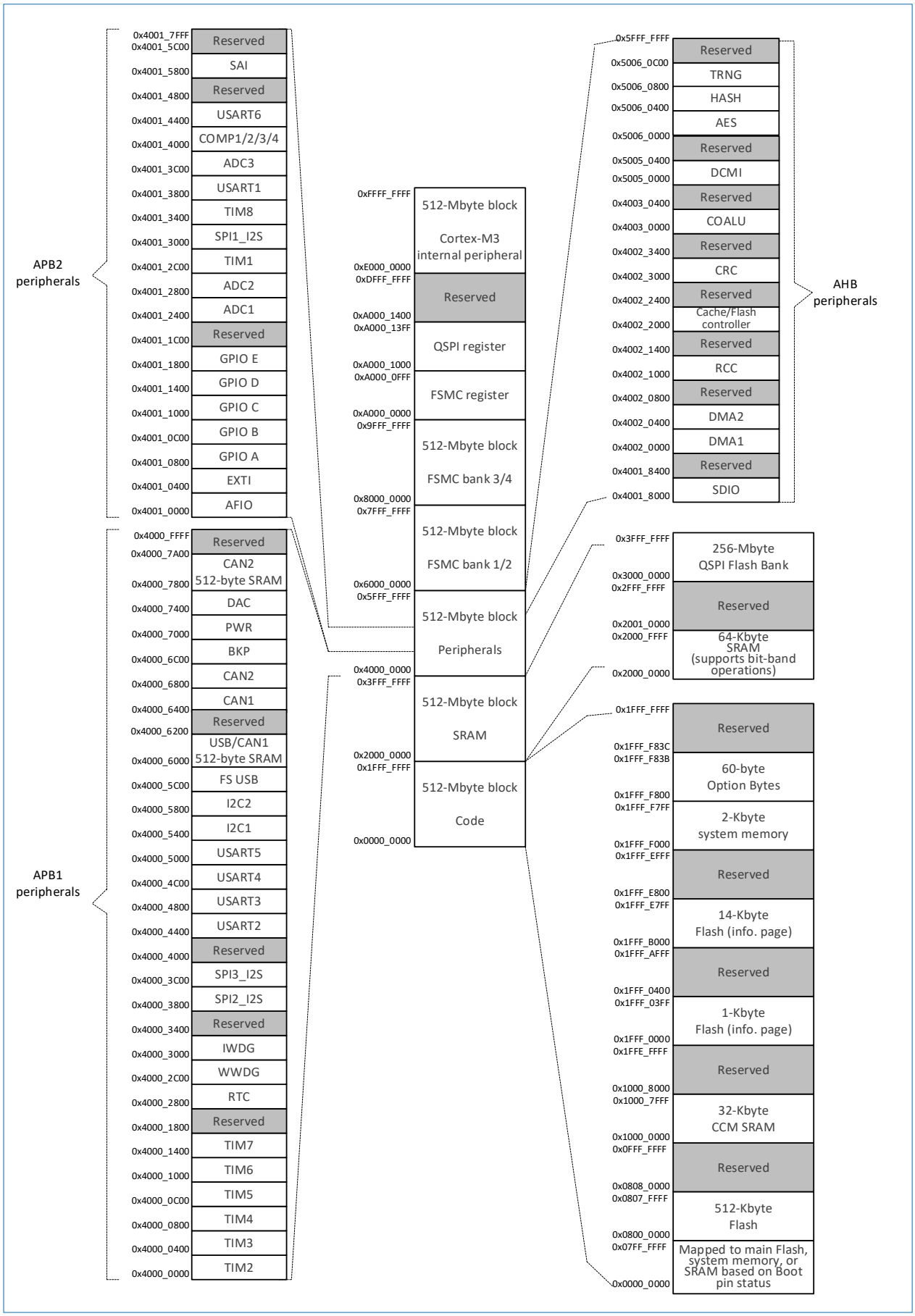

Figure 3-2 Memory mapping

3.2.1 Flash

HK32AUTO39A-3A integrates a Flash memory of up to 527 Kbytes to store programs and data. The Flash consists of a 512-Kbyte main Flash block and a 15-Kbyte information block.

- Flash data width: 128 bits, 2 Kbytes per page
- Flash access: write in half words (16 bits), words (32 bits), two words (64 bits), or four words (128 bits); read in 128 bits
- Supports Flash read/write protection.
- Integrates the instruction prefetch buffer and data buffer.
- Integrates a module for automatically encrypting and decrypting Flash instructions to protect the intellectual property (IP) of on-chip software

3.2.2 SRAM

HK32AUTO39A-3A integrates a-64 Kbyte SRAM. The SRAM can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.2.3 Cache

The device integrates 1 Kbyte of high-speed cache for storing instructions.

- 8-way set associative
- The least recently used (LRU) strategy is adopted.
- The embedded counter counts the hit rate of instructions stored in the cache.
- The cache control register can be configured to cache specific instructions. The data of one of the following instruction fetch operations can be cached at a time:
  - I-Bus instruction fetch from internal Flash
  - SYS-Bus instruction fetch from external Flash via QSPI
  - SYS-Bus instruction fetch from external Flash via FSMC

3.2.4 CCM SRAM

HK32AUTO39A-3A embeds 32 Kbytes of core-coupled memory (CCM) SRAM whose memory logic address is from 0x10000000 to 0x10007FFF. CCM SRAM can be accessed in words, half words, or bytes and is accessible from I-BUS, D-BUS, DMA1, and DMA2.

3.3 DMA

The flexible general-purpose DMAs (seven-channel DMA1 and five-channel DMA2) manage the data transfer from memories to memories, from peripherals to memories, and from memories to peripherals. The two DMAs support circular buffer management, preventing the interrupt that occurs when the DMA controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by software. The length, source, and destination of data to be transferred can be independently set by using software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, SDIO, and ADC.

3.4 COALU

Hangshun's proprietary coprocessing arithmetic logic unit (COALU) can realize the effect of most arithmetic instructions supported by ARM® Cortex®-M4, including the calculation of 32-bit single-precision floating-point numbers. Additionally, COALU supports a variety of 32-bit and 64-bit customized arithmetic operations, which makes HK32AUTO39A-3A an MCU with improved calculation capability suitable for different types of calculation.

- Fixed-point calculation
  - 64-bit/32-bit root calculation
  - 64-bit/32-bit division
  - Saturation
    - Saturated multiply accumulate
    - 32-bit saturated addition/subtraction
    - Single instruction multiple data (SIMD) saturated addition/subtraction
    - Data saturation
  - SIMD addition/subtraction
  - Half addition/subtraction result
  - Extended addition/subtraction
  - Multiply accumulate and SIMD multiply accumulate
- Floating-point calculation
  - Floating-point addition
  - Floating-point subtraction
  - Floating-point multiplication
  - Floating-point division
  - Floating-point root calculation
  - Floating-point multiply accumulate
  - Conversion between floating-point numbers and fixed-point numbers (including the conversion between 32-bit floating-point numbers and fixed-point numbers, and between 64-bit floating-point numbers and fixed-point numbers)

3.5 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32AUTO39A-3A integrates a CRC hardware calculation unit. It is used to get a CRC code from an 8-, 16-, or 32-bit data word by using a generator polynomial.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with the reference signature that is generated at link time and stored at a specified memory location.

3.6 NVIC

HK32AUTO39A-3A embeds a nested vectored interrupt controller (NVIC) to manage interrupts flexibly with the lowest interrupt latency.

- The closely coupled NVIC ensures low latency in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

The HK32AUTO39A-3A MCU has 71 external interrupts numbered from 0 to 70.

Table 3-1 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	–3	Fixed	Reset	Reset	0x0000 0004
-	–2	Fixed	NMI	Non-maskable interrupt. The RCC clock security system (CSS) is connected to the NMI vector.	0x0000 0008
-	–1	Fixed	HardFault	All classes of fault	0x0000 000C
-	0	Configurable	MemManage	Memory management	0x0000 0010
-	1	Configurable	BusFault	Pre-fetch instruction fault/Memory access fault	0x0000 0014
	2	Configurable	UsageFault	Undefined instruction and illegal state	0x0000 0018
-	-	-	-	Reserved	0x0000 001C- 0x0000 002B
-	3	Configurable	SVCall	System service call via SWI instruction	0x0000 002C
-	4	Configurable	DebugMonitor	Debug monitor	0x0000 0030
-	-	-	-	Reserved	0x0000 0034
-	5	Configurable	PendSV	Pendable request for system service	0x0000 0038
-	6	Configurable	SysTick timer	SysTick timer	0x0000 003C
0	7	Configurable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Configurable	PVD	PVD through EXTI line 16 detection interrupt	0x0000 0044
2	9	Configurable	TAMPER	Tamper interrupt	0x0000 0048
3	10	Configurable	RTC	RTC global interrupt	0x0000 004C
4	11	Configurable	FLASH	Flash global interrupt	0x0000 0050
5	12	Configurable	RCC	RCC global interrupt	0x0000 0054
6	13	Configurable	EXTI0	EXTI line 0 interrupt	0x0000 0058
7	14	Configurable	EXTI1	EXTI line 1 interrupt	0x0000 005C
8	15	Configurable	EXTI2	EXTI line 2 interrupt	0x0000 0060
9	16	Configurable	EXTI3	EXTI line 3 interrupt	0x0000 0064
10	17	Configurable	EXTI4	EXTI line 4 interrupt	0x0000 0068
11	18	Configurable	DMA1_Channel1	DMA1 channel 1 global interrupt	0x0000 006C
12	19	Configurable	DMA1_Channel2	DMA1 channel 2 global interrupt	0x0000 0070
13	20	Configurable	DMA1_Channel3	DMA1 channel 3 global interrupt	0x0000 0074
14	21	Configurable	DMA1_Channel4	DMA1 channel 4 global interrupt	0x0000 0078
15	22	Configurable	DMA1_Channel5	DMA1 channel 5 global interrupt	0x0000 007C
16	23	Configurable	DMA1_Channel6	DMA1 channel 6 global interrupt	0x0000 0080
17	24	Configurable	DMA1_Channel7	DMA1 channel 7 global interrupt	0x0000 0084
18	25	Configurable	ADC1_2	ADC1/ADC2 global interrupt (Combined with EXTI24, EXTI25)	0x0000 0088
19	26	Configurable	USB_HP_CAN_TX	USB high priority or CAN TX interrupts	0x0000 008C
20	27	Configurable	USB_LP_CAN_RX0	USB low priority or CAN RX0 interrupts	0x0000 0090
21	28	Configurable	CAN_RX1	CAN RX1 interrupt	0x0000 0094
22	29	Configurable	CAN_SCE	CAN SCE interrupt	0x0000 0098
23	30	Configurable	EXTI9_5	EXTI line [9:5] interrupts	0x0000 009C
24	31	Configurable	TIM1_BRK	TIM1 break interrupt	0x0000 00A0
25	32	Configurable	TIM1_UP	TIM1 update interrupt	0x0000 00A4
26	33	Configurable	TIM1_TRG_COM	TIM1 trigger and COM interrupts	0x0000 00A8
27	34	Configurable	TIM1_CC	TIM1 capture/compare interrupt	0x0000 00AC
28	35	Configurable	TIM2	TIM2 global interrupt	0x0000 00B0
29	36	Configurable	TIM3	TIM3 global interrupt	0x0000 00B4
30	37	Configurable	TIM4	TIM4 global interrupt	0x0000 00B8
31	38	Configurable	I2C1_EV	I2C1 event interrupt	0x0000 00BC
32	39	Configurable	I2C1_ER	I2C1 fault interrupt	0x0000 00C0
33	40	Configurable	I2C2_EV	I2C2 event interrupt	0x0000 00C4
34	41	Configurable	I2C2_ER	I2C2 fault interrupt	0x0000 00C8

Position	Priority		Name	Description	Address
35	42	Configurable	SPI1	SPI1 global interrupt	0x0000 00CC
36	43	Configurable	SPI2	SPI2 global interrupt	0x0000 00D0
37	44	Configurable	USART1	USART1 global interrupt	0x0000 00D4
38	45	Configurable	USART2	USART2 global interrupt	0x0000 00D8
39	46	Configurable	USART3	USART3 global interrupt	0x0000 00DC
40	47	Configurable	EXTI15_10	EXTI line [15:10] interrupts	0x0000 00E0
41	48	Configurable	RTCAlarm	RTC alarm through EXTI line 17 interrupt	0x0000 00E4
42	49	Configurable	USBWakeUp	USB wake-up from standby through EXTI line 18 interrupt	0x0000 00E8
43	50	Configurable	TIM8_BRK	TIM8 break interrupt	0x0000 00EC
44	51	Configurable	TIM8_UP	TIM8 update interrupt	0x0000 00F0
45	52	Configurable	TIM8_TRG_COM	TIM8 trigger and commutation interrupts	0x0000 00F4
46	53	Configurable	TIM8_CC	TIM8 capture/compare interrupt	0x0000 00F8
47	54	Configurable	ADC3	ADC3 global interrupt (including EXTI26)	0x0000 00FC
48	55	Configurable	FSMC	FSMC global interrupt	0x0000 0100
49	56	Configurable	SDIO	SDIO global interrupt	0x0000 0104
50	57	Configurable	TIM5	TIM5 global interrupt	0x0000 0108
51	58	Configurable	SPI3	SPI3 global interrupt	0x0000 010C
52	59	Configurable	USART4	USART4 global interrupt	0x0000 0110
53	60	Configurable	USART5	USART5 global interrupt	0x0000 0114
54	61	Configurable	TIM6	TIM6 global interrupt	0x0000 0118
55	62	Configurable	TIM7	TIM7 global interrupt	0x0000 011C
56	63	Configurable	DMA2_Channel1	DMA2 channel 1 global interrupt	0x0000 0120
57	64	Configurable	DMA2_Channel2	DMA2 channel 2 global interrupt	0x0000 0124
58	65	Configurable	DMA2_Channel3	DMA2 channel 3 global interrupt	0x0000 0128
59	66	Configurable	DMA2_Channel4_5	DMA2 channel 4 and channel 5 global interrupts	0x0000 012C
60	67	Configurable	QSPI	QSPI interrupt	0x0000 0130
61	68	Configurable	DCMI	DCMI interrupt	0x0000 0134
62	69	Configurable	COALU/AES	COALU/AES interrupt	0x0000 0138
63	70	Configurable	CAN2_TX	CAN2 TX interrupt	0x0000 013C
64	71	Configurable	CAN2_RX0	CAN2 RX0 interrupt	0x0000 0140
65	72	Configurable	CAN2_RX1	CAN2 RX1 interrupt	0x0000 0144
66	73	Configurable	CAN2_SCE	CAN2 SCE interrupt	0x0000 0148
67	74	Configurable	Hash	Hash interrupt	0x0000 014C
68	75	Configurable	EXTI23_20	Voltage comparator through EXTI line [23:20] interrupts	0x0000 0150
69	76	Configurable	USART6	USART6 global interrupt	0x0000 0154
70	77	Configurable	SAI	SAI_IRQ Handler	0x0000 0158

3.7 EXTI

The extended interrupt/event controller (EXTI) is comprised of 26 edge detectors that are used to generate interrupt/event requests. EXTI0 – EXTI15 connected to I/Os

The connections of the other 10 EXTI lines are as follows:

- EXTI 16 connected to the PVD output
- EXTI 17 connected to the RTC alarm event
- EXTI 18 connected to the USB wakeup event
- EXTI 20 connected to the COMP1 output
- EXTI 21 connected to the COMP2 output
- EXTI 22 connected to the COMP3 output

- EXTI 23 connected to the COMP4 output
- EXTI 24 connected to the ADC1 AWD event
- EXTI 25 connected to the ADC2 AWD event
- EXTI 26 connected to the ADC3 AWD event

EXTI lines from EXTI 24 to EXTI 26 are used for the input of internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). EXTI lines from EXTI 24 to EXTI 26 can detect the rising edge of events in only Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system.

3.8 Resets

HK32AUTO39A-3A supports the system reset, power reset, and backup domain reset.

3.8.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain. You can identify a reset source by checking reset status flags in the RCC_CSR register.

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW Reset)
- Low-power management reset

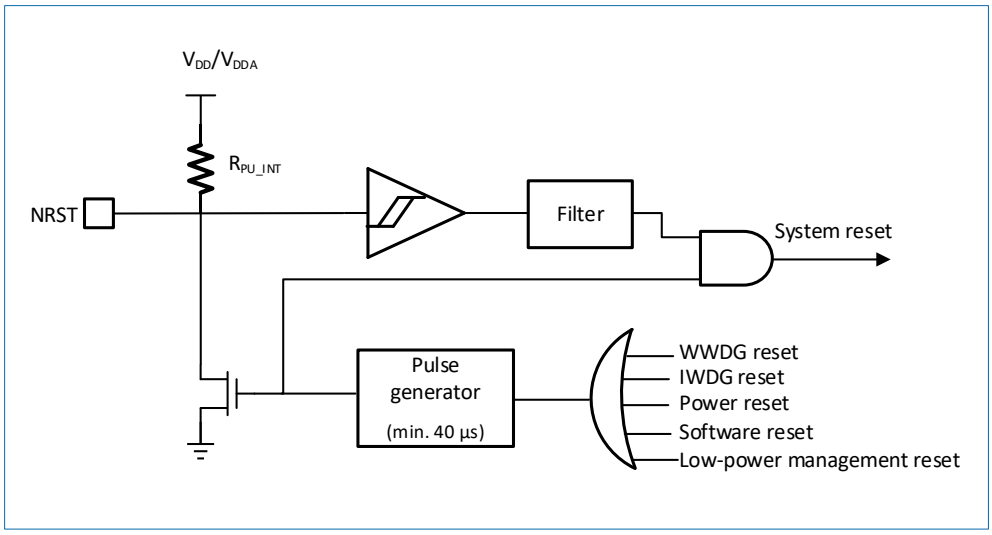

Figure 3-3 Reset circuitry

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004.

The internal reset signal is output on the NRST pin. The pulse generator guarantees a pulse duration of at least 40 µs for each internal or external reset source. When the NRST pin is pulled low and an external reset is generated, a reset pulse is generated.

3.8.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)

- Exit from Standby mode

The power reset resets all registers, except for the registers in the backup domain.

HK32AUTO39A-3A embeds the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply is over the POR/PDR threshold. When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuit is required.

3.8.3 Backup domain reset

The backup domain has two dedicated resets that only affect the backup domain. A backup domain reset is generated when one of the following events occurs:

- Software reset: Set the BDRST bit in the backup domain control register RCC_BDCR.
- V_{DD} and (or) V_{BAT} are powered on again after being powered off.

3.9 Clocks

A system clock is selected when the MCU starts. During the reset, the 8 MHz HSI is selected as the CPU clock by default, then a 4 MHz – 32 MHz HSE can be selected. If the external clock fails, it will be isolated and a corresponding interrupt will be generated.

HK32AUTO39A-3A also provides the LSI, LSE, and GPIO input as clock sources and uses the PLL to generate required clocks.

HK32AUTO39A-3A integrates a clock security system (CSS) circuit. The threshold for the detection of HSE frequency is adjustable.

3.9.1 Clock sources

Table 3-2 Clock sources

Clock	Description
HSI clock	Output frequency: 56 MHz, which can be divided into 28 MHz or 8 MHz (default value)
HSE clock	Frequency: 4 MHz to 32 MHz Supports the input of an external clock from the OSC_IN pin
PLL clock	Input frequency: 2 MHz to 80 MHz Output frequency: 16 MHz to 120 MHz
LSI clock	Frequency: 30 kHz to 60 kHz (typical value: 40 kHz)
LSE clock	Frequency: 32.768 kHz Supports the input of a 32.768 kHz external clock from the OSC32_IN pin
GPIO input clock	PA1, PB1, PC7, PB7: up to 64 MHz

3.9.2 Clock tree

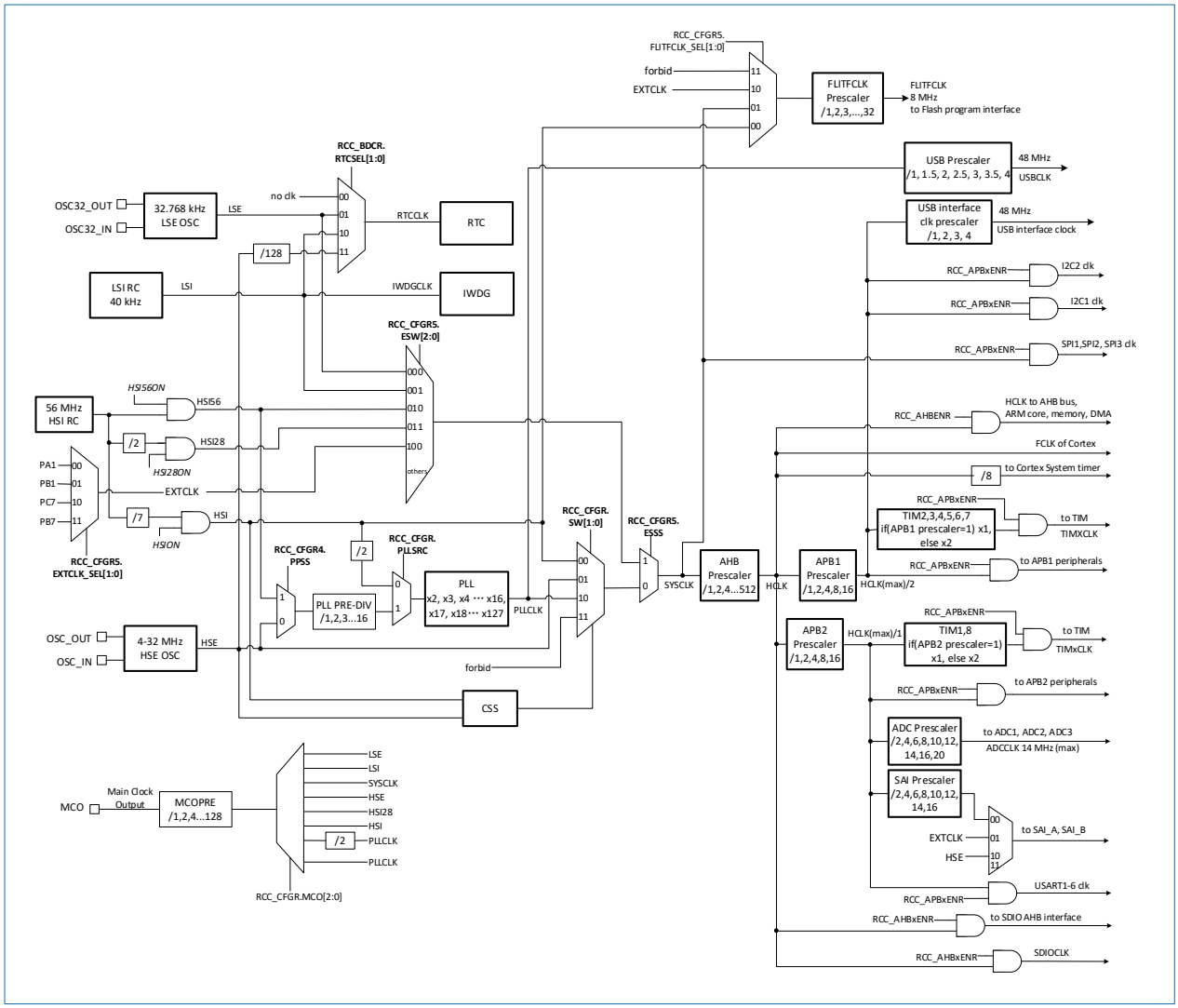

Figure 3-4 Clock tree

Note:

- PLL input clock: HSI8/2, HSI56/PREDIV, and HSE/PREDIV are available.
- SYSCLK: HSI8, HSI28, HSI56, HSE, PLL, LSI, LSE, and GPIO input clock are available. HSI (8 MHz) is the default clock.
- FLITFCLK: HSI8, GPIO input clock, and SYSCLK clock are available.

3.10 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.11 Power supply scheme

- V_{DD}: 2.0 V to 3.6 V. The V_{DD} pin supplies power to I/O pins and internal low dropout regulators (LDOs).
- V_{DDA}: 2.0 V to 3.6 V. The V_{DDA} pin supplies power to the analog circuitry, such as the ADC and temperature sensor.
- V_{BAT} = 1.8 V to 3.6 V: When V_{DD} is powered off, V_{BAT} supplies power to the RTC, external 32 kHz oscillator, and backup registers.

3.12 Power supply monitor

HK32AUTO39A-3A MCUs contain the power-on reset (POR)/power-down reset (PDR) circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the POR/PDR threshold (see Table 4-6). When V_{DD} is less than the POR/PDR threshold, the device is in the reset state and no external reset circuit is required.

HK32AUTO39A-3A integrates a programmable voltage detector (PVD). The PVD monitors the V_{DD} power supply and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated, and the interrupt program may send a warning message or set the MCU to the safe state. The PVD is enabled by setting the register.

3.13 Low-power modes

HK32AUTO39A-3A supports several low-power modes to achieve the best compromise between low power consumption, short startup time, and multiple wakeup sources.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the phase-locked loop (PLL), HSE oscillator, and HSI oscillator are disabled. The MCU can be woken up from Stop mode by any extended interrupt/event controller (EXTI) line. The EXTI line source can be any of the 16 external I/O pins, a PVD output, an RTC alarm, or a USB wakeup signal.

- Standby mode

  In Standby mode, the MCU achieves extremely low power consumption. The internal LDOs are off, so the entire 1.2 V domain is powered off. The PLL, HSI oscillator, and HSE oscillator are disabled. The SRAM content and register content are lost, except for registers in the backup domain. The Standby circuitry works as normal. MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

- Shutdown mode

  In Shutdown mode, the MCU achieves extremely low power consumption. All internal LDOs and all clock sources are off. The power supply of the backup domain is off by default (which can be configured to on). The shutdown wakeup circuitry works as normal. MCUs exit from Shutdown mode when an external reset on the NRST pin, an IWDG reset, or a rising edge on the WKUP pin occurs. By default, the power supply of the backup domain is off, so an RTC alarm cannot make the MCU exit from Shutdown mode. The power supply of the backup domain is configurable.

Table 3-3 Entry into and exit from low-power modes

Operating Mode	Entry	Exit	Core Domain Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
Sleep	1. Set PWR_CR:LPDS = 0 and PWR_CR:PDDS = 0. 2. The software executes WFI/WFE instructions.	Any IRQ interrupt/event, including SysTick.	The CPU clock is off. No impact on other clocks or the ADC clock.	On	On
Stop	1. Set PWR_CR:PDDS = 0. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions.	Any EXTI line. The MCU is pre-woken up by ADC sampling at a specified time. The real wake-up occurs when the conditions are met.	All clocks stop.	HSI and HSE oscillators are off.	On or in low-power mode (configured in PWR_CR)

Operating Mode	Entry	Exit	Core Domain Clock Status	V_{DD} Domain Clock Status	Voltage Regulator Status
Standby	1. Set PWR_CR:LPDS = 0 and PWR_CR:PDDS = 1. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions. 4. Clear the WUF bit in the Power control/status register PWR_CSR.	Three polarity-configurable external pins (WKUPx), the RTC alarm, and the IWDG reset.	All clocks stop.	HSI and HSE oscillators are off.	Off
Shutdown	1. Set PWR_CR:LPDS = 0, PWR_CR:PDDS = 1, and PWR_CSR2:SHDS = 1. 2. Set the SLEEPDEEP bit in the Cortex®-M3 system control register. 3. The software executes WFI/WFE instructions.	Three polarity-configurable external pins (WKUPx) and the RTC alarm (when the power supply of the backup domain is configured to on).	All clocks stop.	All clocks stop.	Off

3.14 RTC and BKP

The power supply to RTC and backup registers is controlled by a switch. When V_{DD} is enabled, V_{DD} supplies power to RTC and backup registers. Otherwise, V_{BAT} supplies power to RTC and backup registers.

3.14.1 RTC

The real-time clock (RTC) has a set of continuously running counters and can provide the clock calendar function via software. In addition, the real-time clock provides alarm interrupt and periodic interrupt functions.

The RTC can be driven by a 32.768 kHz external oscillator or an internal low-power RC oscillator whose typical frequency is 40 kHz. An external 512 Hz signal is used for the compensation of natural quartz deviation. The RTC has a 32-bit programmable counter for long-term measurement in conjunction with the compare register. A 20-bit prescaler is used for the time base clock. By default, the prescaler is configured to generate a time base of 1 second from a clock at 32.768 kHz.

The device has a wakeup timer for periodic wakeup.

3.14.2 BKP

Backup registers are used to store user application data. The system reset and power reset do not reset backup registers. Backup registers are not reset upon wakeup from Standby mode. HK32AUTO39A-3A provides 43 backup data registers (BKP_DR0 to BKP_DR42).

3.15 IWDG

The independent watchdog (IWDG) is based on a 12-bit down counter and an 8-bit prescaler. The IWDG is clocked from an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use IWDG in window mode. The reset initial value of the IWDG can be set through option bytes.

3.16 WWDG

The window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running

mode or used to reset the system when a problem occurs. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.17 SysTick timer

The SysTick timer is a dedicated timer of the operating system. It is a standard down counter with the following features:

- 24-bit down counter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.18 Basic timer

HK32AUTO39A-3A integrates basic timers TIM6 and TIM7. A basic timer can be used as a 16-bit generic time base or used to generate a DAC trigger signal.

3.19 General-purpose timer

Every general-purpose timer (TIM2/TIM3/TIM4/TIM5) provides a 16-bit auto-reload up/down counter, a 16-bit prescaler, and four independent channels. Every channel can be used for input capture, output compare, PWM output, and one-pulse mode output. The general-purpose timers can work with the advanced timer through the Timer Link feature for synchronization and event chaining. In debug mode, the counter can be frozen.

The general-purpose timers (except for TIM3) can be used to trigger DAC.

Every general-purpose timer can generate PWM outputs and has an independent DMA request mechanism.

The four input channels of TIM2/TIM3/TIM4/TIM5 support triggering on the rising edge, falling edge, or both.

3.20 Advanced timer

HK32AUTO39A-3A integrates the advanced timers TIM1 and TIM8. Each timer can be deemed as a three-phase PWM generator with six channels that have complementary PWM outputs with programmable inserted dead-times. The advanced timer can also be used as a complete general-purpose timer. The four independent channels of the advanced timer can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). In debug mode, the counter can be frozen. Many functions of the advanced timers are the same as those of general-purpose timers, and the two types of timers have the same structure. Therefore, the advanced timers can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

Only TIM8 can trigger the DAC.

TIM1 and TIM8 have the following functions:

- CCER[15]: CC4NP bit in the TIM_CCER register for inputting triggers on the rising and falling edges
- CR1[15]: ETR_CLR_SEL bit in the TIM_CR1 register for selecting an external pin or the voltage comparator COMP4 to clear PWM outputs.
- CR1[14]: BRK_SEL bit in the TIM_CR1 register for selecting an external pin or the voltage comparator COMP1/2/3 to output PWM breaks.

- The four input channels of TIM1 and TIM8 support triggering on the rising edge, falling edge, or both.

3.21 USART

HK32AUTO39A-3A embeds six universal synchronous/asynchronous receivers/transmitters (USART1/USART2/USART3/USART4/USART5/USART6). These interfaces provide asynchronous communications, IrDA SIR ENDEC support, multi-processor communications, single-wire half-duplex communications, and LIN Master/Slave capability.

USART1 and USART6 interfaces can communicate at a speed of up to 7.5 Mbit/s. USART2, USART3, USART4, and USART5 interfaces communicate at a speed of up to 3.75 Mbit/s. All the USART interfaces provide hardware management of the CTS and RTS signals, Smart Card mode (compliant with ISO 7816), and SPI-like communication mode. All USART interfaces can be operated by using the DMA controller.

3.22 I2C

HK32AUTO39A-3A embeds two I2C bus interfaces. The I2C bus interfaces can work as a master or slave and support the standard and fast modes. The I2C interfaces support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). They have embedded hardware CRC generation/verification. They can be operated by using the DMA controller and support SMBus V2.0/PMBus.

3.23 SPI

HK32AUTO39A-3A has three serial peripheral interfaces (SPIs). In master or slave mode, the full-duplex and half-duplex communication speed is up to 18 Mbit/s. The 3-bit prescaler provides eight master mode frequencies. Each frame can be configured to 8-bit or 16-bit. The hardware CRC generation/verification supports the basic SD card and MMC mode.

All SPI interfaces can be operated by using the DMA controller.

The three SPI interfaces can operate in I2S mode. The three standard I2S interfaces can operate in master or slave mode and can be configured to operate with 16-bit or 32-bit resolution. These interfaces can also be configured as input or output channels. The supported audio sampling frequency ranges from 8 kHz to 192 kHz. If an I2S interface is configured as a master, the master clock can be output to an external DAC or CODEC at 256 times the sampling frequency.

3.24 QSPI

The quad serial peripheral interface (QSPI) is a communication interface for single, dual, or quad SPI Flash memories. The QSPI Flash interface can operate in:

- Indirect mode (directly accesses the QSPI registers)
- Status polling mode (periodically reads the external Flash memory status register)
- Memory mapping mode (the external Flash memory is mapped to the MCU address space)

Up to 256 Mbytes of external Flash can be mapped to the MCU address space. Eight-bit, 16-bit, and 32-bit data access is allowed. The execution of code is supported. The opcode and frame format are fully programmable. Single data rate (SDR) and double data rate (DDR) are supported.

3.25 CAN

HK32AUTO39A-3A has two independent controller area network (CAN) interfaces. The CAN interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN interface has three transmit mailboxes and two three-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.26 USB

HK32AUTO39A-3A embeds a USB controller that complies with the full-speed USB device standard. The USB

interface endpoint settings can be configured by using the software. It provides suspend/resume support. The dedicated 48 MHz clock for USB is generated by the internal main PLL.

3.27 FSMC

- The flexible static memory controller (FSMC) can interface with 1 Gbyte of external static memories, including:
  - Static random access memory (SRAM)
  - Read-only memory (ROM)
  - NOR Flash
  - PSRAM (four memory banks)
- Two NAND Flash memory banks with error correction code (ECC) hardware that checks up to 8 Kbytes of data
- Compatible with 16-bit PC Cards
- Supports burst mode access to synchronous memories, such as NOR Flash and PSRAM
- 8-bit or 16-bit data bus
- Independent chip select (CS) for each memory bank
- Separate configuration for each memory bank
- Supports write enable and byte lane select outputs when PSRAM and SRAM devices are used
- Translates 32-bit wide AHB transactions into consecutive 16-bit or 8-bit access to external 16-bit or 8-bit devices
- With the 2-word long write FIFO (each word is 32-bit wide), FSMC can free the AHB for other operations when data is written to slow memories. Before a new FSMC operation is started, the FIFO is drained. The FSMC inserts wait states until the current memory access is completed.
- Asynchronous wait control for external memories
- Write encryption and read decryption for 16-bit external memories
- Supports Intel 8080 mode and Motorola 6800 mode, and can flexibly connect to various LCD controllers.

3.27.1 TFT LCD interface

Some of the FSMC interfaces are thin film transistor (TFT) liquid crystal display (LCD) interfaces, which can directly drive LCDs. You can use either the TFT LCD interfaces or other FSMC interfaces (excluding TFT LCD interfaces) at a time. Four TFT LCD panels can be driven by using the FSMC interface (RGB: 5 bits for red, 6 bits for green, and 5 bits for blue). Four horizontal synchronization signals, four vertical synchronization signals, and four data enable signals of the four TFT LCD panels are output.

3.28 SDIO

A secure digital (SD)/secure digital input-output (SDIO)/MultiMediaCard (MMC) host interface is embedded in HK32AUTO39A-3A. It is compliant with MMC System Specification Version 4.2 in three different data bus modes:

- 1-bit (default)
- 4-bit
- 8-bit: In this mode, the interface allows data transfer at up to 48 MHz, and the interface is compliant with SD Memory Card Specification Version 2.0.

SD Memory Card Specification Version 2.0 supports two data bus modes: 1-bit (default) and 4-bit.

The MCU of the current version supports only one SD/SDIO/MMC 4.2 card each time but multiple cards of MMC 4.1 or earlier versions each time. In addition to SD/SDIO/MMC, this interface is compatible with the CE-ATA digital

protocol version 1.1.

3.29 DCMI

The digital camera memory interface (DCMI) is a synchronous parallel digital interface that can receive image and video data from an external CMOS camera module at a high speed.

DCMI has the following features:

- Supports various data formats: YCbCr4:2:2/RGB565 video and JPEG compressed data.
- 8-bit, 10-bit, 12-bit, or 14-bit parallel interface
- Configurable polarity for the pixel clock and synchronization signals
- Supports the sampling of continuous frames or a single frame
- Provides the automatic crop feature
- Supports frame skipping, line skipping, and pixel skipping sampling
- 8-word receive FIFO

3.30 SAI

The serial audio interface (SAI) complies with most audio interface protocols, such as:

- I2S
- LSB or MSB-justified
- PCM/DSP
- TDM
- AC'97
- SPDIF
- PDM

The SAI has two independent audio protocol processing modules. Each module has its independent clock unit and protocol processing unit. You can configure the modules to work together or independently or configure each module in master or slave mode and transmitter or receiver mode.

The SAI supports dual-channel/single-channel, μ_law/a_law compression/decompression.

3.31 TRNG

The true random number generator (TRNG) is a random number generator that provides a 32-bit random number based on continuous analog noise.

TRNG uses an 8 MHz HSI. After TRNG is enabled, TRNG_DR register can be read after about 1,500 clock periods.

- Provides 32-bit random numbers generated by the analog generator.
- The interval at which two random numbers are generated is 40 × TRNG_CLK clock periods.
- The entropy of TRNG is monitored for the identification of exceptional behaviors (generation of stable values or stable value sequences).
- TRNG can be disabled to reduce power consumption.

3.32 AES

HK32AUTO39A-3A integrates an advanced encryption and decryption unit fully compliant with Federal Information Processing Standards 197 (FIPS 197).

- Supports electronic code book (ECB)/cipher block chaining (CBC)/counter mode (CTR).

- 128/192/256-bit key configurable
- Encryption and decryption computation time:
  - 128-bit key: 57 clock periods
  - 192-bit key: 67 clock periods
  - 256-bit key: 77 clock periods
- Decryption key preparation time:
  - 128-bit key: 57 clock periods
  - 192-bit key: 67 clock periods
  - 256-bit key: 77 clock periods
- Supports the randomization of the AES clock by using TRNG.
- More convenient protection of the register content and easier resumption of the context when interrupts occur.

3.33 Hash

The hash module is applicable to data authentication applications and is compliant with the following protocols:

- Federal Information Processing Standards Publications 180-2 (FIPS PUB 180-2)
- Secure Hash Algorithm 256 (SHA-256)

When the SHA-256 fast computation processing system is the slave, the input data can be in words, half words, bytes, and bits (little-endian representation).

To adapt to the SHA-256 standard that adopts the big-endian mode, the last input data of little-endian mode is automatically padded to fit the digest minimum block size of 512 bits (16 × 32 bits).

3.34 ADC

HK32AUTO39A-3A has three 12-bit analog-to-digital converters (ADCs) that can perform conversions in single or scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface include:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single sample

The ADC can be operated by using the DMA controller. The analog watchdog function can realize precise monitoring of one, some, or all selected channels. When the monitored signal exceeds the preset threshold, an interrupt is generated. The events generated by general-purpose timers (TIMx) and advanced timers (TIM1/TIM8) can be internally connected to the ADC start trigger events and injection trigger events respectively. The application program then synchronizes the A/D conversion with timers.

3.35 DAC

HK32AUTO39A-3A embeds a digital-to-analog converter (DAC). This DAC embeds two 12-bit buffered DAC channels. They are used to convert 2-channel digital signals to 2-channel analog voltage signals and output the signals.

The main features of DAC include:

- Two DACs: each corresponds to an output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode

- Update synchronization
- Noise-wave generation
- Triangular-wave generation
- Independent or simultaneous conversions of the two DAC channels
- DMA capability for each channel
- External triggering for conversion
- Input voltage reference V_{REF+}

HK32AUTO39A-3A has eight DAC trigger inputs. The update outputs of timers can trigger the DAC channels and can be connected to different DMA channels.

3.36 Voltage comparator

HK32AUTO39A-3A incorporates up to four voltage comparators (COMPs).

- Four pairs of voltages are input to four independent voltage comparators via eight I/Os.
- The outputs of the four voltage comparators can be inputs to I/Os or event inputs to timers.
  - The output of one voltage comparator can be the OCREF_CLR event of TIM1 and TIM8.
  - The outputs of three voltage comparators can be the Break event of TIM1 and TIM8.
- The outputs of the voltage comparators can be event inputs to EXTI for system wakeup and interrupt generation.
- Programmable hysteresis voltage of each voltage comparator: 0 mV or 30 mV
- Voltage comparators have programmable speeds and power modes.
  - Low-speed ultra-low-power mode: the power consumption can be as low as 3 µA.
  - Low-speed low-power mode: the typical power consumption is 5 µA.
  - Medium-speed medium-power mode: the typical power consumption is 40 µA.
  - High-speed high-power mode: the typical power consumption is 100 µA.
- The output polarity of voltage comparators is configurable: high level or low level.

3.37 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.38 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32AUTO39A-3A MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process that has a security mechanism.

3.39 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from Flash memory

- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the USART1 interface.

3.40 Debug and trace port

HK32AUTO39A-3A embeds the ARM SWJ-DP which is a combined JTAG-DP and SW-DP that enables you to connect either a serial wire debug (SWD) or JTAG probe to a target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively. A special signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress values within a short time.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}–V_{SS}	External main power supply voltage (including V_{DDA} and V_{DD})	–0.5	3.63	V
V_{IN}	Input voltage on pins	V_{SS} – 0.3	V_{DD}	
$\|\Delta V_{DDx}\|$	Variation between different power pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	Variation between different ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	150	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of the positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–45 to +150	°C
T_J	Maximum junction temperature (except for HK32AUTO39A-3ACET7)	125	
	Maximum junction temperature (applicable to HK32AUTO39A-3ACET7)	105	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	60	MHz
f_{PCLK2}	Internal APB2 clock frequency	0	120	MHz
V_{DD}	Standard operating voltage	2.0	3.6	V
V_{DDA}(1)	Analog operating voltage	2.0	3.6	V
V_{BAT}	Backup operating voltage	1.8	3.6	V
T	Operating temperature (except for HK32AUTO39A-3ACET7)	–40	125	°C
	Operating temperature (applicable to HK32AUTO39A-3ACET7)	–40	105	°C

(1). It is recommended that you use the same power supply for V_{DD} and V_{DDA}.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (V_{DD} rising edge)	PLS[2:0] = 000	2.183	2.188	2.196	V
		PLS[2:0] = 001	2.286	2.289	2.298	
		PLS[2:0] = 010	2.393	2.399	2.407	
		PLS[2:0] = 011	2.502	2.508	2.518	
		PLS[2:0] = 100	2.621	2.629	2.639	
		PLS[2:0] = 101	2.726	2.733	2.745	
		PLS[2:0] = 110	2.839	2.846	2.855	
		PLS[2:0] = 111	2.958	2.969	2.979	
	Programmable voltage detector level selection (V_{DD} falling edge)	PLS[2:0] = 000	2.116	2.119	2.125	
		PLS[2:0] = 001	2.208	2.211	2.220	
		PLS[2:0] = 010	2.305	2.310	2.320	
		PLS[2:0] = 011	2.399	2.406	2.416	
		PLS[2:0] = 100	2.506	2.512	2.521	
		PLS[2:0] = 101	2.596	2.602	2.613	
		PLS[2:0] = 110	2.693	2.701	2.710	
		PLS[2:0] = 111	2.798	2.805	2.817	

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge(2)	1.8	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.0	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	Reset duration	-	1.50	2.50	4.50	ms

(1). PDR is based on the monitoring of V_{DD} and V_{DDA}. POR is based on the monitoring of only V_{DD}.

(2). The actual performance value is guaranteed to be smaller than the minimum $V_{POR/PDR}$ value.

(3). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C(1)	0.74	0.8	0.811	V
		–40°C to 125°C(2)	(TBD)	(TBD)	(TBD)	V

(1). The condition from –40°C to 105°C is for HK32AUTO39A-3ACET7.

(2). The condition from –40°C to 125°C is for HK32AUTO39A-3ACET3, HK32AUTO39A-3ARET3, and HK32AUTO39A-3AVET3.

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition		V_{DD} = 3.3 V				Unit
			–40°C	25°C	105°C	125°C	
Run mode	CPU operating at 120 MHz; APB clock enabled; Four wait states to access Flash.	Cache enabled	12.18	20.95	23.44	(TBD)	mA
		Cache disabled	11.2	19.34	21.82		mA
	CPU operating at 120 MHz; APB clock disabled; Four wait states to access Flash.	Cache enabled	6.71	11.50	13.81		mA
		Cache disabled	6.1	10.44	12.75		mA
	CPU operating at 8 MHz (HSE); APB clock enabled; Zero wait states to access Flash.	Cache enabled	1.83	1.98	4.1		mA
		Cache disabled	3.65	3.91	6.12		mA
	CPU operating at 8 MHz (HSE); APB clock disabled; Zero wait states to access Flash.	Cache enabled	1.19	1.36	3.41		mA
		Cache disabled	1.15	1.25	3.36		mA
	CPU operating at 40 kHz; APB clock enabled, using the 40 kHz LSI.		0.23	0.31	2.33		mA
	CPU operating at 32.768 kHz; APB clock enabled, using the 32.768 kHz LSE.		0.23	0.3	2.32		mA
Sleep mode	CPU paused; APB clock enabled, using the 120 MHz clock.		8.52	14.63	17.01		mA
	CPU paused; APB clock disabled, using the 120 MHz clock.		3.3	5.65	7.85		mA
	CPU paused; APB clock enabled, using the 8 MHz HSI.		1.56	1.69	3.72		mA
	CPU paused; APB clock disabled, using the 8 MHz HSI.		0.88	1.01	3.04		mA
Stop mode	CPU paused; LDO operating at full speed; HSE/HSI/LSE disabled; IWDG disabled.		202.67	303	2179		µA
	CPU paused; LDO in the low-power state; HSE/HSI/LSE disabled, IWDG disabled.		18.38	89.47	1374		µA
Standby mode	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; The Standby circuitry works as normal; LSI oscillator enabled; IWDG enabled.		2.98	3.87	30.29		µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; The Standby circuitry works as normal; LSI oscillator disabled; IWDG disabled.		2.96	3.87	30.22		µA
	CPU powered off, internal LDO disabled, core domain (including CPU, SRAM, Flash, registers) powered off; The Standby circuitry works as normal; HSE, HSI, LSE, and LSI disabled.		2.35	3.36	29.72		µA
Shutdown mode	CPU paused, LSE enabled, RTC running (BKPPDS = 0)		1.7	2.67	21.87		µA
	CPU paused, LSE disabled, RTC disabled (BKPPDS = 1)		0.04	0.09	1.60		µA
	CPU paused, LSE disabled, RTC stopped (BKPPDS = 0)		1.31	2.19	21.27		µA
V_{BAT}	CPU paused, LSE/LSI enabled, RTC running		1.7	2.67	25.86		µA
	CPU paused, LSE/LSI enabled, RTC stopped		1.31	2.19	21.27		µA

4.2.6 HSE clock characteristics

Table 4-9 HSE oscillator circuit characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{crystal}$(1)	Crystal oscillator frequency range supported by the oscillator circuit	-	4	-	32	MHz

(1). The value is guaranteed in design.

HK32AUTO39A-3A integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

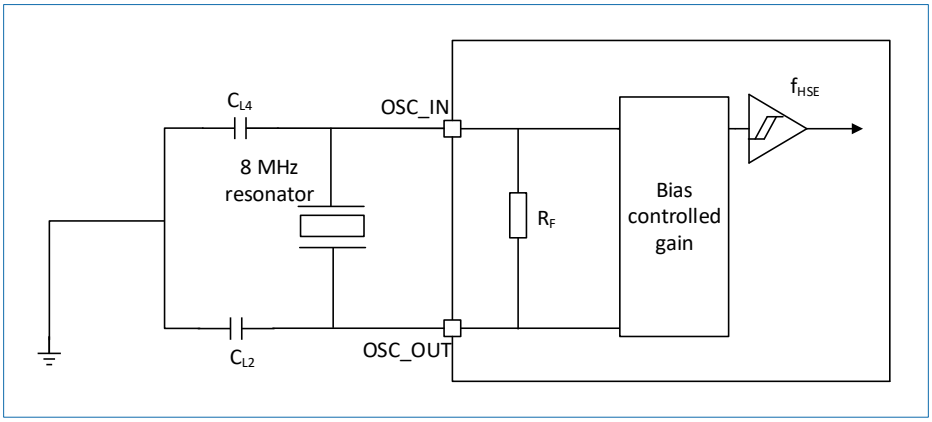

Figure 4-1 HSE negative feedback circuit

When HSE is configured to bypass mode, the HSE oscillator circuit is disabled. The OSC_IN pin can work as a clock input pin from which an external clock signal is input. The following table describes the requirements for this clock signal.

Table 4-10 Characteristics of the clock signal input from OSC_IN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	Frequency	-	1	8	25	MHz
V_{HSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$T_{w(HSE)}$	Effective high/low level duration		5	-	-	ns
$Tr_{(HSE)}$/$Tf_{(HSE)}$	Rise/Fall time		-	-	20	
$Cin_{(HSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.7 LSE clock characteristics

Table 4-11 LSE oscillator circuit characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{crystal}$(1)	Crystal oscillator frequency range supported by the oscillator circuit	-	-	32.768	-	kHz
R_F(1)	Feedback resistor	-	-	2		MΩ
T_{stb}	Oscillator startup time(2)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	2000	ms
C(1)	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12.5	-	pF
g_m	Oscillator transconductance	Started	-	-	-	
I_2(1)	LSE driving current	-	-	400	-	nA

(1). The values are guaranteed in design.

(2). T_{stb} refers to the time from LSE startup to the time when it outputs stable frequency signals.

HK32AUTO39A-3A integrates an LSE negative feedback oscillator circuit. The following startup circuit outside the

chip is recommended:

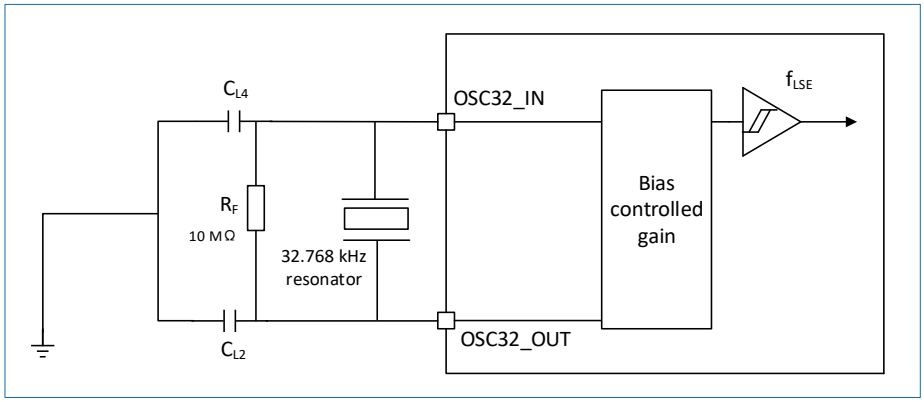

Figure 4-2 LSE negative feedback circuit

When LSE is configured to bypass mode, the LSE oscillator circuit is disabled. The OSC32_IN pin can work as a clock input pin from which an external clock signal is input. The following table describes the requirements for this clock signal.

Table 4-12 Characteristics of the clock signal input from LSE_OSC32_IN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{LSE_ext}	Frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the input pin		0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	Low level voltage on the input pin		V_{SS}	-	0.3 × V_{DD}	
$Tw_{(LSE)}$	Effective high/low level duration		450	-	-	ns
$Tr_{(LSE)}/Tf_{(LSE)}$	Rise/Fall time		-	-	50	
$Cin_{(LSE)}$	Input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.8 HSI clock characteristics

Table 4-13 Characteristics of the HSI clock

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI} RC 56	RC oscillator	-		-	56	-	MHz
f_{HSI}	Frequency	-		-	8	-	
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Oscillator accuracy	Factory trimmed accuracy (ambient temperature)		–1	-	1	
		Factory calibrated	TA= –40°C to 125°C	-	-	(TBD)	%
			TA= –40°C to 105°C	-	-	2.5	%
			TA= –40°C to 85°C	-	-	2.2	%
			TA = 0°C to 70°C	-	-	2	%
$Tsu_{(HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		1	-	2	µs
$I_{DD(HSI)}$	Oscillator power consumption	-		-	80	100	µA

4.2.9 LSI clock characteristics

Table 4-14 Characteristics of the LSI clock

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$tsu_{(LSI)}$	Oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$	Oscillator power consumption	-	0.65	1.2	µA

4.2.10 PLL characteristics

Table 4-15 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	8.0	80	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	120	MHz
t_{LOCK}	PLL lock time	-	80	120	μs
Jitter	Cycle-to-cycle jitter	-	5	13	ps

4.2.11 GPIO input clock

Clocks can be input from PA1, PB1, PC7, and PB7.

Table 4-16 GPIO input clock characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_{ext}	Input clock frequency	1	8.0	64	MHz
	Input clock duty cycle	40	-	60	%

4.2.12 Flash memory characteristics

Table 4-17 Flash memory characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PROG}	One-byte programming time	6	-	7.5	μs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
IDD_{PROG}	One-byte programming current	-	-	5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Read current@24 MHz	-	2	3	mA
	Read current@1 MHz	-	0.25	0.4	mA
N_{END}	Erasure endurance	100,000			Cycles
t_{RET}	Data retention	20			Years

4.2.13 I/O pin input characteristics

Table 4-18 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	1.6	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.5	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	1.56	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.26	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	300	-	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V 0 < V_{IN} < 3.3 V	-	0.01	1	μA
		V_{DD} = 3.3 V V_{IN} = 5 V	-	0.02	1	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	35	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	35	-	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.14 I/O pin output characteristics

Table 4-19 I/O pin output direct current characteristics

Speed Mode OSPEEDy[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	V
	V_{OH}	Output high level voltage		-	125	V
01	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	V

Speed Mode OSPEEDy[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
	V_{OH}	Output high level voltage	R_{Load} = 5 Kohm	-	125	V
11	V_{OL}	Output low level voltage	CL = 50 pF, V_{DD} = 2 V to 3.6 V R_{Load} = 5 Kohm	-	2	V
	V_{OH}	Output high level voltage		-	125	V

Table 4-20 I/O pin output alternating current characteristics

Mode OSPEEDy[1:0]	Symbol	Parameter	Condition	Min	Max	Unit
10	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	125	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125	
01	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25	
11	$f_{max(IO)out}$	Max frequency	CL = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	5	ns
	$tr_{(IO)out}$	Output low to high level rise time		-	5	ns

4.2.15 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuits.

Table 4-21 NRST pin input characteristics

Symbol	Parameter	Min	Max	Unit
T_{Noise}	Low level ignored duration	-	265	ns

4.2.16 TIM characteristics

Table 4-22 TIM characteristics

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$F_{TIMxCLK}/2$ (1)	MHz

(1). $f_{TIMxCLK}$ = 120 MHz or 60 MHz.

4.2.17 QSPI characteristics

Table 4-23 QSPI characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ck}	QSPI clock frequency	2.7 V < V_{DD} < 3.6 V C_{load} = 30 pF	-	30	-	MHz
$t_{w(CKH)}$	QSPI clock high time	f_{AHBCLK} = 120 MHz, presc = 0	$t_{(ck)}/2 - 2$	-	$t_{(ck)}/2$	ns
$t_{w(CKL)}$	QSPI clock low time		$t_{(ck)}/2$	-	$t_{(ck)}/2 + 2$	ns
$t_{s(IN)}$	Data input setup time	-	8	-	-	ns
$t_{h(IN)}$	Data input hold time	-	5	-	-	ns
$t_{v(OUT)}$	Data output effective time	-	-		5.5	ns
$t_{h(OUT)}$	Data output hold time	-	0	-	-	ns

4.2.18 ADC characteristics

Table 4-24 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2	3.3	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0			V
I_{VREF}	Reference input current	-	-	150	480	μA
INL	Integral non linearity (maximum difference between the actual conversion point and the end point correlation line)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1.5	±4	LSB
DNL	Differential non linearity (maximum difference between the actual step and the ideal step)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1	±3	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S	Sampling frequency	-	0.05	-	1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} grounded)	-	VREF+	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}	Sample switch resistance	-	-	-	1	kΩ
C_{ADC}	Sample and hold capacitance	-	-	-	5	pF
t_{CAL}	ADC calibration time	f_{ADC} = 14 MHz	5.9			μs
		-	83			$1/f_{ADC}$
t_{lat}	Input trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	μs
		-	-	-	3	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	μs
		-	-	-	2	$1/f_{ADC}$
t_S	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	μs
		-	1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on startup time	-	0	0	1	μs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	μs
		-	14 to 252 (sampling time ts + 12.5 for successive approximation)			$1/f_{ADC}$

4.2.19 DAC characteristics

Table 4-25 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	2.0	3.3	3.6	V
V_{REF+}	Reference supply voltage	2.0	3.3	3.6	V
V_{SSA}	Ground	0	0	0	V
R_{LOAD}	Resistive load with buffer enabled	5	-	-	kΩ
R_O	Impedance output with buffer disabled	-	15	-	kΩ
C_{LOAD}	Capacitive load	-	-	-	pF
DAC_OUT min	Lower DAC_OUT voltage with buffer enabled	0.1	-	-	V
DAC_OUT max	Higher DAC_OUT voltage with buffer enabled	-	-	V_{DD} – 0.1	V
DAC_OUT min	Lower DAC_OUT voltage with buffer disabled	0	-	-	mV
DAC_OUT max	Higher DAC_OUT voltage with buffer disabled	-	-	V_{REF}	V
$I_{DDVREF+}$	DAC direct current consumption in quiescent mode (standby mode)	108	135	162	μA
I_{DDA}	DAC direct current consumption in quiescent mode	-	-	429	μA
DNL	Differential non linearity (difference between two consecutive code – 1LSB)	-	-	±1	LSB
INL	Integral non linearity (difference between measured	-	-	±4	LSB

Symbol	Parameter	Min	Typ	Max	Unit
	value at code i and the value at code i on a line drawn between code 0 and last code 1023)	-	-	±4	LSB
Offset	Offset error (difference between the measured value at code 0x800 and the ideal value V_{REF+}/2)	-	-	±10	mV
		-	-	±12	LSB
Gain error	Gain error	-	-	±0.5	%
$t_{SETTLING}$	Settling time (full scale: when DAC_OUT reaches the final value ±1LSB, the transition for a 10-bit input code from the minimum to the maximum)	-	3	4	µs
Update rate	Maximum frequency of obtaining a correct DAC_OUT change when the input code changes slightly (from code i to i + 1LSB)	-	-	1	MS/s
t_{WAKEUP}	Wakeup time from the off state (setting the ENx bit in the DAC control register)	-	6.5	10	µs
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	–67	–40	dB

4.2.20 Temperature sensor characteristics

Table 4-26 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L	Temperature linearity	-		±1	±2	°C
V_{25}	Output voltage	25°C	0.76	0.909	0.94	V
Avg_Slope	Average slope	-	2.9	3	3.1	mV/°C

5 Typical circuitry

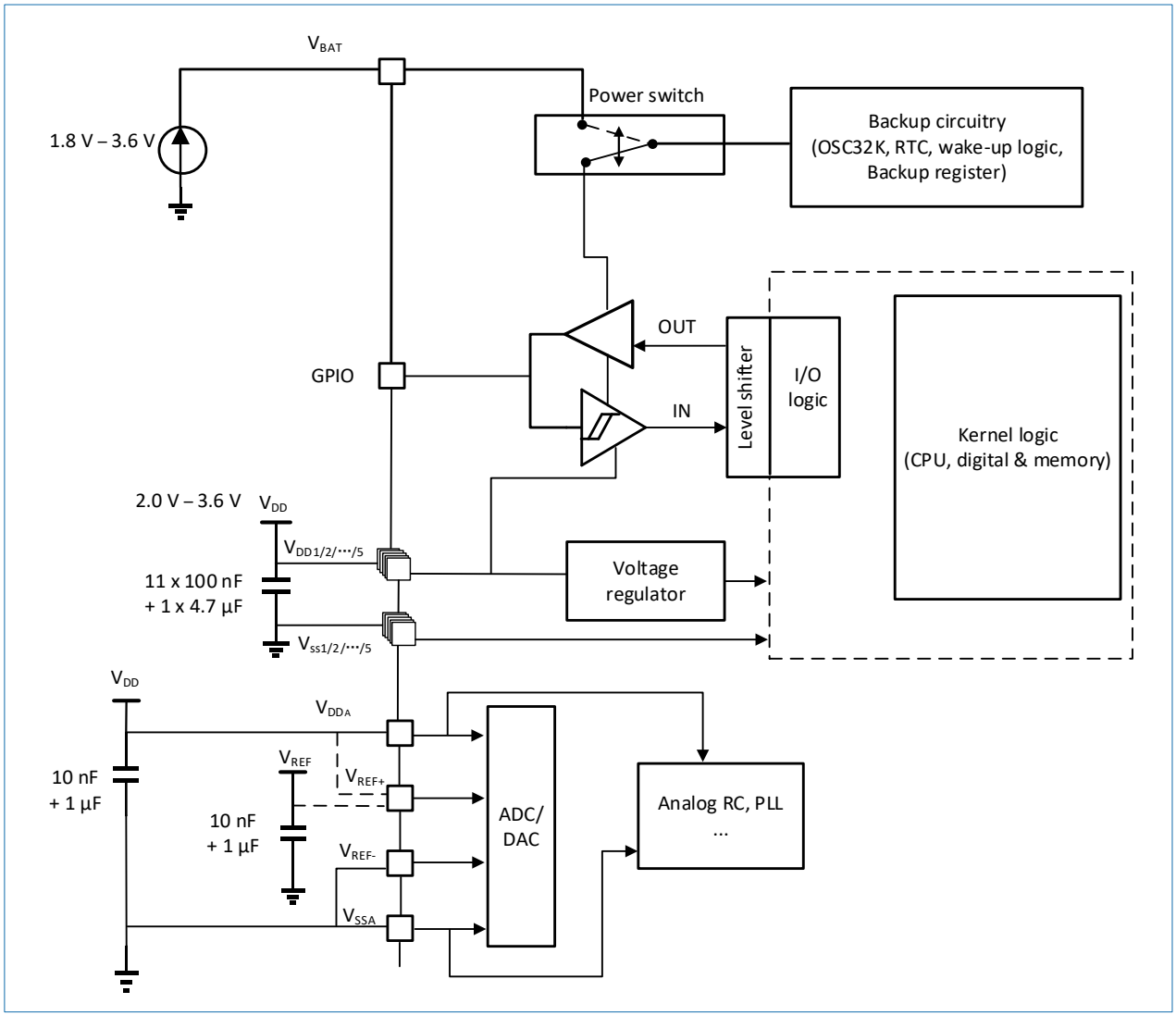

Figure 5-1 Power supply block diagram

6 Pinouts and pin descriptions

HK32AUTO39A-3A is delivered in LQFP48, LQFP64, and LQFP100 packages. The pinouts of the packages are as follows:

6.1 LQFP48

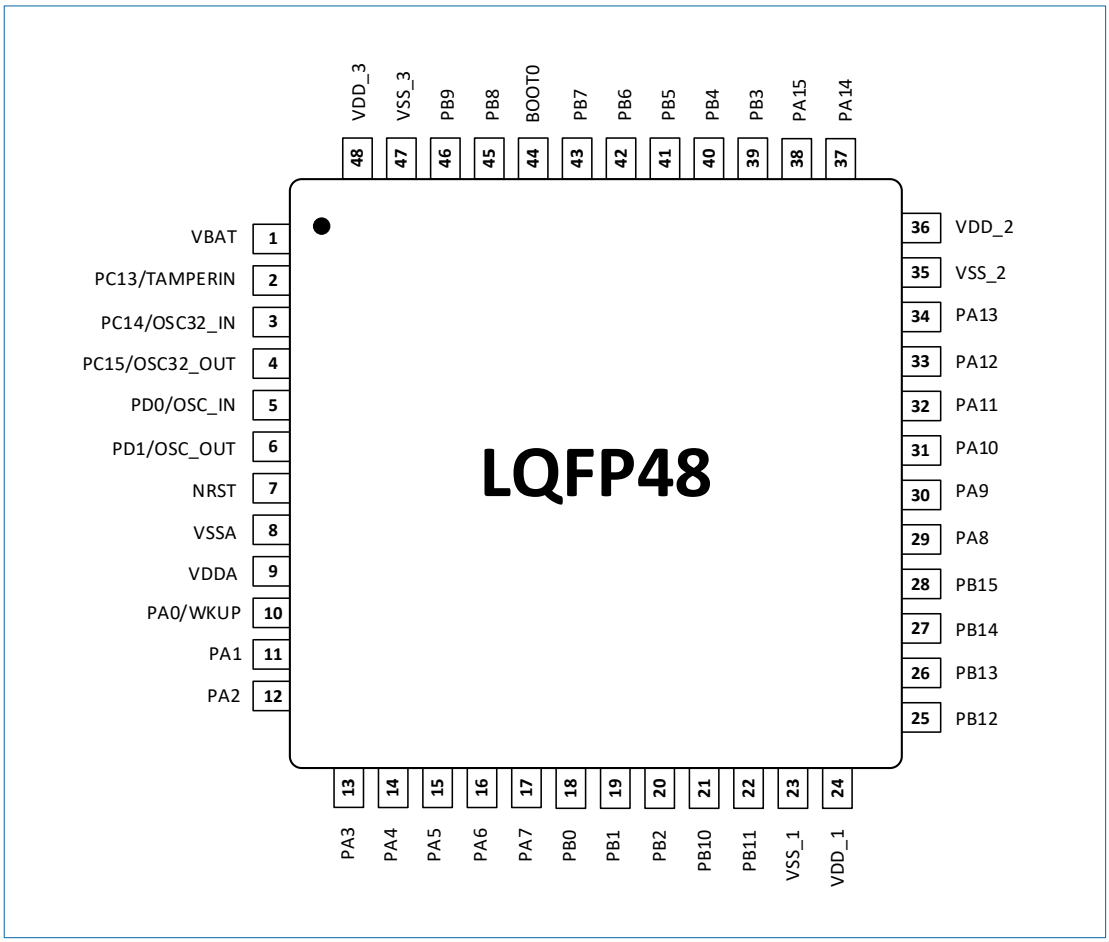

Figure 6-1 LQFP48 package pinout

6.2 LQFP64

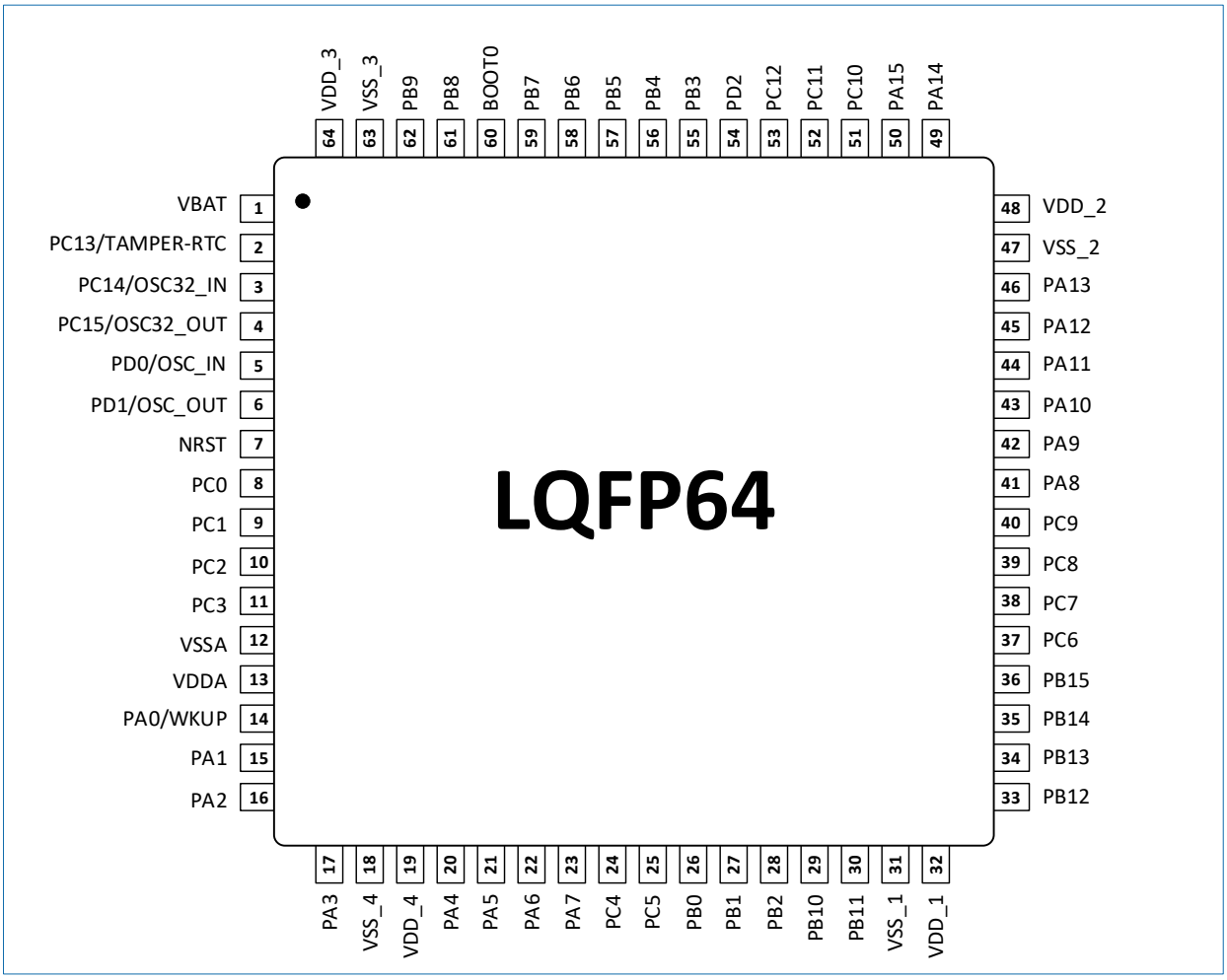

Figure 6-2 LQFP64 package pinout

6.3 LQFP100

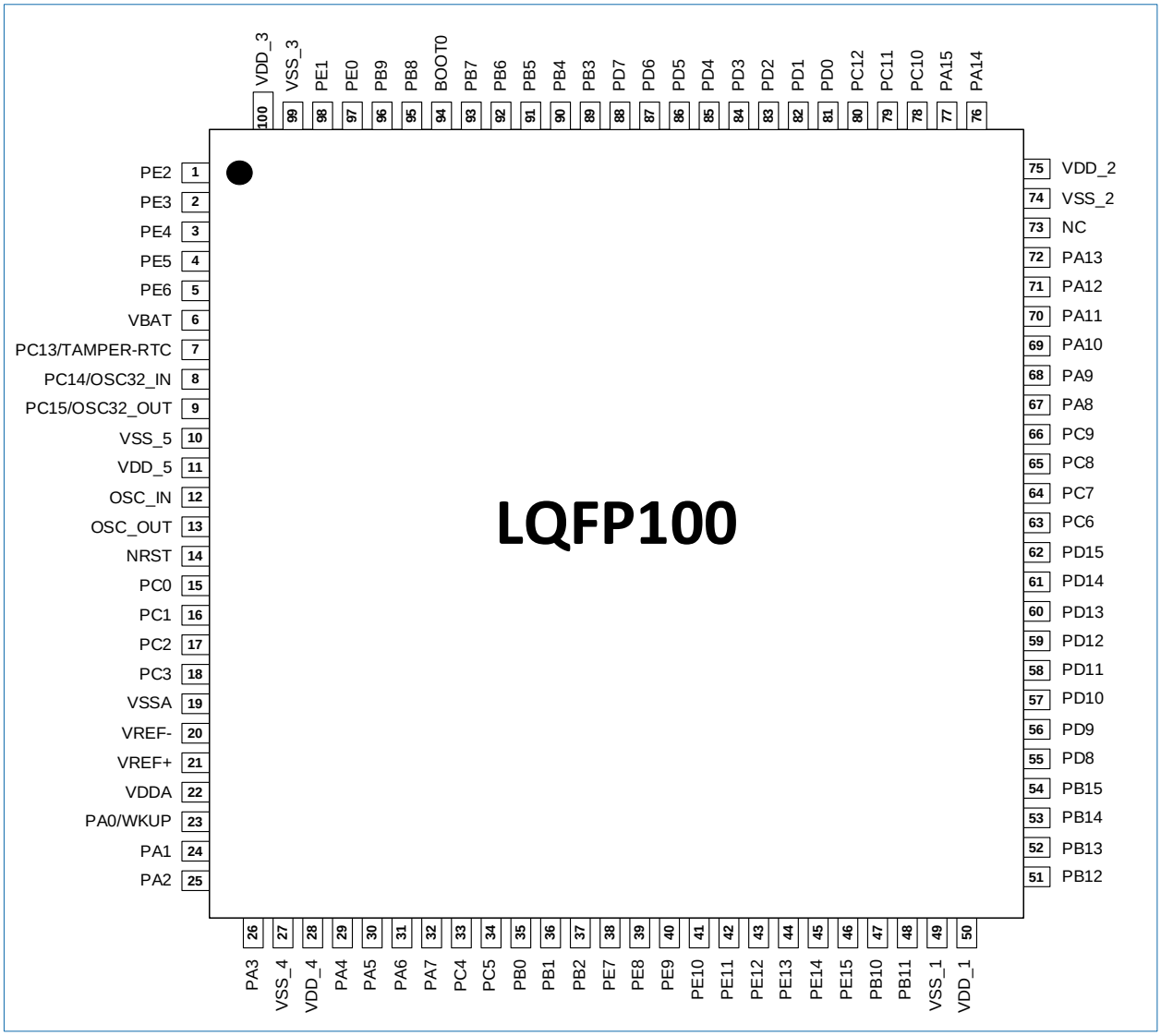

Figure 6-3 LQFP100 package pinout

6.4 Pin description

The following table shows pin descriptions of LQFP48, LQFP64, and LQFP100 packages.

Table 6-1 Pin description of each package

LQFP48	LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
-	-	1	PE2	I/O	-	TRACECKO/FSMC_A23/ADC2_IN17	TXEV/EXTIN2/SAI_MCLK_A
-	-	2	PE3	I/O	-	TRACEDO0/FSMC_A19/ADC2_IN18	TXEV/EXTIN3
-	-	3	PE4	I/O	-	TRACEDO1/FSMC_A20/ADC3_IN17	TXEV/EXTIN4/SAI_FS_A
-	-	4	PE5	I/O	-	TRACEDO2/FSMC_A21/ADC3_IN18	TXEV/EXTIN5/SAI_SCK_A
-	-	5	PE6	I/O	FT	TRACEDO3/FSMC_A22	TXEV/EXTIN6/SAI_SD_A
1	1	6	VBAT	S	-	-	-
2	2	7	PC13/ TAMPER-RTC	I/O(3)	-	TAMPER-RTC/WKUP1/RTCO/ QSPI_BK1_NCS	TXEV/EXTIN13
3	3	8	PC14/OSC32_IN	I/O(3)	-	OSC32_IN/LSE_CKI	TXEV/EXTIN14

LQFP48	LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
			(PC14)				
4	4	9	PC15/OSC32_OUT (PC15)	I/O(3)	-	OSC32_OUT	TXEV/EXTIN15
-	-	10	VSS_5	S	-	-	-
-	-	11	VDD_5	S	-	-	-
5	5	-	PD0/OSC_IN (OSC_IN)	I/O	-	OSC_IN/HSE_CKI	TXEV/PD0/CAN1_RX/EXTIN0
6	6	-	PD1/OSC_OUT (OSC_OUT)	I/O	-	OSC_OUT	TXEV/PD1/CAN1_TX/EXTIN1
-	-	12	OSC_IN	I	-	OSC_IN/HSE_CKI	-
-	-	13	OSC_OUT	O	-	OSC_OUT	-
7	7	14	NRST	I/O	-	-	-
-	8	15	PC0	I/O	-	ADC123_IN10/DCMI_PIXCLK	TXEV/EXTIN0/FSMC_A13
-	9	16	PC1	I/O	-	ADC123_IN11/DCMI_PIXDI13 / TFT_DEN1	TXEV/EXTIN1
-	10	17	PC2	I/O	-	ADC123_IN12/DCMI_PIXDI12 / TFT_VSYNC1	TXEV/EXTIN2
-	11	18	PC3	I/O	-	ADC123_IN13/DCMI_PIXDI11 / TFT_HYSNC1	TXEV/EXTIN3
8	12	19	VSSA	S	-	-	-
-	-	20	VREFN	S	-	-	VSSA and VREFN are internally connected in the LQFP48 and LQFP64 package.
-	-	21	VREFP	S	-	-	VDDA and VREFP are internally connected in the LQFP48 and LQFP64 package.
9	13	22	VDDA	S	-	-	-
10	14	23	PA0/WKUP(PA0)	I/O (3)	-	WKUP0/USART2_CTS/ADC123_IN0/ TIM2_CH1_ETR/TIM5_CH1/ TIM8_ETR/EXTIN0/DCMI_PIXDI10	TXEV/FSMC_NE4
11	15	24	PA1	I/O	-	USART2_RTS/ADC123_IN1/ TIM5_CH2/TIM2_CH2/EXTIN1/ RCC_CKI0/DCMI_PIXDI9	TXEV/FSMC_A14
12	16	25	PA2	I/O	-	USART2_TX/TIM5_CH3/ ADC123_IN2/TIM2_CH3/EXTIN2/ TFT_DCLK	TXEV
13	17	26	PA3	I/O	-	USART2_RX/TIM5_CH4/ ADC123_IN3/TIM2_CH4/EXTIN3/ DCMI_PIXDI8/SAI_MCLK_A	TXEV/FSMC_A15
-	18	27	VSS_4	S	-	-	-
-	19	28	VDD_4	S	-	-	-
14	20	29	PA4	I/O	-	SPI1_NSS/USART2_CK/DAC1_OUT/ ADC12_IN4/EXTIN4/TFT_DEN2/ I2S1_WS/TIM5_ETR/SAI_FS_B	TXEV
15	21	30	PA5	I/O	-	SPI1_SCK/DAC2_OUT/ADC12_IN5/ EXTIN5/TFT_VSYNC2/I2S1_CK / SAI_MCLK_B	TXEV
16	22	31	PA6	I/O	-	SPI1_MISO/TIM8_BKIN/ADC1	TXEV/TIM1_BKIN

LQFP48	LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
						2_IN6/TIM3_CH1/EXTIN6/TFT_HYSNC2/SAI_SCK_B	
17	23	32	PA7	I/O	-	SPI1_MOSI/TIM8_CH1N/ADC12_IN7/TIM3_CH2/EXTIN7/DCMI_PIXDI7/I2S1_SD/SAI_SD_B	TXEV/TIM1_CH1N/ FSMC_A0
-	24	33	PC4	I/O	-	ADC12_IN14/DCMI_PIXDI6/ I2S1_MCK	TXEV/EXTIN4/FSMC_A1
-	25	34	PC5	I/O	-	ADC12_IN15/DCMI_PIXDI5	TXEV/EXTIN5/FSMC_A2
18	26	35	PB0	I/O (3)	-	ADC12_IN8/TIM3_CH3/TIM8_CH2N/WKUP2/DCMI_PIXDI4	TXEV/TIM1_CH2N/EXTIN0/ FSMC_A3/CAN2_RX
19	27	36	PB1	I/O	-	ADC12_IN9/TIM3_CH4/TIM8_CH3N/RCC_CKI1/DCMI_PIXDI3	TXEV/TIM1_CH3N/EXTIN1/ FSMC_A4/CAN2_TX
20	28	37	PB2	I/O	FT	BOOT1(4)/QSPI_BK1_IO0/USART6_CK	TXEV/EXTIN2/FSMC_A5/ SAI_SD_A
-	-	38	PE7	I/O	FT	FSMC_D4	TXEV/TIM1_ETR/EXTIN7/ SAI_SD_B
-	-	39	PE8	I/O	FT	FSMC_D5	TXEV/TIM1_CH1N/EXTIN8/ SAI_SCK_B
-	-	40	PE9	I/O	FT	FSMC_D6	TXEV/TIM1_CH1/EXTIN9/ SAI_FS_B
-	-	41	PE10	I/O	FT	FSMC_D7	TXEV/TIM1_CH2N/EXTIN10/ SAI_MCLK_B
-	-	42	PE11	I/O	FT	FSMC_D8	TXEV/TIM1_CH2/EXTIN11
-	-	43	PE12	I/O	FT	FSMC_D9	TXEV/TIM1_CH3N/EXTIN12
-	-	44	PE13	I/O	FT	FSMC_D10	TXEV/TIM1_CH3/EXTIN13
-	-	45	PE14	I/O	FT	FSMC_D11	TXEV/TIM1_CH4/EXTIN14
-	-	46	PE15	I/O	FT	FSMC_D12	TXEV/TIM1_BKIN/EXTIN15
21	29	47	PB10	I/O	-	I2C2_SCL/USART3_TX/COMP1_O	TXEV/TIM2_CH3/EXTIN10/ FSMC_INT2/SAI_SCK_A
22	30	48	PB11	I/O	-	I2C2_SDA/USART3_RX/COMP2_O	TXEV/TIM2_CH4/EXTIN11/ FSMC_INT3
23	31	49	VSS_1	S	-	-	-
24	32	50	VDD_1	S	-	-	-
25	33	51	PB12	I/O	FT	SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN/ DCMI_PIXDI2/TFT_DEN3/ADC3_IN16/CAN2_RX	TXEV/EXTIN12
26	34	52	PB13	I/O	FT	SPI2_SCK/I2S2_CK/USART3_CTS/ TIM1_CH1N/DCMI_PIXDI1/ TFT_VSYNC3/CAN2_TX/USART6_TX	TXEV/EXTIN13
27	35	53	PB14	I/O	FT	SPI2_MISO/TIM1_CH2N/ USART3_RTS/DCMI_PIXDI0/ TFT_HYSNC3/USART6_RX	TXEV/EXTIN14
28	36	54	PB15	I/O	FT	SPI2_MOSI/I2S2_SD/TIM1_CH3N/ USART4_CK	TXEV/EXTIN15/FSMC_INTR
-	-	55	PD8	I/O	FT	FSMC_D13	TXEV/USART3_TX/EXTIN8
-	-	56	PD9	I/O	FT	FSMC_D14	TXEV/USART3_RX/EXTIN9
-	-	57	PD10	I/O	FT	FSMC_D15	TXEV/USART3_CK/EXTIN10
-	-	58	PD11	I/O	FT	FSMC_A16_CLE	TXEV/USART3_CTS/ EXTIN11
-	-	59	PD12	I/O	FT	FSMC_A17_ALE	TXEV/TIM4_CH1/ USART3_RTS/EXTIN12
-	-	60	PD13	I/O	FT	FSMC_A18	TXEV/TIM4_CH2/EXTIN13
-	-	61	PD14	I/O	FT	FSMC_D0	TXEV/TIM4_CH3/EXTIN14
-	-	62	PD15	I/O	FT	FSMC_D1	TXEV/TIM4_CH4/EXTIN15

LQFP48	LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
-	37	63	PC6	I/O	FT	I2S2_MCK/TIM8_CH1/SDIO_D6 USART4_CTS	TXEV/TIM3_CH1/EXTIN6/ FSMC_A6
-	38	64	PC7	I/O	FT	I2S3_MCK/TIM8_CH2/SDIO_D7 RCC_CKI2/USART4_RTS	TXEV/TIM3_CH2/EXTIN7/ FSMC_A7
-	39	65	PC8	I/O	FT	TIM8_CH3/SDIO_D0	TXEV/TIM3_CH3/EXTIN8/ FSMC_A8/USART1_CTS/ USART5_TX
-	40	66	PC9	I/O	FT	TIM8_CH4/SDIO_D1	TXEV/TIM3_CH4/EXTIN9/ FSMC_A9/USART1_RTS/ USART5_RX
29	41	67	PA8	I/O	FT	USART1_CK/TIM1_CH1/RCC_MCO/ EXTIN8/QSPI_BK1_IO1/SAI_SCK_A	TXEV/FSMC_A10
30	42	68	PA9	I/O	FT	USART1_TX/TIM1_CH2/EXTIN9/ QSPI_BK1_IO2/SAI_FS_A	TXEV/FSMC_A11
31	43	69	PA10	I/O	FT	USART1_RX/TIM1_CH3/EXTIN10 QSPI_BK1_IO3/SAI_SD_A	TXEV/FSMC_A12
32	44	70	PA11	I/O	FT	USART1_CTS/USB_DM/CAN1_RX/ TIM1_CH4/EXTIN11/DCMI_VYSNC	TXEV
33	45	71	PA12	I/O	FT	USART1_RTS/USB_DP/CAN1_TX/ TIM1_ETR/EXTIN12/DCMI_HYSNC	TXEV
34	46	72	PA13 (JTMS/SWDIO)	I/O	FT	USART6_CTS	PA13/TXEV/DCMI_VYSNC FSMC_NIORD
-	-	73	NC	-	-	-	-
35	47	74	VSS_2	S	-	-	-
36	48	75	VDD_2	S	-	-	-
37	49	76	PA14 (JTCK/SWCLK)	I/O	FT	EXTIN14/USART5_CK	PA14/TXEV/FSMC_NIOWR/ USART2_CTS/I2C1_SMBA/ DCMI_HYSNC
38	50	77	PA15 (JTDI)	I/O	FT	SPI3_NSS/I2S3_WS/EXTIN15/ QSPI_CKO/USART6_RTS	TXEV/TIM2_CH1_ETR/PA15/ SPI1_NSS/FSMC_NREG/ USART2_RTS/I2S1_WS
-	51	78	PC10	I/O	-	USART4_TX/SDIO_D2/COMP1_N	TXEV/USART3_TX/EXTIN10/ FSMC_A24/USART2_TX
-	52	79	PC11	I/O	-	USART4_RX/SDIO_D3/COMP1_P	TXEV/USART3_RX/EXTIN11/FSMC_A25/USART2_RX
-	53	80	PC12	I/O	-	USART5_TX/SDIO_CK/COMP2_N	TXEV/USART3_CK/EXTIN12/FSMC_NE2_NCE3/USART2_CK
-	-	81	PD0	I/O	FT	FSMC_D2	TXEV/CAN1_RX/EXTIN0
-	-	82	PD1	I/O	FT	FSMC_D3	TXEV/CAN1_TX/EXTIN1
-	54	83	PD2	I/O	-	TIM3_ETR/USART5_RX/SDIO_CMD/COMP2_P	TXEV/EXTIN2 FSMC_NE3_NCE4_1
-	-	84	PD3	I/O	FT	FSMC_CLK/USART5_CTS	TXEV/USART2_CTS/EXTIN3/ SPI3_NSS/I2S3_WS
-	-	85	PD4	I/O	FT	FSMC_NOE/USART5_RTS	TXEV/USART2_RTS/EXTIN4/ SPI3_SCK/I2S3_CK
-	-	86	PD5	I/O	FT	FSMC_NWE	TXEV/USART2_TX/EXTIN5/ SPI3_MISO
-	-	87	PD6	I/O	FT	FSMC_NWAIT	TXEV/USART2_RX/EXTIN6/ SPI3_MOSI/I2S3_SD
-	-	88	PD7	I/O	FT	FSMC_NE1/FSMC_NCE2	TXEV/USART2_CK/EXTIN7/
39	55	89	PB3	I/O	-	TRACESWO/SPI3_SCK/I2S3_C	TXEV/PB3/TIM2_CH2/SPI1_S

LQFP48	LQFP64	LQFP100	Pin Name (default function after resets)	Type(1)	5 V-tolerant(2)	Alternate Function	Additional Function
			(JTDO)			K/TFT_DEN4/QSPI_BK2_NCS/ ADC3_IN5/COMP3_N	CK/I2S1_CK/EXTIN3/DCMI_PIXDI13/SAI_SCK_B
40	56	90	PB4 (NJRST)	I/O	-	SPI3_MISO/TFT_VSYNC4/ QSPI_BK2_IO0/ADC3_IN6/COMP3_P	TXEV/PB4/TIM3_CH1/ SPI1_MISO/EXTIN4/ DCMI_PIXDI12/SAI_MCLK_B
41	57	91	PB5	I/O	-	I2C1_SMBA/SPI3_MOSI/I2S3_SD/ TFT_VSYNC4/QSPI_BK2_IO1/ ADC3_IN7/COMP4_N	TXEV/TIM3_CH2/SPI1_MOSI/ I2S1_SD/EXTIN5/CAN2_RX/ DCMI_PIXDI11/SAI_SD_B
42	58	92	PB6	I/O	-	I2C1_SCL/TIM4_CH1/ QSPI_BK2_IO2/ADC3_IN8/COMP4_P	TXEV/USART1_TX/EXTIN6/ DCMI_PIXDI10/ FSMC_NCE4_2/CAN2_TX/ I2S1_MCK/SAI_FS_B
43	59	93	PB7	I/O	FT	I2C1_SDA/FSMC_NADV/TIM4_CH2/RCC_CKI3/QSPI_BK2_IO3	TXEV/USART1_RX/EXTIN7
44	60	94	BOOT0(4)	I	-	-	-
45	61	95	PB8	I/O	-	TIM4_CH3/SDIO_D4/COMP3_O	TXEV/I2C1_SCL/CAN1_RX/EXTIN8/FSMC_CD/USART4_TX/ SAI_MCLK_A
46	62	96	PB9	I/O	-	TIM4_CH4/SDIO_D5/COMP4_O	USART4_RX/TXEV/I2C1_SDA/ CAN1_TX/EXTIN9/SAI_FS_A
-	-	97	PE0	I/O	FT	TIM4_ETR/FSMC_NBL0	TXEV/EXTIN0
-	-	98	PE1	I/O	FT	FSMC_NBL1	TXEV/EXTIN1
47	63	99	VSS_3	S	-	-	-
48	64	100	VDD_3	S	-	-	-

(1). I = input, O = output, I/O = input/output, S = supply.

(2). FT: 5 V tolerant.

(3). Except for these pins, the other I/O pins have the Schmitt function and can be configured via registers.

(4). BOOT0/BOOT1 pin is connected to an internal weak pull-down resistor.

7 Packages

7.1 Package outlines

7.1.1 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

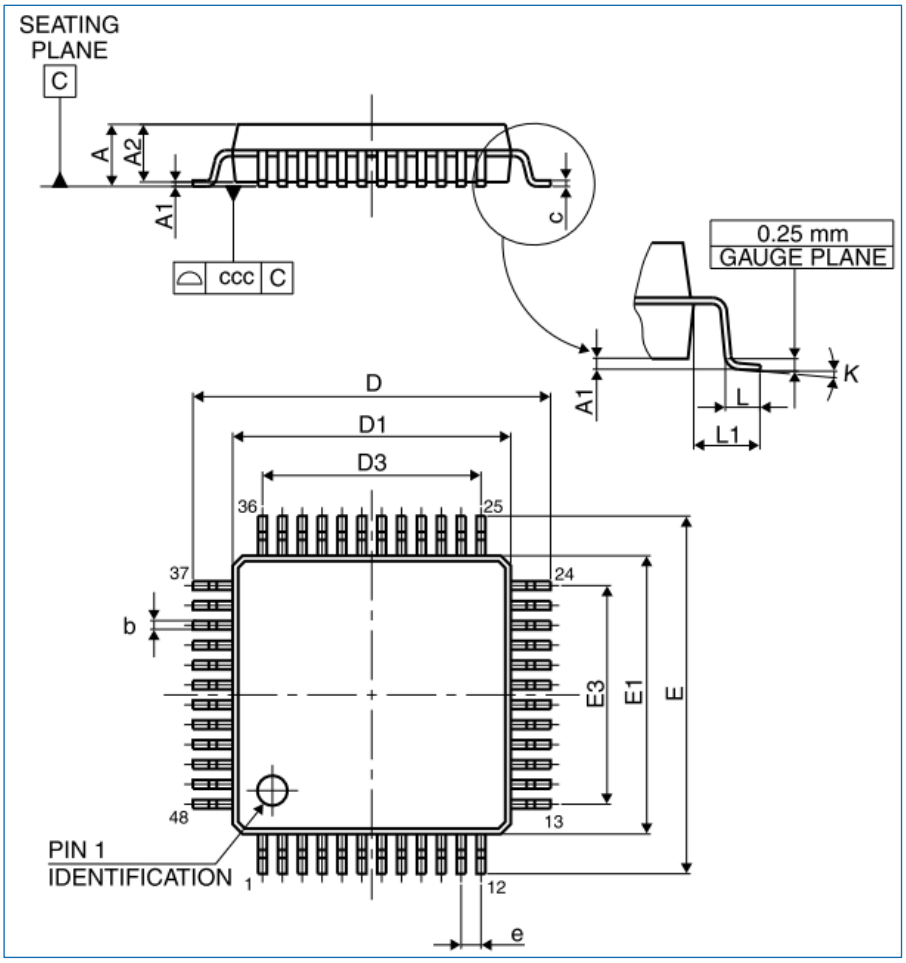

Figure 7-1 LQFP48 package outline

Table 7-1 LQFP48 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch, 64-pin low-profile quad flat package.

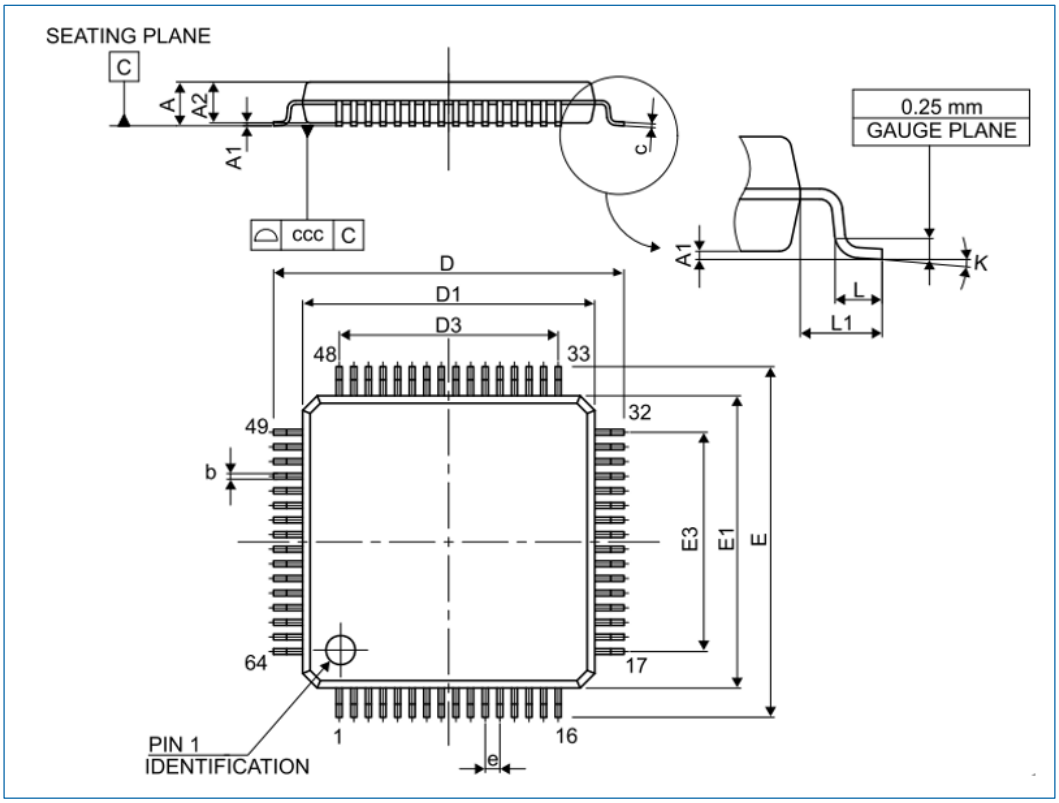

Figure 7-2 LQFP64 package outline

Table 7-2 LQFP64 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.3 LQFP100

LQFP100 is a 14 mm × 14 mm, 0.5 mm pitch, 100-pin low-profile quad flat package.

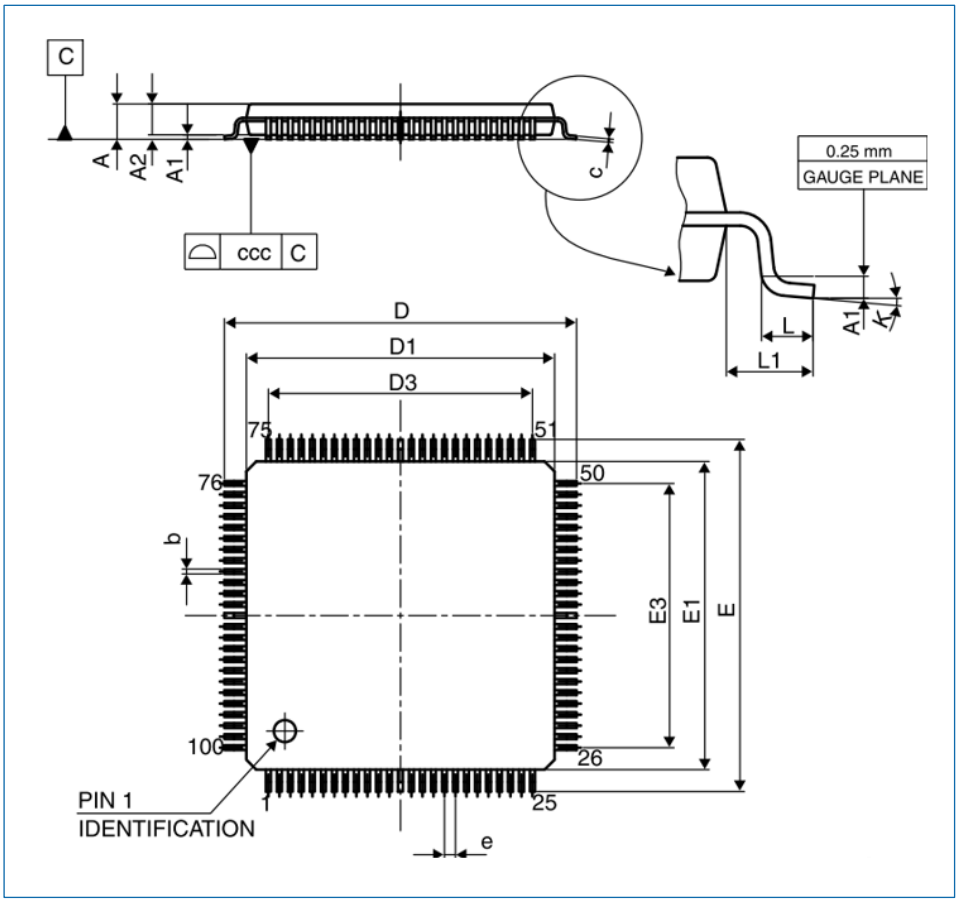

Figure 7-3 LQFP100 package outline

Table 7-3 LQFP100 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-4 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP48 marking

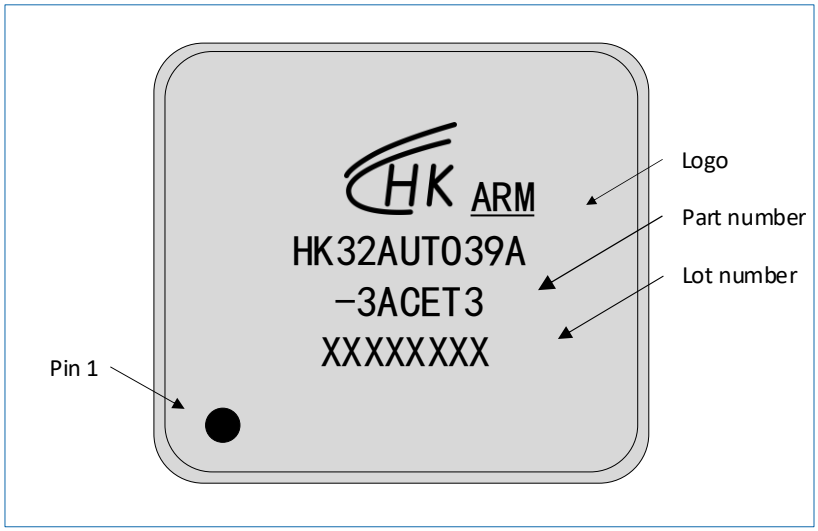

Figure 7-4 LQFP48 HK32AUTO39A-3ACET3 marking example

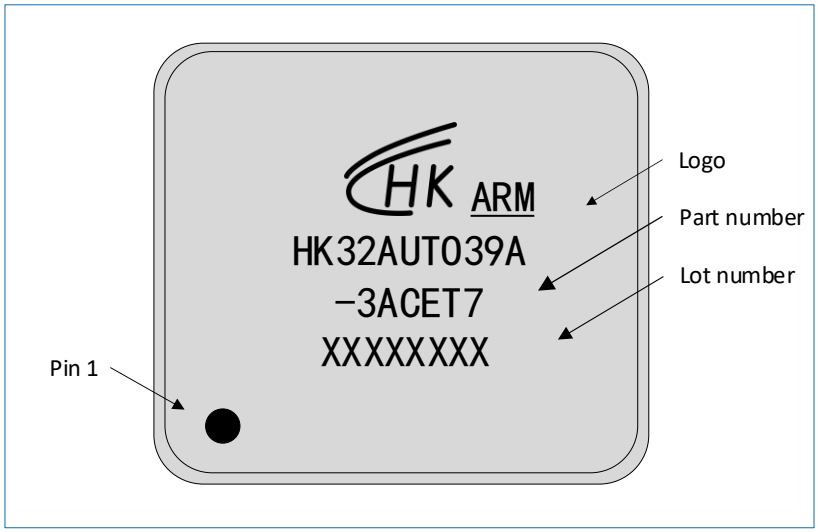

Figure 7-5 LQFP48 HK32AUTO39A-3ACET7 marking example

7.2.2 LQFP64 marking

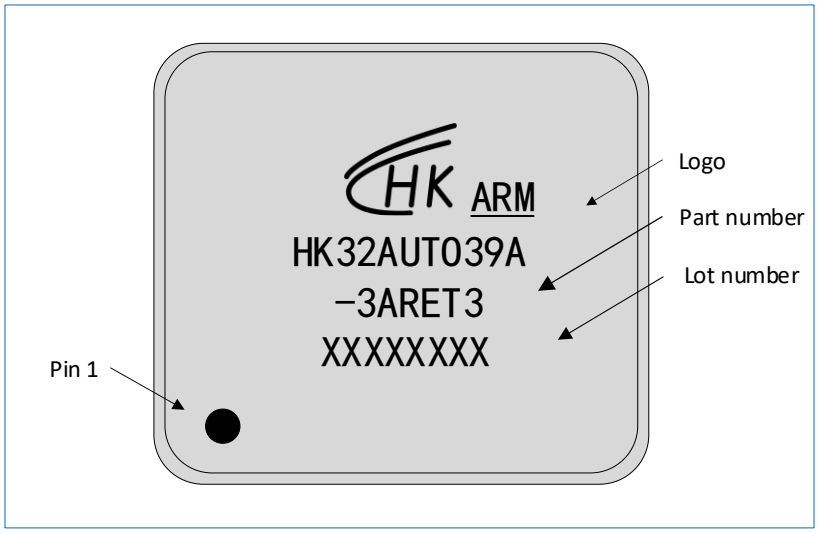

Figure 7-6 LQFP64 HK32AUTO39A-3ARET3 marking example

7.2.3 LQFP100 marking

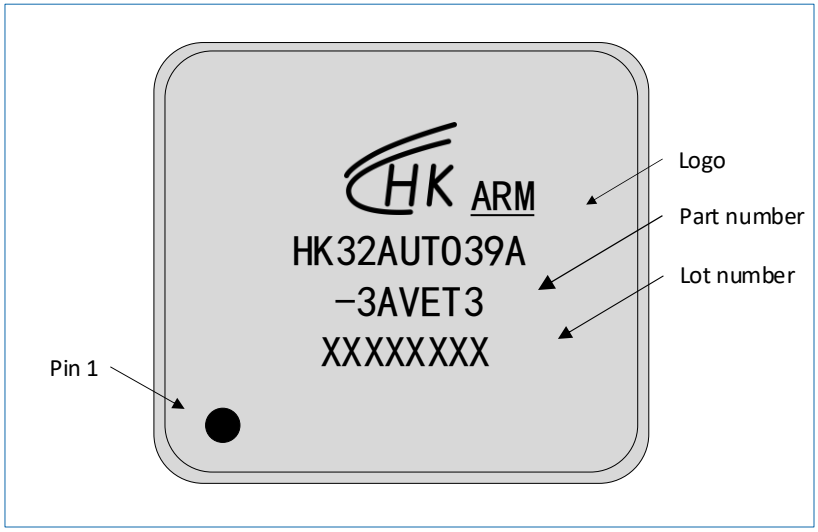

Figure 7-7 LQFP100 HK32AUTO39A-3AVET3 marking example

8 Ordering information

8.1 Device numbering conventions

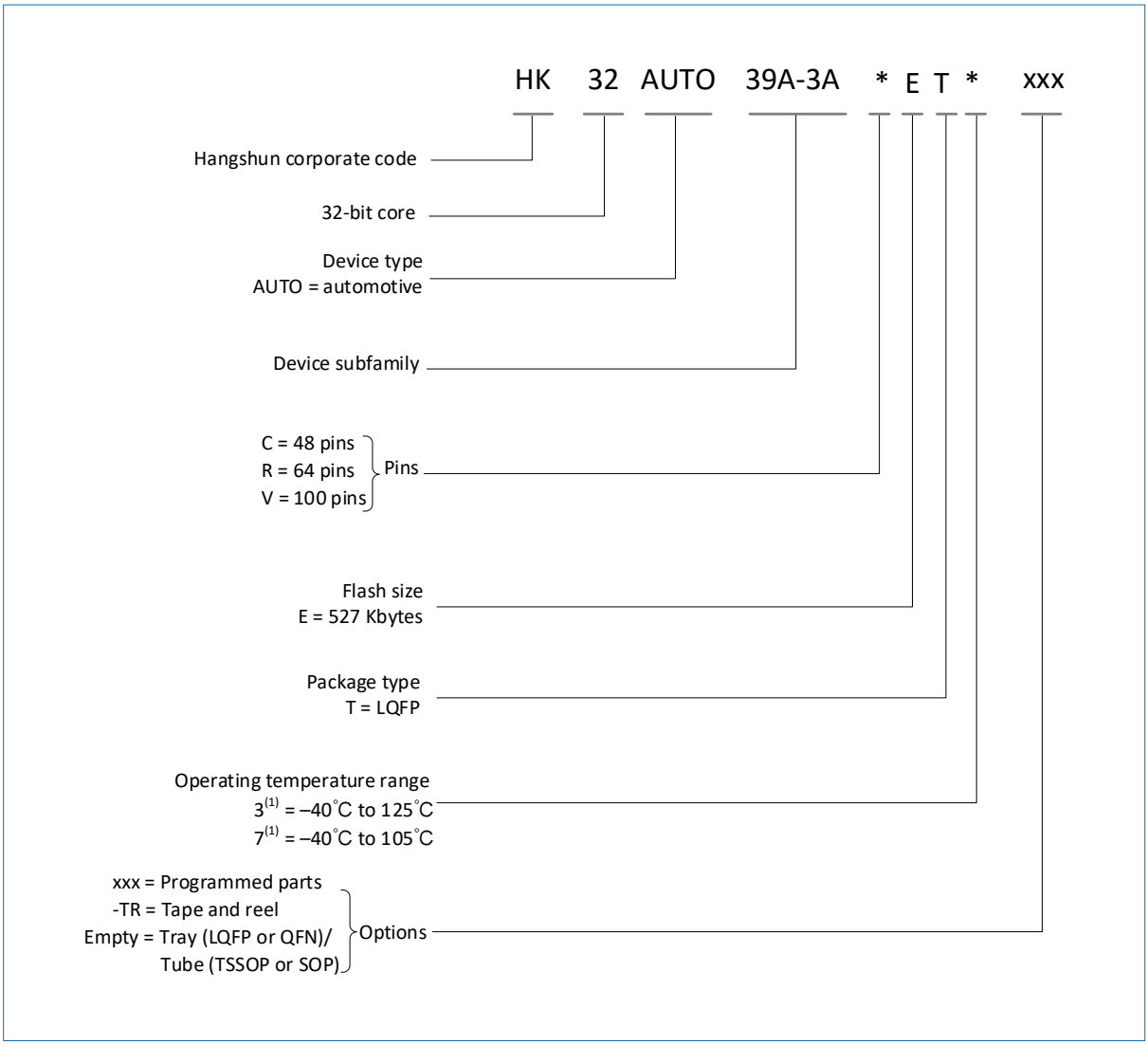

Figure 8-1 Device numbering conventions

Note:

(1). The operating temperature of HK32AUTO39A-3ACET7 is from –40°C to 105°C. For other part numbers of HK32AUTO39A-3A series, the operating temperature is from –40°C to 125°C.

8.2 Packaging information

Table 8-1 Packaging information

Package	Part Number	Shipping Option	Remarks
LQFP48	HK32AUTO39A-3ACET7	Tray	-
LQFP48	HK32AUTO39A-3ACET7-TR	Tape and reel	-
LQFP48	HK32AUTO39A-3ACET3	Tray	-
LQFP48	HK32AUTO39A-3ACET3-TR	Tape and reel	-
LQFP64	HK32AUTO39A-3ARET3	Tray	-
LQFP64	HK32AUTO39A-3ARET3-TR	Tape and reel	-
LQFP100	HK32AUTO39A-3AVET3	Tray	-
LQFP100	HK32AUTO39A-3AVET3-TR	Tape and reel	-

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DCMI	Digital Camera Memory Interface
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
FM	Fast Mode
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSB	Least Significant Bit
LSE	Low-Speed External (clock signal)
LSI	Low-speed Internal (clock signal)
LVD	Low Voltage Detector
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSPS	Million Samples per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PVD	Programmable Voltage Detector
PWM output	Pulse Width Modulation
QSPI	Queued Serial Peripheral Interface
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTC	Real-time Clock
SAI	Serial Audio Interface
SDIO	Secure Digital Input and Output
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
TRNG	True Random Number Generator
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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