HK32ASPIN02x Datasheet

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Shenzhen Hangshun Chip Technology R&D Co., Ltd.

http://www.hsxp-hk.com

Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32ASPIN02x series microcontrollers (MCUs). It helps you quickly understand the characteristics and functions of HK32ASPIN02x.

Audience

This document is intended for:

- HK32ASPIN02x developers
- HK32ASPIN02x testers
- HK32ASPIN02x users

Release Notes

This document is applicable to HK32ASPIN02x series MCUs.

Revision History

Version	Date	Description
1.0	2022/12/08	The initial release.
1.1	2024/01/05	1. Added the part number HK32ASPIN022K8U7 of the QFN32 package and updated the Device overview, Pinouts and pin descriptions, Packages, and Ordering information sections accordingly. 2. Updated Figure 3-1 HK32ASPIN021C8T7 block diagram. 3. Updated Figure 3-2 HK32ASPIN021C8T7 memory mapping. 4. Updated Figure 3-3 Reset signal. 5. Updated the maximum T_L value in section "4.2.20 Temperature sensor characteristics". 6. Updated the pinout figures and pin descriptions in section "6 Pinouts and pin descriptions": added the GPIO description to NRST and Boot0 pins. 7. Added the description that UART and I2C support the exchange of pin functions to sections "6.6 Pin descriptions" and "6.7 Alternate function table". 8. Updated the QFN32 package outline and parameters in section "7.1.4 QFN32". 9. Added sections "7.2 Device marking" and "8.1 Device numbering conventions". 10. Updated section "7.2.5 TSSOP24 marking".

Contents

1 Introduction

This document is the datasheet for HK32ASPIN02x series MCUs. HK32ASPIN02x is a family of cost-effective MCUs developed specifically for motors by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32ASPIN020:
  - HK32ASPIN020E8P7 (TSSOP24 package)
  - HK32ASPIN020K8T7 (LQFP32 package)
  - HK32ASPIN020S8T7 (LQFP44 package)
- HK32ASPIN021:
  - HK32ASPIN021K8T7 (LQFP32 package)
  - HK32ASPIN021C8T7 (LQFP48 package)
- HK32ASPIN022:
  - HK32ASPIN022K8U7 (QFN32 package)
  - HK32ASPIN022K8T7 (LQFP32 package)
  - HK32ASPIN022C8T7 (LQFP48 package)

For more details of HK32ASPIN02x, see *HK32ASPIN02x User Manual*.

2 Product overview

HK32ASPIN02x is a family of MCUs developed specifically for motors. It adopts the ARM® Cortex®-M0 core and incorporates the patented electric motor acceleration (EMACC) unit of Hangshun. The maximum operating frequency of HK32ASPIN02x can reach 80 MHz. Each HK32ASPIN02x MCU has 60 Kbytes of Flash and eight Kbytes of SRAM.

HK32ASPIN02x embeds a 16-bit advanced timer (four PWM output channels in total, three of which have complementary PWM outputs with programmable inserted dead-times), four 16-bit general-purpose timers, and a 32-bit general-purpose timer.

The analog circuitry embedded in HK32ASPIN02x includes a 12-bit ADC (simultaneous sample and hold by two sample and hold units, with 16 channels), two operational amplifiers (OPAMPs) that can operate in PGA mode, three voltage comparators (comparator threshold output from DAC), a power-on reset (POR)/power-down reset (PDR)/brown-out reset (BOR) circuitry, a temperature sensor, and an internal reference voltage (for internal ADC sampling).

Except for the power pins, ground pins, and NRST pin, all the other pins of HK32ASPIN02x can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided. All I/Os support 5 V input and output.

HK32ASPIN02x supports the conventional Flash read/write protection and also offers the patented Flash code encryption function of Hangshun. To meet the data integrity check as well as the encryption and decryption requirements of various applications, HK32ASPIN02x provides the cyclic redundancy check (CRC) hardware unit. You can configure the Flash control register to remap interrupt vectors in the main Flash.

HK32ASPIN02x incorporates several communication interfaces: six UART interfaces, a high-speed SPI, an I2C interface, and a CAN interface.

HK32ASPIN02x also integrates the division and square root (DVSQ) calculation unit that provides higher performance than software and faster responses to external events.

HK32ASPIN02x provides Sleep and Stop low-power modes that can meet the requirements of power consumption-sensitive applications.

With the diversified peripherals, HK32ASPIN02x is best suited for the square wave control and field-oriented control (FOC) of the brushless direct current (BLDC) motor and permanent magnet synchronous motor (PMSM):

- Electric tools
- Industrial fans
- Compressors
- Electric vehicles
- Range hoods
- Vacuum cleaners
- Water pumps
- Ceiling fans
- Air conditioners

2.1 Features

- CPU core
  - ARM® Cortex®-M0
  - Maximum frequency: 80 MHz
  - 24-bit SysTick timer

- Supports the remapping of interrupt vectors (by configuring the Flash control register)

- Operating voltage range
  - Single power domain (main power supply V_{DD}): 2.2 V to 5.5 V
- Operating temperature range: –40°C to +105°C
- Typical operating current
  - Run mode 1.8 mA@3.3 V
  - Sleep mode 364 µA@3.3 V
  - Stop mode: 361 µA@3.3 V
- Memory
  - 60-Kbyte Flash
    - No wait states to access Flash when the CPU frequency is 24 MHz or lower
    - Separate read and write protection for Flash data
    - Encryption for instructions and data stored in the Flash, preventing the damage caused by physical attacks
  - 8-Kbyte SRAM
- Clocks
  - High-speed external clock (HSE): 4 – 24 MHz (typical value: 8 MHz)
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): 8 MHz (HSI)/14 MHz (HSI14)/56 MHz (HSI56) configurable
  - Low-speed internal clock (LSI): 32.768 kHz
  - PLL output clock: 80 MHz (maximum value)
  - GPIO external input clock: 30 MHz (maximum value)
- Resets
  - External pin reset (NRST pin)
  - Option byte loading (OBL) reset
  - Window watchdog counting terminates (WWDG reset)
  - Independent watchdog counting terminates (IWDG reset)
  - Power reset (POR/PDR/BOR)
  - Software reset (SW reset)
- Programmable voltage detector (PVD)
  - Adjustable 14-level thresholds for detected voltage
  - Rising edge or falling edge detection configurable
- GPIO
  - Provides up to 42 GPIOs
  - All GPIOs support 5 V input/output
- 2 × DMA controllers
  - Each has five channels for the selection of different request sources
  - Can be triggered by multiple peripherals such as the timer, SPI, I2C, UART, and ADC
- Data communication interfaces
  - 6 × UARTs

- 1 × I2C
  - Transmission rate at 1 Mbit/s, 400 kbit/s, or 100 kbit/s
  - Can wake up the MCU from Stop mode when receiving data
- Up to 1 × high-speed SPI
  - Transmission rate at up to 18 Mbit/s
- 1 × 2.0A/2.0B CAN

- Timers
  - 1 × 16-bit advanced timer: TIM1
    - Four PWM outputs, three of which with programmable inserted dead-times
    - Supports the break function triggered by signals output from external pins or internal comparators
    - The outputs of CC4 to CC6 can trigger ADC at multiple points in time.
  - 5 × general-purpose timers
    - 1 × 32-bit general-purpose timer: TIM2
    - 4 × 16-bit general-purpose timers: TIM3/TIM14/TIM15/TIM16
- Division and square root (DVSQ) calculation unit
  - Supports 32-bit fixed point division, with the quotient and remainder calculated
  - Supports 32-bit fixed point high-precision root calculation
- Electric motor acceleration (EMACC)
  - Supports the coordinate rotation digital computer (CORDIC) algorithm for sine and cosine
  - Supports Clarke, Park, and Inverse Park transformations
  - Supports space vector pulse width modulation (SVPWM)
  - Supports 1 × high-speed motor data transmission channel (Trace)
- Data security
  - Cyclic redundancy check (CRC) hardware implementation unit
- On-chip analog circuitry
  - 1 × 12-bit SAR ADC with two sample and hold units (up to 16 analog input channels)
    - Maximum frequency: 2 MSPS (12-bit)
    - Two independent sample and hold units, which can sample two signals simultaneously
    - Supports the conversion by four independent regular queues and a test queue
    - Supports automatic continuous conversion and scan conversion
    - In regular queues, the conversion request of a channel can be redirected to another channel
    - Supports multiple hardware trigger sources (such as TIM1_TRGO, TIM1_CCx, and GPIO input events)
    - Supports the function of averaging the sampled data of multiple channels in regular queues
    - Independent register for each channel to save data
  - Internal reference voltage
    - The output of the internal reference voltage is connected to an independent ADC channel.
  - Temperature sensor
    - The temperature sensor output is connected to an independent ADC channel.

- 3 × voltage comparators (COMPs)
  - The reference voltage of the comparator is from the external signal input or internal 8-bit DAC.
  - The output of comparators can be used as the break of the advanced timer.
- 2 × operational amplifiers (OPAMPs)
  - Programmable amplification factor
  - The output pin of amplifiers can be used as an ADC sampling channel.

- 96-bit unique ID (UID) of each MCU
  - Used as the serial number and security key
  - Used to activate the secure boot process
- CPU trace and debug
  - Serial wire debug (SWD) interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Reliability
  - Passes HBM3000V/CDM2000V/LU200mA level tests (PC15 passes HBM500V, PF1 passes HBM1000V)

2.2 Device overview

Table 2-1 HK32ASPIN02x series features

Feature		HK32ASPIN021C8T7	HK32ASPIN022C8T7	HK32ASPIN020S8T7	HK32ASPIN020K8T7	HK32ASPIN021K8T7	HK32ASPIN022K8T7	HK32ASPIN022K8U7	HK32ASPIN020E8P7
GPIO		42	41	40	29	28	27	27	21
Package		LQFP48		LQFP44	LQFP32			QFN32	TSSOP24
Operating voltage		2.2 V – 5.5 V							
Operating temperature		–40°C to +105°C							
Memory	Flash (Kbyte)	60							
	SRAM (Kbyte)	8							
CPU	Core	Cortex®-M0							
	Frequency	80 MHz							
DMA (Channels)		2 (5 channels each)							
Division and square root (DVSQ) calculation unit		1							
Clock	LSI	32.768 kHz							
	HSI	Configurable to 8 MHz/14 MHz/56 MHz							
	PLL output clock	Supported							
	HSE	4 MHz – 24 MHz							
	LSE	32.768 kHz			Not supported				
Timer	Advanced timer	1 (16-bit): TIM1							
	General-purpose timer	1 (32-bit): TIM2 4 (16-bit): TIM3, TIM14, TIM15, TIM16							
	SysTick	1							

Feature		HK32ASPIN021C8T7	HK32ASPIN022C8T7	HK32ASPIN020S8T7	HK32ASPIN020K8T7	HK32ASPIN021K8T7	HK32ASPIN022K8T7	HK32ASPIN022K8U7	HK32ASPIN020E8P7
	timer								
	IWDG	1							
	WWDG	1							
Comm. peripheral	UART	6							
	I2C	1							
	SPI	1							Not supported
	CAN	1							
IRTIM		1							
ADC	ADC (External channels)	1 (12)	1 (12)	1 (12)	1 (10)	1 (10)	1 (10)	1 (10)	1 (9)
	Reference selection	Internal reference voltage							
	ADC conversion frequency	2 MSPS (12-bit)							
	ADC accuracy	Configurable to 6/8/10/12-bit							
Temperature sensor		1							
Voltage comparator (COMP)		3							
Operational amplifier (OPAMP)		2							
Electric motor acceleration (EMACC)		1							
Programmable voltage detector (PVD)		1							
Info. security	CRC	1							
	96-bit UID	1							

3 Function description

3.1 Block diagram

HK32ASPIN02x integrates a Flash memory of 60 Kbytes to store programs and data.

ARM® Cortex®-M0 is a 32-bit RISC processor that delivers outstanding computational performance and advanced system responses to interrupts. With the ARM® Cortex®-M0 core embedded, the HK32ASPIN02x family is compatible with all ARM tools and software.

The following figure shows the block diagram of HK32ASPIN021C8T7 as an example:

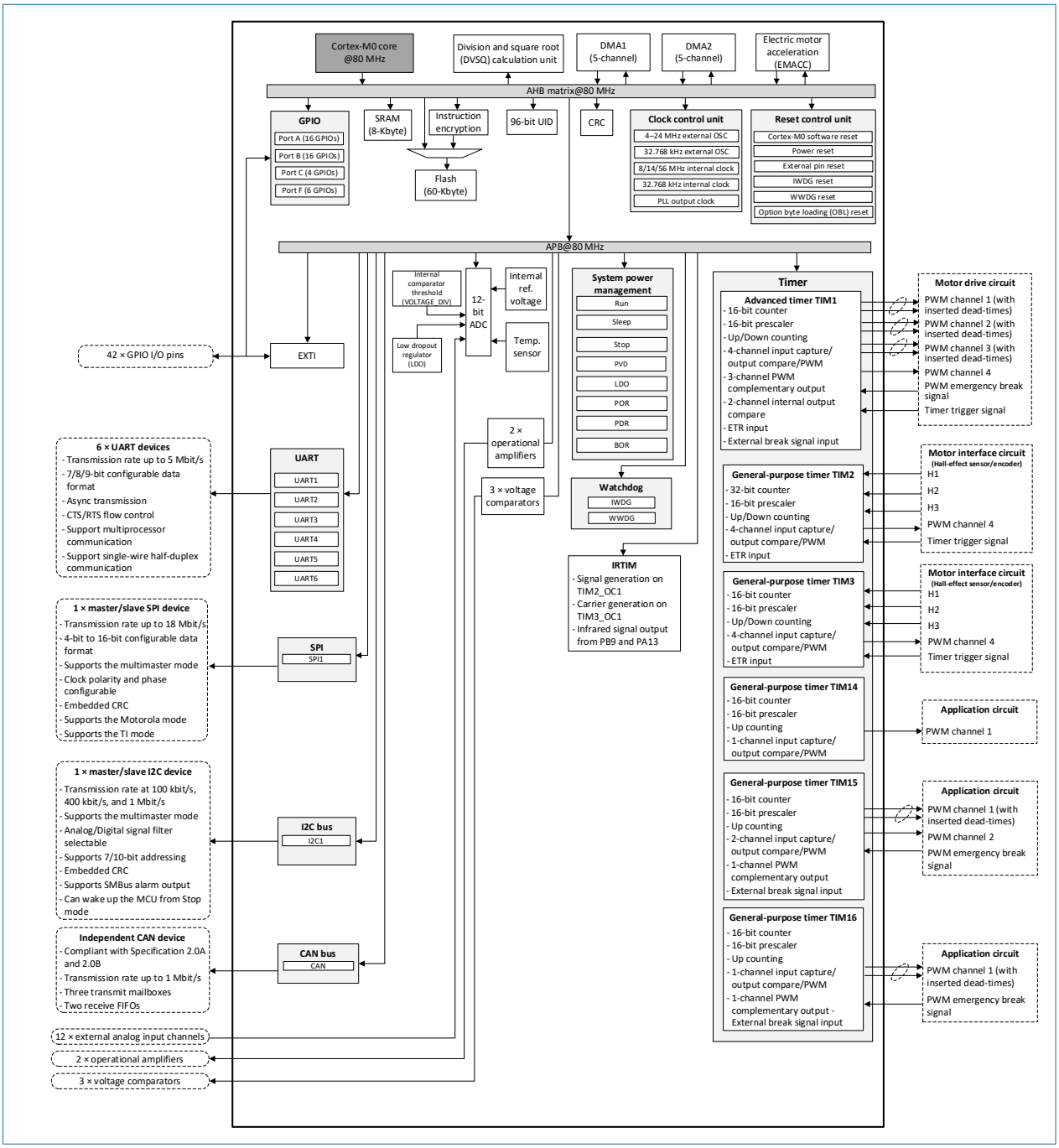

Figure 3-1 HK32ASPIN021C8T7 block diagram

3.2 Memory mapping

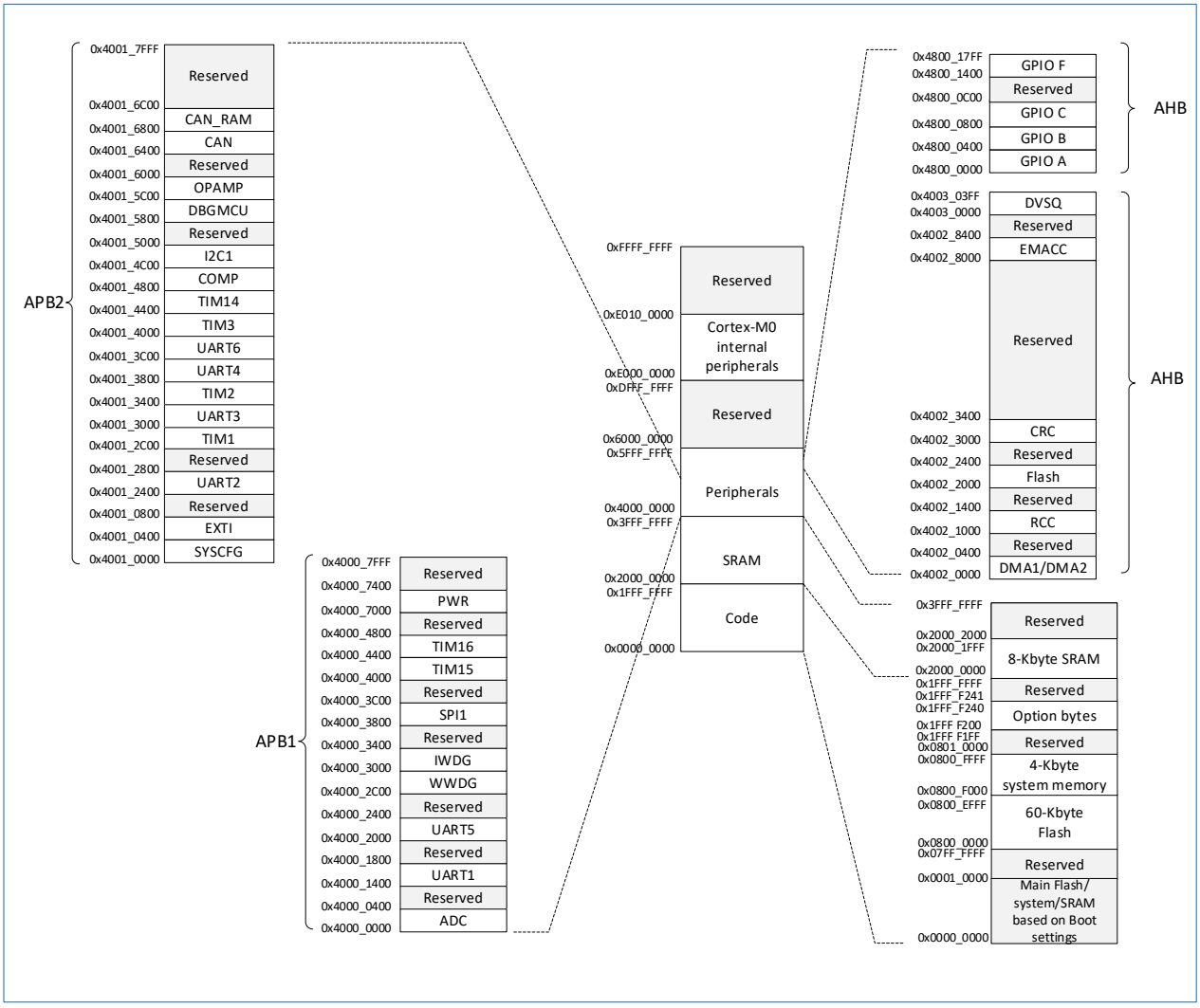

Figure 3-2 HK32ASPIN021C8T7 memory mapping

3.3 Memory

3.3.1 Flash

HK32ASPIN02x integrates a Flash memory of 60 Kbytes to store programs and data.

You can configure the Flash control register to remap interrupt vectors in the 60-Kbyte space.

3.3.2 SRAM

HK32ASPIN02x integrates an 8-Kbyte SRAM that can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait states, meeting the requirements of most applications.

3.4 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32ASPIN02x integrates a CRC hardware calculation unit. It is used to get a CRC code from an 8-, 16-, or 32-bit data word by using a generator polynomial.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with the reference signature that is generated at link time and stored at a specified memory location.

3.5 Power supply scheme

The V_{DD} ranging from 2.2 V to 5.5 V is the external power supply (no V_{BAT}) that supplies power to the digital

circuitry, I/O pins, and internal voltage regulator of the MCU.

3.6 Power supply monitor

HK32ASPIN02x MCUs contain the POR/PDR/BOR circuitry. When the supply voltage reaches 2.2 V, the MCU can work normally. When V_{DD}/V_{DDA} is lower than the specified V_{POR}/V_{PDR} threshold, the MCU will be reset without using any external reset circuit. During the power-on process, BOR guarantees that the MCU is in the reset state until the supply voltage reaches the specified V_{BOR} threshold. When BOR is disabled, the power-down is controlled by power-down reset (PDR).

The device incorporates a programmable voltage detector (PVD) which can monitor V_{DD} and V_{DDA} and compare them with the V_{PVD} threshold. The V_{PVD} threshold can be configured by using the software. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated. The interrupt program can send a warning message or set the MCU to the safe state. You can set the register to enable the PVD.

3.7 Boot modes

When the system starts, the boot pin is used to select one of the following boot modes:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram Flash via the UART1 (PA8/PA9) interface.

3.8 Low-power modes

HK32ASPIN02x supports Sleep and Stop low-power modes.

- Sleep mode: Only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.
- Stop mode: MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the phase-locked loop (PLL), HSE oscillator, and HSI oscillator are disabled. The MCU can be woken up from Stop mode by any extended interrupt/event controller (EXTI) line. The EXTI line source can be any of the 16 external I/O pins. I2C can wake up the MCU from Stop mode when receiving data.

3.9 Resets

3.9.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR. You can identify the reset source by checking reset status flags in the RCC_CSR register.

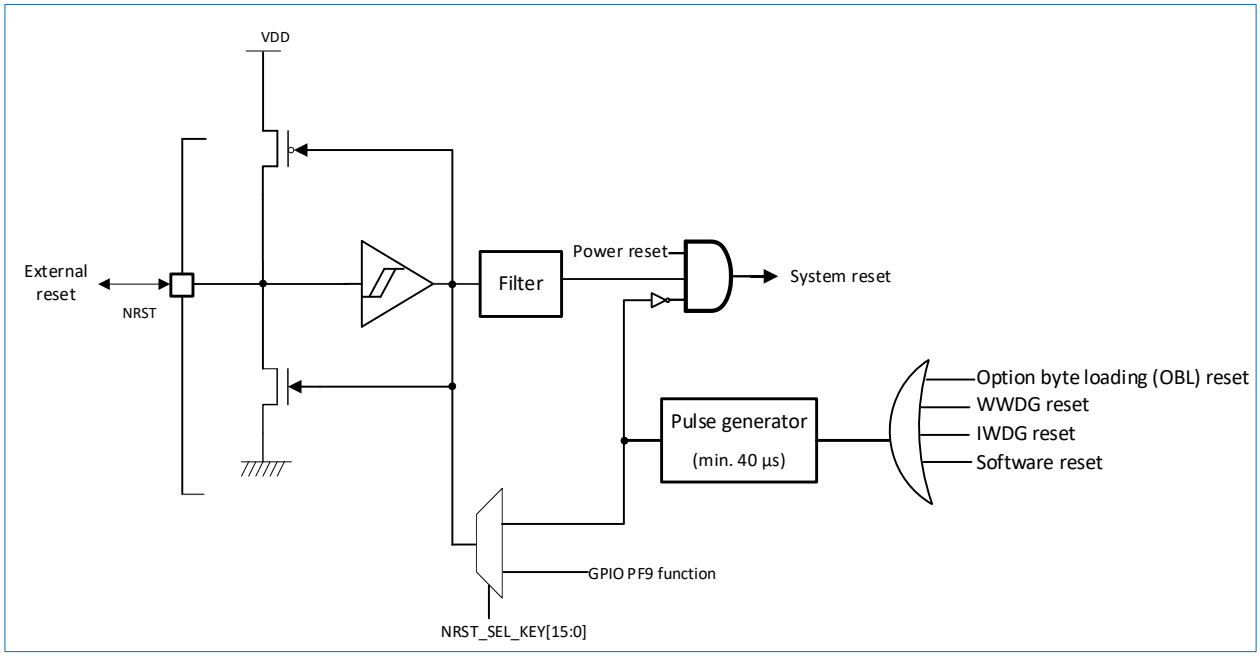

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Option byte loading (OBL) reset
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Power reset (POR/PDR/BOR)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.

The reset sources eventually act on the NRST pin. The NRST pin keeps the low level during resets. The reset entry vector is fixed on address 0x00000004. The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.9.2 Power reset

A power reset is generated when any of the following events occurs:

- Power-on reset (POR)/Power-down reset (PDR)
- Brown-out reset (BOR)

HK32ASPIN02x MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the 2.2 V threshold. When V_{DD} is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

HK32ASPIN02x also integrates the BOR. By default, BOR is unavailable. The power supply is under the monitoring of POR/PDR. You can configure the option byte to enable or disable BOR.

3.10 Clocks and clock tree

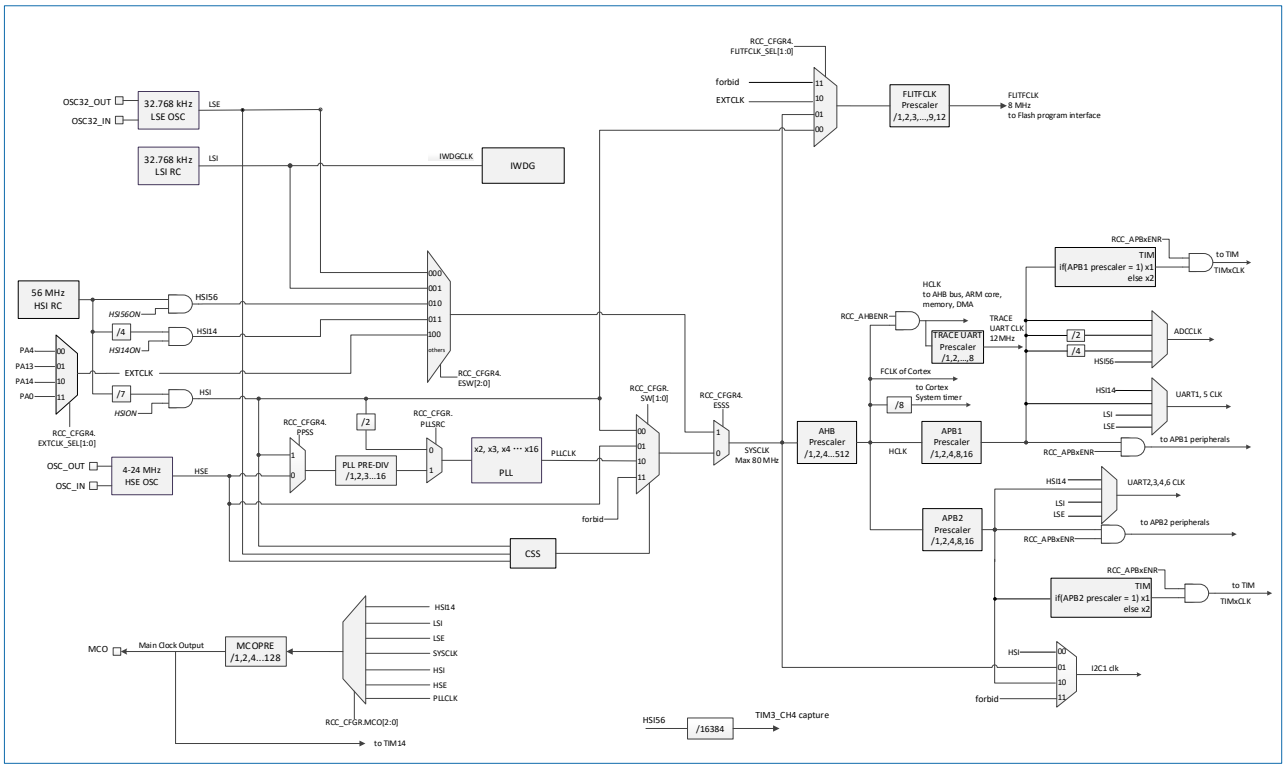

Figure 3-4 Clock tree

(1). Note: LSE is only available in LQFP48 and LQFP44 packages.

As the figure shows, HSI and HSI14 are generated by the same internal oscillator operating at 56 MHz. Therefore, when HSI or HSI14 is used, disabling the other clock cannot reduce power consumption. HSI/HSE can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI/HSE together with PLL to configure different system clock frequencies.

HK32ASPIN02x MCUs use SYSCLK as the CPU clock when they start. The internal RC oscillator outputs a 56 MHz clock. This 56 MHz clock divided by seven is the HSI that is used as the default system clock when the MCU is powered on.

HK32ASPIN02x provides more clock sources for the system clock and offers convenient, flexible, and diverse operating modes to customers. The following clocks can act as the system clock:

- High-speed external clock (HSE): 4 MHz to 24 MHz
- Low-speed external clock (LSE): 32.768 kHz
- High-speed internal clock (HSI): 8 MHz (HSI)/14 MHz (HSI14)/56 MHz (HSI56)
- Low-speed internal clock (LSI): 32.768 kHz
- PLL output clock: 80 MHz (maximum value)
- GPIO external input clock: 30 MHz (maximum value)

The clock frequency of the AHB and the APB domain can be configured by using several prescalers. The maximum clock frequency of the AHB can be 80 MHz. The maximum clock frequency of the APB domain can be 80 MHz.

The clock security system (CSS) supervises the HSE and LSE and switches to another clock source when it detects faults.

3.11 Interrupts and events

3.11.1 NVIC

HK32ASPIN02x incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 31 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities while maintaining the lowest interrupt latency.

- The NVIC closely coupled with the core interface ensures low latencies in interrupt processing.
- The interrupt entry vector address is directly passed to the core.
- Supports the early processing of interrupts.
- Processes late-arriving interrupts that have higher priorities.
- Supports tail-chaining.
- The processor state is automatically saved.
- The previous state is resumed upon interrupt exit with no extra instructions needed.

Table 3-1 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	–3	Fixed	Reset	Reset	0x0000 0004
-	–2	Fixed	NMI	Non-maskable interrupt. The clock security system (CSS) is connected to the non-maskable interrupt (NMI) vector.	0x0000 0008
-	–1	Fixed	HardFault	All classes of fault	0x0000 000C
-	3	Configurable	SVCall	System service call via SWI instruction	0x0000 002C
-	5	Configurable	PendSV	Pendable request for system service	0x0000 0038
-	6	Configurable	SysTick	System tick timer	0x0000 003C
0	7	Configurable	WWDG	Window watchdog interrupt	0x0000 0040
1	8	Configurable	PVD	PVD interrupt (combined with EXTI line 16)	0x0000 0044
2	9	-	-	Reserved	0x0000 0048
3	10	Configurable	FLASH	Flash global interrupt	0x0000 004C
4	11	Configurable	RCC	RCC global interrupt	0x0000 0050
5	12	Configurable	EXTI0_1	EXTI line [1:0] interrupts	0x0000 0054
6	13	Configurable	EXTI2_3	EXTI line [3:2] interrupts	0x0000 0058
7	14	Configurable	EXTI4_15	EXTI line [15:4] interrupts	0x0000 005C
8	15	Configurable	DMA1_CH1	DMA1 channel 1 interrupt	0x0000 0060
9	16	Configurable	DMA1_CH2_3	DMA1 channel 2/3 interrupt	0x0000 0064
10	17	Configurable	DMA1_CH4_5	DMA1 channel 4/5 interrupt	0x0000 0068
11	18	Configurable	ADC	ADC global interrupt	0x0000 006C
12	19	Configurable	TIM1	TIM1 global interrupt	0x0000 0070
13	20	Configurable	UART1	UART1 global interrupt	0x0000 0074
14	21	Configurable	TIM2	TIM2 global interrupt	0x0000 0078
15	22	Configurable	TIM3	TIM3 global interrupt	0x0000 007C
16	23	Configurable	UART3	UART3 global interrupt	0x0000 0080
17	24	Configurable	UART4	UART4 global interrupt	0x0000 0084
18	25	Configurable	TIM14	TIM14 global interrupt	0x0000 0088

Position	Priority		Name	Description	Address
19	26	Configurable	TIM15	TIM15 global interrupt	0x0000 008C
20	27	Configurable	TIM16	TIM16 global interrupt	0x0000 0090
21	28	Configurable	DMA2_CH1	DMA2 channel 1 interrupt	0x0000 0094
22	29	Configurable	DMA2_CH2_3	DMA2 channel 2/3 interrupt	0x0000 0098
23	30	Configurable	DMA2_CH4_5	DMA2 channel 4/5 interrupt	0x0000 009C
24	31	Configurable	I2C1_SPI1	I2C1 and SPI1 global interrupt I2C1 wakeup interrupt (combined with EXTI line 21)	0x0000 00A0
25	32	Configurable	UART2	UART2 global interrupt	0x0000 00A4
26	33	Configurable	EMACC	EMACC global interrupt	0x0000 00A8
27	34	Configurable	CAN	CAN global interrupt	0x0000 00AC
28	35	Configurable	DVSQ	DVSQ global interrupt	0x0000 00B0
29	36	Configurable	COMP1_COMP2_COMP3	COMP1/COMP2/COMP3 global interrupt (combined with EXTI lines 18/19/20)	0x0000 00B4
30	37	Configurable	UART5	UART5 global interrupt	0x0000 00B8
31	38	Configurable	UART6	UART6 global interrupt	0x0000 00BC

3.11.2 EXTI

The extended interrupt/event controller (EXTI) manages asynchronous interrupts and events. It outputs event requests to the CPU, outputs interrupt requests to the interrupt controller, and outputs wakeup requests to the power supply management module.

EXTI can be categorized into edge-configurable EXTI and edge-fixed EXTI. For the edge-fixed EXTI, only the rising edge is the trigger edge. The EXTI only operates in Stop mode and is used to wake up the core from Stop mode.

- Manages up to 21 interrupt/event requests
  - 20 edge-configurable EXTI lines
    - Trigger edge configurable: rising edge or falling edge
    - Dedicated flag for the interrupt status bit
    - Interrupts and events can be triggered by software.
  - 1 edge-fixed EXTI line
- Each interrupt/event line can be triggered and masked independently.
- Detects external signals whose pulse width is shorter than the APB2 clock period.

3.12 GPIOs

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by the digital and analog alternate functions. All GPIOs are high current-capable. The configuration of I/O alternate functions can be locked as needed by performing a specific operation, which helps avoid unexpected writes to the I/O registers.

3.13 SYSCFG

The HK32ASPIN02x MCU has a set of system configuration registers. SYSCFG provides the following functions:

- Enable or disable the fast mode plus of I2C on some I/O ports.
- The CTS of UART can be remapped to RX and the RTS of UART can be remapped to TX.
- Remap the memory areas.
- Manage external interrupts connected to GPIOs.

- Manage the remapping of LSI, HSI, and LSE signals to TIM3_CH4.
- Manage the switch controlling the output of some internal analog signals to I/Os.
- Configure the internal voltage divider (8-bit DAC).

3.14 DMA

The direct memory access (DMA) controller is used for high-speed data transfer from peripherals to memories, from memories to memories, and from peripherals to peripherals. DMA can quickly move data to the destination without CPU intervention, saving CPU resources for other applications.

HK32ASPIN02x integrates two DMA controllers. Each DMA controller has five channels that are respectively dedicated for the management of memory access requests from one or multiple peripherals. The DMA controller has an arbiter to handle the priorities of different DMA requests.

- Provides five configurable independent channels.
- Each channel is connected to dedicated trigger hardware. The trigger by software is also supported.
- Supports circular buffer management.
- TIM1/2/3/15/16, SPI1, UART1/2/3/4/6, I2C1, and ADC can generate DMA requests.

3.15 COMP

HK32ASPIN02x has three extremely low-power voltage comparators: COMP1, COMP2, and COMP3. The three comparators can be used independently (via the corresponding GPIO), used for motor control, or used with timers.

- The comparator triggered by the analog signal can wake up the MCU from low-power modes.
- Used for analog signal conditioning.

3.16 OPAMP

The operational amplifier (OPAMP) can be flexibly configured to amplify signals and meet the requirements of motors. The two internal operational amplifiers can be configured as inverting and non-inverting combined operational amplifiers with different gains or be cascaded by using external resistors.

3.17 DVSQ

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - Supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports divide-by-zero interrupt and overflow interrupt.

3.18 EMACC

Electric motor acceleration (EMACC) can be used on brushless direct current (BLDC) motors controlled by the field-oriented control (FOC) algorithm. EMACC accelerates the mathematical operations of motor drives. Mathematical operations can be completed at a speed higher than that of software-based mathematical operations while occupying fewer CPU resources. The EMACC-embedded MCUs support higher motor rotation speeds and improved drive frequencies under the same CPU frequency.

On HK32ASPIN02x MCUs, the coordinate rotation digital computer (CORDIC) algorithm, Clarke, Park, and Inverse Park transformations, proportional-integral-derivative (PID) control, and space vector pulse width modulation (SVPWM) module of the FOC algorithm are based on hardware. This helps free up CPU resources and speed up computing. Users input Ia, Ib, and the θ electrical angle. After the processing by EMACC, the output of SVPWM, such as the PWM duty cycle of A, B, and C phases, can be obtained. EMACC further decreases the time consumed by the FOC algorithm.

HK32ASPIN02x contains a data tracker (EMACC_TRACE) which is a high-speed serial interface hardware module. During the motor commissioning or high-speed running process, EMACC_TRACE outputs EMACC parameters in real time. In addition, four bytes are provided for the output of user-defined data, which facilitates motor commissioning.

EMACC can significantly increase algorithm efficiency.

3.19 Timers

The HK32ASPIN02x MCU has an advanced timer and five general-purpose timers. The following table describes the functions of timers.

Table 3-2 Functions of timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	1 to 65536	Yes	Yes	4	3
General-purpose timer	TIM2	32-bit	Up, down, up/down	1 to 65536	Yes	No	4	No
	TIM3	16-bit	Up, down, up/down	1 to 65536	Yes	No	4	No
	TIM14	16-bit	Up	1 to 65536	No	No	1	No
	TIM15	16-bit	Up	1 to 65536	Yes	Yes	2	1
	TIM16	16-bit	Up	1 to 65536	Yes	Yes	1	1

3.19.1 Advanced timer

HK32ASPIN02x integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of the advanced timer can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

- Two extra internal channels for output compare

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If TIM1 is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). Many functions of TIM1 are the same as those of the general-purpose timer. Therefore, the advanced timer can work together with the general-purpose timer through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

3.19.2 General-purpose timer

HK32ASPIN02x integrates five general-purpose timers.

- TIM2 and TIM3

  TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have four independent channels respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output.

  TIM2 and TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14

  TIM14 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 has one channel for input capture, output compare, PWM output, and one-pulse mode output. In debug mode, the counter can be frozen. TIM14 cannot generate DMA requests.

- TIM15 and TIM16

  TIM15 and TIM16 are both based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM15 and TIM16 both have complementary outputs with programmable inserted dead-times and can generate independent DMA requests. TIM15 has two channels. TIM16 has one channel. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output. In debug mode, the counter can be frozen.

3.19.3 SysTick timer

SysTick timer is a dedicated timer of the operating system. It is a standard downcounter with the following features:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.20 IRTIM

An infrared interface (IRTIM) is embedded in HK32ASPIN02x MCUs. The IRTIM works with infrared LEDs to provide the remote control function. To generate infrared remote control signals, you must enable the IRTIM (PB9/PA13) and configure TIM2 channel 1 (TIM2_OC1) and TIM3 channel 1 (TIM3_OC1).

The infrared receiver function can be implemented by setting TIM2 channel 1 and TIM3 channel 1 to the basic input capture mode.

3.21 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 32.768 kHz RC oscillator (LSI). The RC oscillator is independent of the main clock, so it can operate in Stop mode. The IWDG can reset the system when a problem occurs or work as a free-running timer to provide timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the window register IWDG_WINR to use IWDG in window mode.

3.22 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free

running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.23 ADC

HK32ASPIN02x incorporates a 12-bit analog-to-digital converter (ADC) which has a total of 12 external channels and four internal channels. The A/D conversions of the channels can be performed in single, continuous, scan, or discontinuous mode.

- ADC clock frequency up to 28 MHz, and ADC conversion frequency up to 2 MSPS
- Two independent sample and hold units whose inputs are from the 16 analog input channels
- The ADC can be served by the DMA controller.
- Flexible queue configuration: four independent regular queues and a test queue
- Flexible arbitration mechanism: a priority from 0 to 3 for each queue. A larger number indicates a higher priority.
- Independent register for each channel to store the conversion result
- Supports the configuration of trigger latency. The ADC conversion starts after the latency elapsed from when the trigger signal is generated.
- The events generated by general-purpose timers (TIM2/TIM3/TIM15) and advanced timer (TIM1) can be internally connected to the ADC start trigger so that A/D conversions can be triggered.

3.23.1 Temperature sensor

The temperature sensor is used to measure the ambient temperature of the device.

3.23.2 Internal reference voltage

The internal reference voltage V_{REFINT} provides a stable voltage output (bandgap voltage reference) for the ADC.

3.24 I2C bus

HK32ASPIN02x has an I2C bus interface that can work in multimaster mode or slave mode. The I2C interface supports the standard mode (up to 100 kHz), fast mode (up to 400 kHz), and fast mode plus (up to 1 MHz) and has an output drive of 15 mA.

The I2C interface provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, host notify protocol, hardware CRC (PEC) generation and verification, timeout verification, and ALERT protocol management.

The I2C interface has a clock independent of the CPU clock domain, so it can wake up the MCU from Stop mode when the address is matched.

Table 3-3 I2C features

I2C Feature	I2C1
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast/Fast mode plus	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
DMA transmission	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

3.25 UART

Six universal asynchronous receivers/transmitters (UART1/UART2/UART3/UART4/UART5/UART6) are embedded in the HK32ASPIN02x MCU and can communicate at up to 10 Mbit/s. This module provides hardware management for the CTS, RTS, and RS485DE signals, multiprocessor communication mode, and single-wire half-duplex communication mode. The UARTs can be served by the DMA controller.

Table 3-4 UART features

UART Mode/Feature	UART1/UART2/UART3/UART4/UART5/UART6
Data word length	7/8/9-bit
DMA transmission	Supported (except for UART5)
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported
RS232 hardware flow control	Supported
RS485 driver enable	Supported

3.26 SPI

Up to one serial peripheral interface (SPI) is embedded in each HK32ASPIN02x MCU. The SPI interface supports full-duplex and half-duplex communication in master or slave mode. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to a value from 4-bit to 16-bit.

Table 3-5 SPI features

SPI Feature	SPI1
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported
DMA transmission	Supported

3.27 CAN

The controller area network (CAN) interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit the standard frames with 11-bit identifiers and the extended frames with 29-bit identifiers. The CAN interface has three transmit mailboxes and two three-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.28 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32ASPIN02x MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) as needed. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot process that has a security mechanism.

3.29 Debug port

Based on the ARM SWJ-DP embedded in HK32ASPIN02x, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Caution:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	5.8	V
V_{IN}	Input voltage on pins	–0.3	5.8	
$\|V_{SSX} – V_{SS}\|$	Variation between different ground pins	-	50	mV

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	105	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current sourced by any I/O and control pin	16	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	–5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	–25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	–55	130	°C
T_J	Maximum junction temperature	–45	110	°C

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	80	
f_{PCLK2}	Internal APB2 clock frequency	-	80	
V_{DD}	Standard operating voltage	2.2	5.5	V
V_{DDA}(1)	Analog operating voltage	2.2	5.5	V

Symbol	Description	Min	Max	Unit
T	Operating temperature	–40	105	°C

(1). V_{DDA} can be lower than V_{DD}. For example, V_{DD} = 4.2 V, V_{DDA} = 3.3 V; V_{DD} = 3.3 V, V_{DDA} = 2.5 V.

4.2.2 PVD

Table 4-5 PVD characteristics

Symbol	Parameter	Level	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (V_{DD} rising edge) (–40°C to 105°C)	V_{PVD2}	2.201	2.443	2.652	V
		V_{PVD3}	2.383	2.641	2.852	
		V_{PVD4}	2.582	2.841	3.052	
		V_{PVD5}	2.761	3.036	3.252	
		V_{PVD6}	2.940	3.220	3.453	
		V_{PVD7}	3.122	3.405	3.652	
		V_{PVD8}	3.279	3.586	3.852	
		V_{PVD9}	3.462	3.783	4.050	
		V_{PVD10}	3.643	3.975	4.252	
		V_{PVD11}	3.820	4.161	4.452	
		V_{PVD12}	4.021	4.375	4.650	
		V_{PVD13}	4.221	4.565	4.851	
		V_{PVD14}	4.381	4.744	5.003	
		V_{PVD15}	4.558	4.925	5.153	
	Programmable voltage detector level selection (V_{DD} falling edge) (–40°C to 105°C)	V_{PVD2}	2.097	2.288	2.497	
		V_{PVD3}	2.257	2.482	2.697	
		V_{PVD4}	2.439	2.674	2.895	
		V_{PVD5}	2.636	2.862	3.098	
		V_{PVD6}	2.798	3.057	3.296	
		V_{PVD7}	2.998	3.253	3.498	
		V_{PVD8}	3.179	3.453	3.697	
		V_{PVD9}	3.358	3.642	3.899	
		V_{PVD10}	3.538	3.841	4.097	
		V_{PVD11}	3.736	4.043	4.297	
		V_{PVD12}	3.917	4.236	4.497	
		V_{PVD13}	4.099	4.432	4.698	
		V_{PVD14}	4.297	4.634	4.896	
		V_{PVD15}	4.479	4.827	5.053	

4.2.3 BOR characteristics

Table 4-6 BOR characteristics

Symbol	Parameter	Level	Min	Typ	Max	Unit
V_{BOR}(1)	BOR detection level selection (V_{DD} rising edge) (–40°C to 105°C)	V_{BOR2}	2.099	2.287	2.352	V
		V_{BOR3}	2.352	2.467	2.550	
		V_{BOR4}	2.550	2.665	2.752	
		V_{BOR5}	2.702	2.860	2.951	
		V_{BOR6}	2.902	3.052	3.150	
		V_{BOR7}	3.100	3.251	3.353	
		V_{BOR8}	3.303	3.460	3.552	
		V_{BOR9}	3.451	3.646	3.752	
		V_{BOR10}	3.651	3.839	3.952	
		V_{BOR11}	3.851	4.042	4.152	
		V_{BOR12}	4.049	4.244	4.352	
		V_{BOR13}	4.200	4.437	4.552	
		V_{BOR14}	4.402	4.647	4.801	
		V_{BOR15}	4.646	4.817	4.897	
	BOR detection level selection (V_{DD} falling edge) (–40°C to 105°C)	V_{BOR2}	2.096	2.221	2.296	
		V_{BOR3}	2.246	2.409	2.498	
		V_{BOR4}	2.447	2.601	2.698	
		V_{BOR5}	2.595	2.786	2.897	
		V_{BOR6}	2.797	2.969	3.096	
		V_{BOR7}	2.997	3.164	3.298	
		V_{BOR8}	3.198	3.373	3.496	
		V_{BOR9}	3.295	3.564	3.696	

Symbol	Parameter	Level	Min	Typ	Max	Unit
		V_{BOR10}	3.494	3.746	3.897	
		V_{BOR11}	3.747	3.957	4.095	
		V_{BOR12}	3.946	4.162	4.295	
		V_{BOR13}	4.095	4.364	4.547	
		V_{BOR14}	4.294	4.567	4.746	
		V_{BOR15}	4.646	4.817	4.897	
$V_{BORhyst}$	BOR hysteresis	-	60	77	93	mV
t_{BORRST}(2)	Time for BOR to take effect after reaching the threshold	-	-	50	-	µs

(1). BOR is based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.4 POR/PDR characteristics

Table 4-7 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge	1.899	2.006	2.104	V
		Rising edge	1.920	2.026	2.141	V
$V_{PDRhyst}$	PDR hysteresis	-	0	21	45	mV
$t_{RSTTEMPO}$(2)	Reset duration	-	-	4	-	ms

(1). PDR and POR are based on the monitoring of only V_{DD}.

(2). The value is guaranteed in design.

4.2.5 Internal reference voltage

Table 4-8 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 105°C	-	1.2	-	V

4.2.6 Operating current characteristics

Table 4-9 Operating current characteristics

Mode	Condition	Parameter	V_{DD} = 3.3 V			Unit
			–40°C	25°C	105°C	
Run mode	HSI = 8 MHz, V_{DD} = 3.3 V APB disabled	Operating current	1.773	1.818	1.867	mA
Sleep mode	LSI = 32.768 kHz, V_{DD} = 3.3 V APB disabled	Operating current	344	364	399	µA
		Wakeup time	-	29.8	-	µs
Stop mode	V_{DD} = 3.3 V	Operating current	340	361	395	µA
		Wakeup time	-	33	-	µs

4.2.7 HSE clock characteristics

Table 4-10 HSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	24	MHz
R_F(1)	Feedback resistor	-	-	2	-	MΩ
$T_{stb\ (HSE)}$(2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	2	-	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (R_S)		-	12	-	pF
$I_{DD\ (HSE)}$(1)	HSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12 pF	20	-	140	µA

(1). The value is guaranteed in design.

(2). $T_{stb\ (HSE)}$ refers to the time from HSE startup to the time when it outputs stable frequency signals.

HK32ASPIN02x integrates an HSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

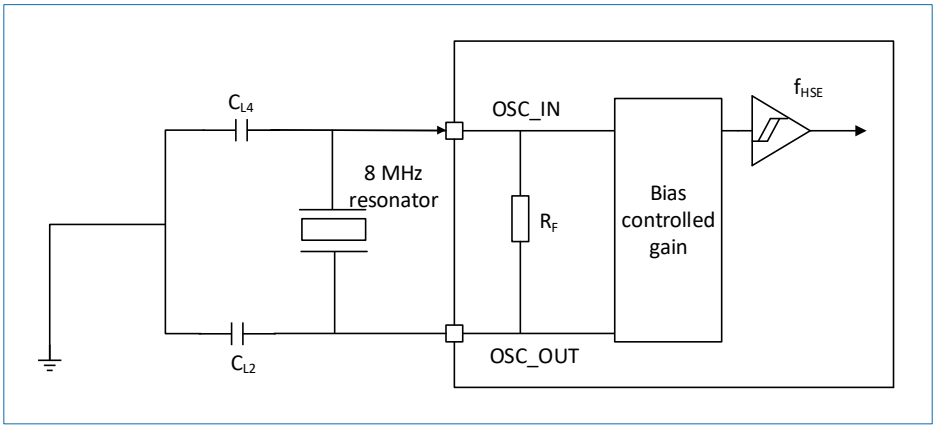

Figure 4-1 HSE negative feedback circuit

Alternatively, an HSE signal can be directly input from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-11 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	-	-	30	MHz
$DuCy_{(HSE)}$(1)	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.8 LSE clock characteristics

Table 4-12 LSE clock characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F(1)	Feedback resistor	-	-	10	-	MΩ
$T_{stb\ (LSE)}$(2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	2000	-	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12	-	pF
$I_{DD\ (LSE)}$(1)	LSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12 pF	-	150	-	nA

(1). The value is guaranteed in design.

(2). $T_{stb\ (LSE)}$ refers to the time from LSE startup to the time when it outputs stable frequency signals.

HK32ASPIN02x integrates an LSE negative feedback oscillator circuit. The following startup circuit outside the chip is recommended:

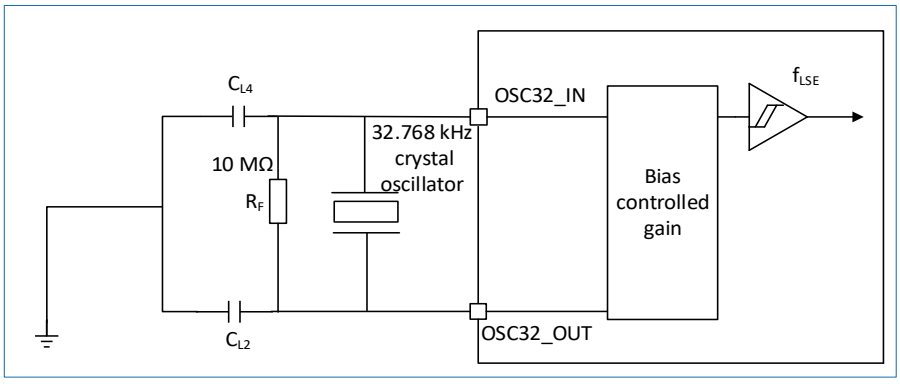

Figure 4-2 LSE negative feedback circuit

Alternatively, an LSE signal can be directly input from the OSC32_IN pin. The following table lists the requirements for this clock signal:

Table 4-13 Characteristics of the input LSE clock (1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	-	32.768	-	kHz
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%

(1). The value is guaranteed in design.

4.2.9 HSI clock characteristics

Table 4-14 HSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	8	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-	45	-	55	%
$ACC_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	–1	-	1	%
		Factory calibration: T_A = –40°C to +105°C	–1	-	0.7	
$T_{stb\ (HSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	5	10	µs
$I_{DD\ (HSI)}$(1)	Oscillator power consumption	8 MHz, V_{DD} = 3.3 V	-	81	101	µA

(1). The value is guaranteed in design.

4.2.10 LSI clock characteristics

Table 4-15 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	-	32.768	-	kHz
$T_{su\ (LSI)}$(1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	120	240	µs
$I_{DD\ (LSI)}$(1)	Oscillator power consumption	-	-	500	-	nA

(1). The value is guaranteed in design.

4.2.11 PLL characteristics

Table 4-16 PLL characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	5	30	MHz
	Input clock duty cycle	45	-	55	%
f_{PLL_OUT}	Output clock frequency	30	-	80	MHz
t_{LOCK}	PLL lock time	-	50	100	µs

(1). The value is guaranteed in design.

4.2.12 Flash memory characteristics

Table 4-17 Flash memory characteristics

Symbol	Parameter	Min	Typ(1)	Max	Unit
T_{PROG}	One-word programming time	73	73	76	µs
T_{ERASE}	Page erase time	4.056	4.056	5.056	ms
	Mass erase time	486.72	486.72	606.72	ms
IDD_{PROG}	Programming current	-	-	3.5	mA
IDD_{ERASE}	Page/Mass erase current	-	-	2	mA
IDD_{READ}	Read current	0.2 (@1 MHz)	3 (@40 MHz)	4.5 (@40 MHz)	mA
N_{END}	Erasure endurance	2	-	-	10k cycles
t_{RET}	Data retention	100 (25°C)	-	-	Years

(1). The typical values are obtained in the following conditions: 1.5 V, TT process corner, 25°C.

4.2.13 I/O pin input characteristics

Table 4-18 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 2.2 V – 5.5 V	0.42 × (V_{DD} – 2 V) + 1 V	-	5.5	V
V_{IL}	Input low level voltage	V_{DD} = 2.2 V – 5.5 V	–0.3	-	0.32 × (V_{DD} – 2 V) + 0.75 V	V
V_{IHhys}	Input high level voltage	V_{DD} = 5.5 V	2.6	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 5.5 V	-	-	2.3	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 2.2 V – 5.5 V	5% × V_{DD}(2)	-	-	mV
I_{lkg}	Input leakage current	V_{DD} = 2.2 V – 5.5 V V_{IN} = 5 V	-	-	3	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	5	-	pF

(1). The value is guaranteed in design.

(2). The minimum value is 100 mV.

4.2.14 I/O pin output characteristics

Table 4-19 I/O pin output direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	2.2 V ≤ V_{DD} ≤ 5.5 V	V_{DD} – 0.5	-	-	V
V_{OL}	Output low level voltage	2.2 V ≤ V_{DD} ≤ 5.5 V	-	-	0.5	V

Table 4-20 I/O pin output alternating current characteristics

Mode OSPEEDy[1:0]	Symbol	Parameter	Condition	Min	Typ	Max	Unit
x0	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 2.2 V – 5.5 V	-	-	105	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	-	105	ns
01	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 2.2 V – 5.5 V	-	-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	-	25	ns
11	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 2.2 V – 5.5 V	-	-	8	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	-	8	ns

4.2.15 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuits.

Table 4-21 NRST pin input characteristics

Symbol	Parameter	Min	Max	Unit
T_{Noise}	Low level ignored duration	-	80	ns

4.2.16 TIM characteristics

Table 4-22 TIM characteristics (1)

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	-	40	MHz

(1). The value is guaranteed in design. $f_{TIMxCLK}$ = 80 MHz.

4.2.17 EMACC characteristics

Table 4-23 Motor drive frequency characteristics

System Clock	ADC Clock	Min	Typ	Max	Unit
80 MHz	$f_{PCLK} = f_{apb}$, $f_{ADC} = f_{PCLK}/4$	-	20	25	kHz

Table 4-24 Comparison between the software and the FOC algorithm with EMACC

Test Condition	Electrical Angle	Coordinate System Conversion	SVPWM	Total Time Consumption	Unit
System clock: 80 MHz (software-based motor library)	11.6	10	4.8	28.8	μs
System clock: 80 MHz (EMACC-powered motor library)	11.6	1.6	2.4	18	μs

4.2.18 ADC characteristics

Table 4-25 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when ADC is enabled	-	2.2	3.3	5.5	V
VREFP	Positive reference voltage	-	2.2	3.3	5.5	V
VREFN	Negative reference voltage	-	0	0	0.1	V
f_{ADC}	ADC clock frequency	-	0.3	14	42	MHz
f_S (1)	Sampling frequency	f_{ADC} = 14 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	VREFN	-	VREFP	V
R_{AIN} (1)	External input impedance	For details, see Table 4-26.				kΩ
R_{ADC} (1)	Sample switch resistance	-	-	-	1	kΩ
C_{ADC} (1)	Sample and hold capacitance	-	-	5	-	pF
$Jitter_{ADC}$	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S(1)	Sampling time	f_{ADC} = 14 MHz	-	1.5	-	Cycles
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz 12-bit resolution	-	14	-	Cycles

(1). The value is guaranteed in design.

The calculation formula of the maximum input impedance R_{AIN}:

$$\mathbf{R}_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-26 Maximum input impedance values (f_{ADC} = 14 MHz)

Sampling Cycles (Cycles)	Sampling Time t_S (μs)	Maximum Input Impedance (kΩ)
1.5	0.11	1.21
7.5	0.54	10.04
13.5	0.96	18.87
28.5	2.04	40.96
41.5	2.96	60.09
55.5	3.96	80.70
71.5	5.11	104.26
239.5	17.11	351.58

Table 4-27 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	$V_{DD} = V_{DDA}$ = 3.3 V	-	15	LSB
EO	Offset error(2)	f_{ADC} = 14 MHz	-	14	
EG	Gain error(3)	Test after ADC calibration	-	5	

Symbol	Parameter	Test Condition	Typ	Max	Unit
ED	Differential linearity error(4)		-	1	
EL	Integral linearity error(5)		-	1	

(1). Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3). Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4). Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5). Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With the restricted V_{DDA}, frequency, and temperature range, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

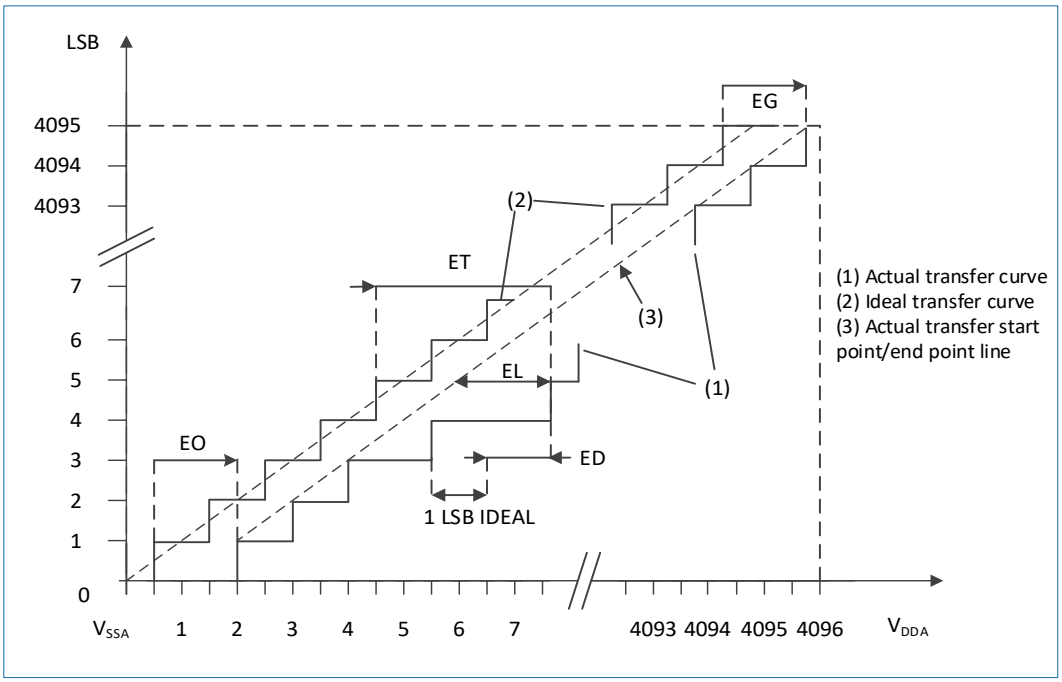

Figure 4-3 ADC accuracy characteristics

Note: For the explanations of EO, ET, EG, EL, and ED, see Table 4-27.

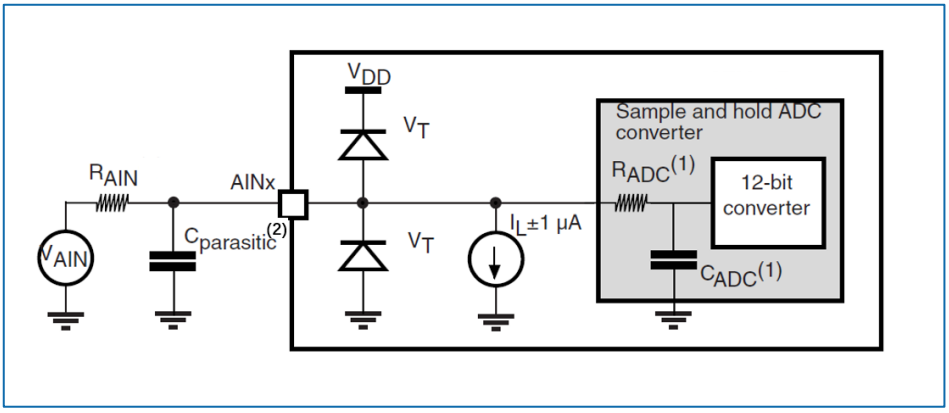

Figure 4-4 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-25.

$C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value reduces conversion accuracy, so f_{ADC} should be decreased.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following Figure 5-1. To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

4.2.19 DAC voltage divider characteristics

Table 4-28 DAC voltage divider characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when DAC is enabled	-	1.8	5	5.5	V
R_O	Output impedance	DAC buffer enabled	-	7	-	kΩ
I_{OUT}(1)	Output current	DAC buffer enabled	-	-	2	mA

(1). The value is guaranteed in design.

4.2.20 Temperature sensor characteristics

Table 4-29 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L	Temperature sensor linearity error	–20°C to 70°C	-	-	±6	°C
		–40°C to 105°C	-	-	±10	
V_{20}	Output voltage	20°C	-	936.6	-	mV
Avg_Slope	Temperature sensor slope	-	-	2.87	-	mV/°C

4.2.21 Voltage comparator (COMP) characteristics

Table 4-30 COMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	2.2	5	5.5	V
V_{com}	Input common mode voltage	-	–0.3	-	5.5	V
V_{diff}	Input differential mode voltage	V_{DDA} = 5 V, V_{com} = 2.5 V (no hysteresis)	5	-	-	mV
V_{hy}	Hysteresis voltage	Level 1	-	0	-	mV
		Level 2	-	30	-	
		Level 3	-	60	-	
		Level 4	-	100	-	
I_{OP}	Operating current (V_{DD} = 5 V)	Low-power mode	-	1	-	µA
		High-power mode	-	5.05	-	
T_{dly}(1)	Output delay (no hysteresis)	High-power mode Rising edge	37	-	86	ns
		Low-power mode Rising edge	572	-	998	
		High-power mode Falling edge	51	-	169	ns
		Low-power mode Falling edge	327	-	1200	

(1). The value is guaranteed in design.

4.2.22 Operational amplifier (OPAMP) characteristics

Table 4-31 OPAMP characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage	-	2.2	5	5.5	V
V_{OUT}	Output voltage	-	0.2	-	V_{DDA} – 0.2	V
CMIR	Input common mode	-	0	-	5.5	V

Item	Description	Condition	Min	Typ	Max	Unit
	voltage					
I_{load}	Output current	R_L = 100 Ω, V_{DDA} = 5 V	-	10	-	mA
I_q	Operating current	No load, static mode	438	900	1700	μA
I_I(1)	Leakage current	OPAMP disabled	-	3	275	nA
V_{OS}	Input bias voltage	Before calibration	-	±10	-	mV
		After calibration	-	-	±1.5	
CMRR	Common mode rejection ratio	-	51	-	145	dB
PSRR	Power supply rejection ratio	-	41	70	109.4	dB
GBW	Bandwidth	-	5.83	10	22.91	MHz
SR	Slew rate	-	5.9	-	21	V/μs
ϕ	Phase margin	-	47	60	71.62	Deg
PGA gain	PGA gain	Level 1	-	2	-	times
		Level 2	-	4	-	
		Level 3	-	8	-	
		Level 4	-	16	-	

(1). The value is guaranteed in design.

5 Typical circuitry

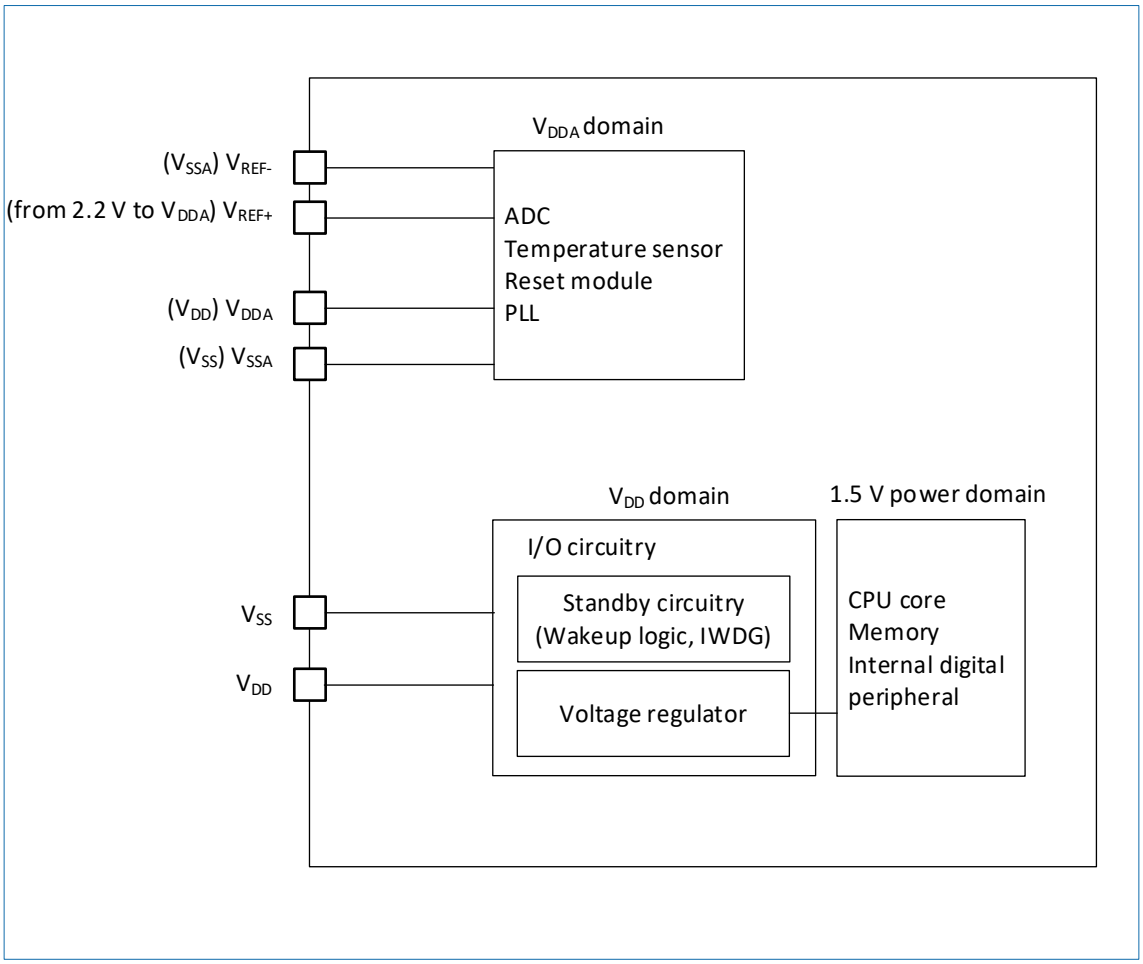

Figure 5-1 Power supply block diagram

6 Pinouts and pin descriptions

HK32ASPIN02x MCUs are delivered in LQFP48, LQFP44, LQFP32, QFN32, and TSSOP24 packages. This chapter describes the pinout and pin description of each package.

6.1 LQFP48

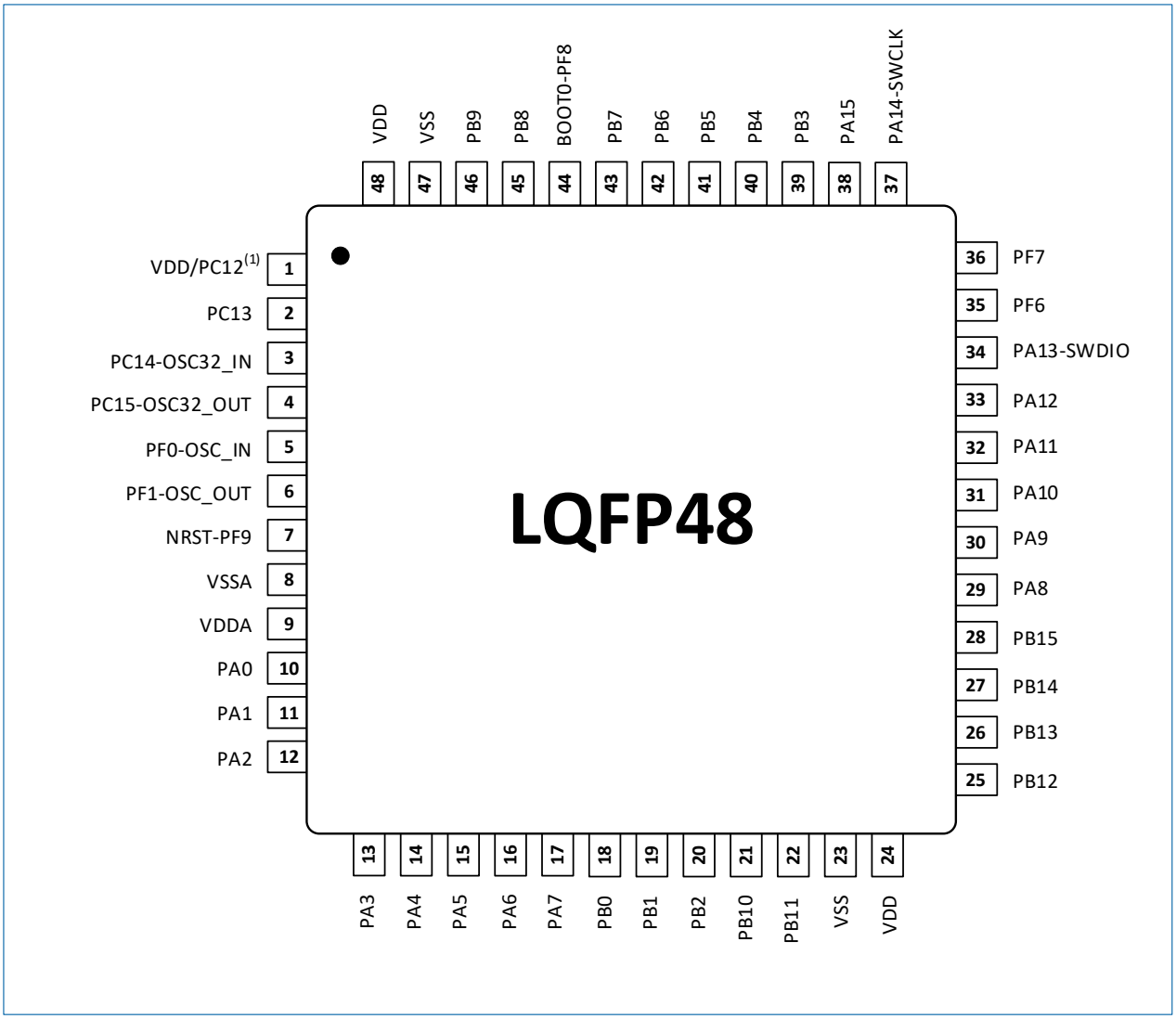

Figure 6-1 LQFP48 package pinout

Note:

(1). On HK32ASPIN021C8T7 MCUs, this pin is PC12. On the HK32ASPIN022C8T7 MCUs, this pin is VDD.

6.2 LQFP44

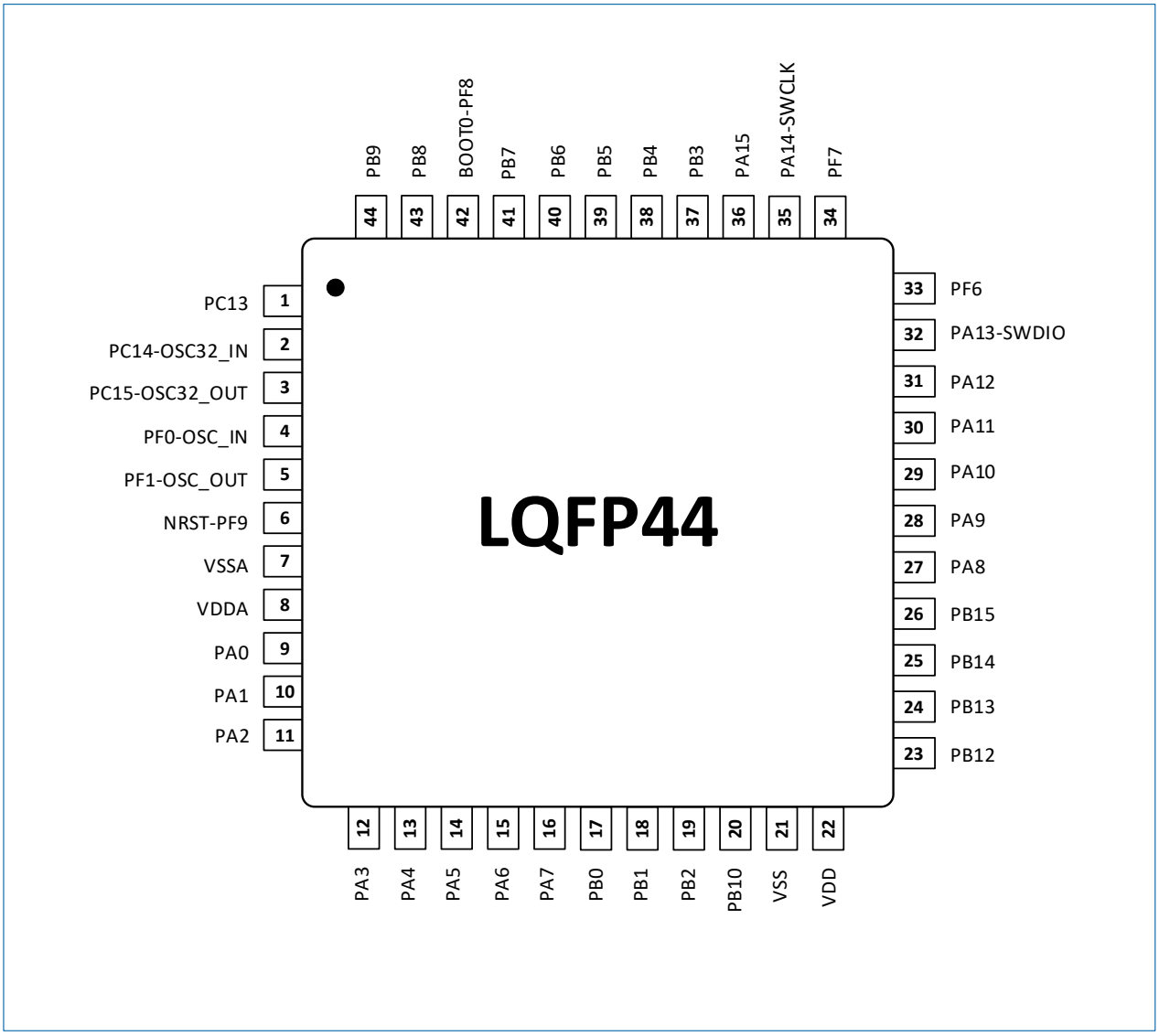

Figure 6-2 LQFP44 package pinout

6.3 LQFP32

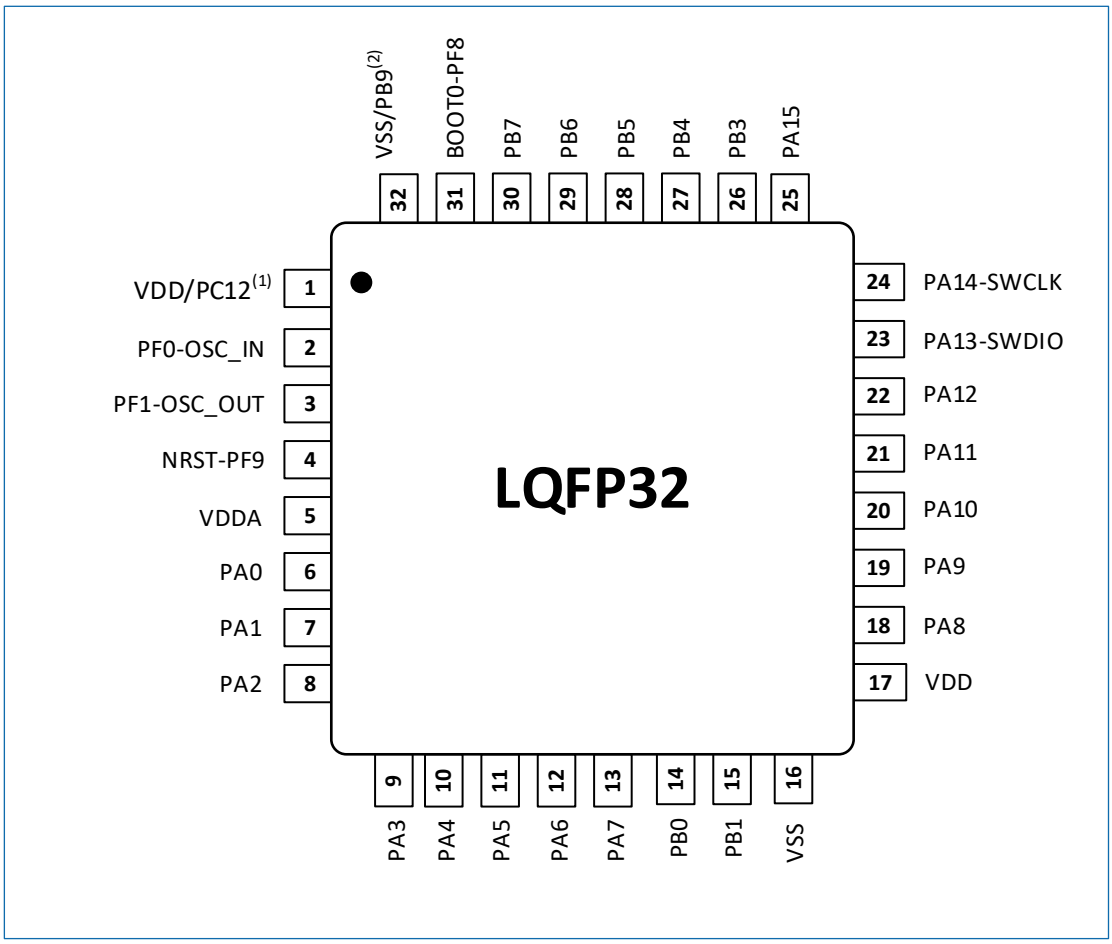

Figure 6-3 LQFP32 package pinout

Note:

(1). On HK32ASPIN020K8T7 and HK32ASPIN021K8T7 MCUs, this pin is PC12. On HK32ASPIN022K8T7 MCUs, this pin is VDD.

(2). On HK32ASPIN020K8T7 MCUs, this pin is PB9. On HK32ASPIN021K8T7 and HK32ASPIN022K8T7 MCUs, this pin is VSS.

6.4 QFN32

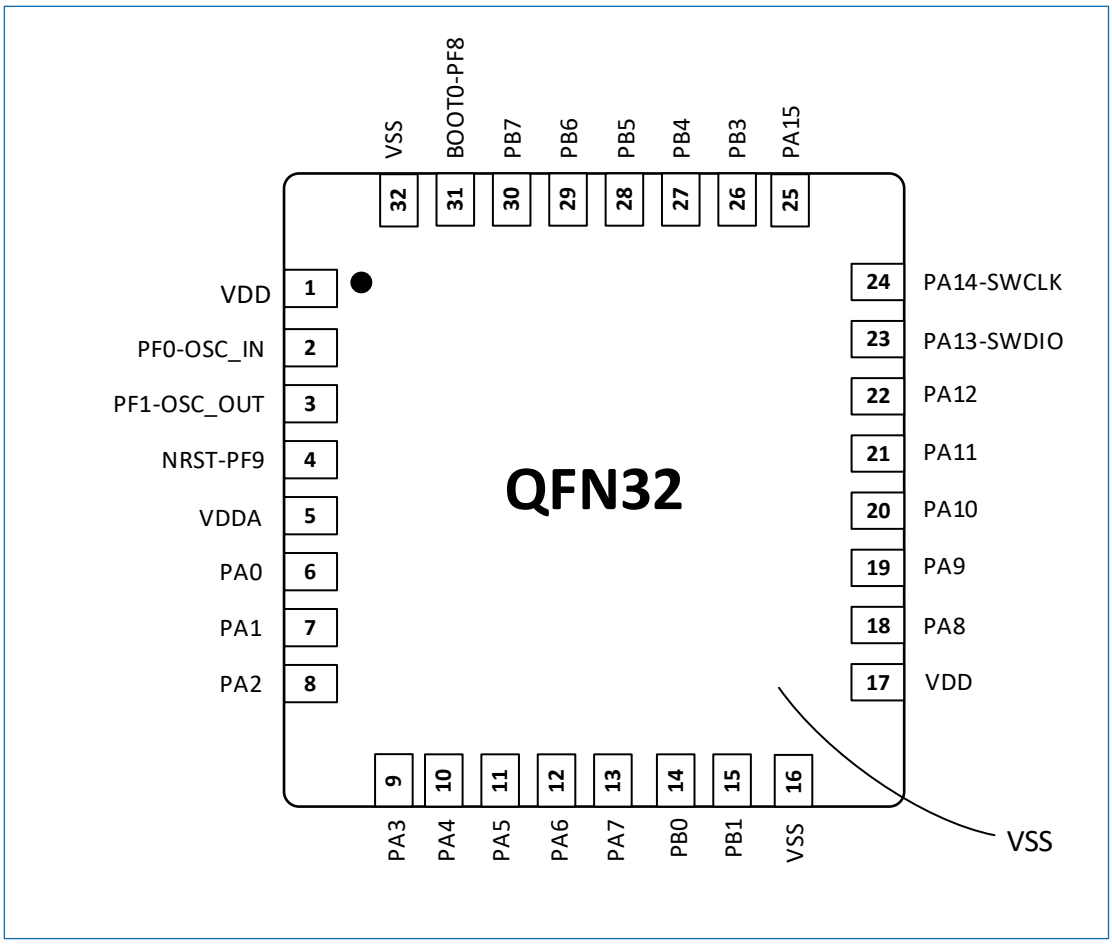

Figure 6-4 QFN32 package pinout

6.5 TSSOP24

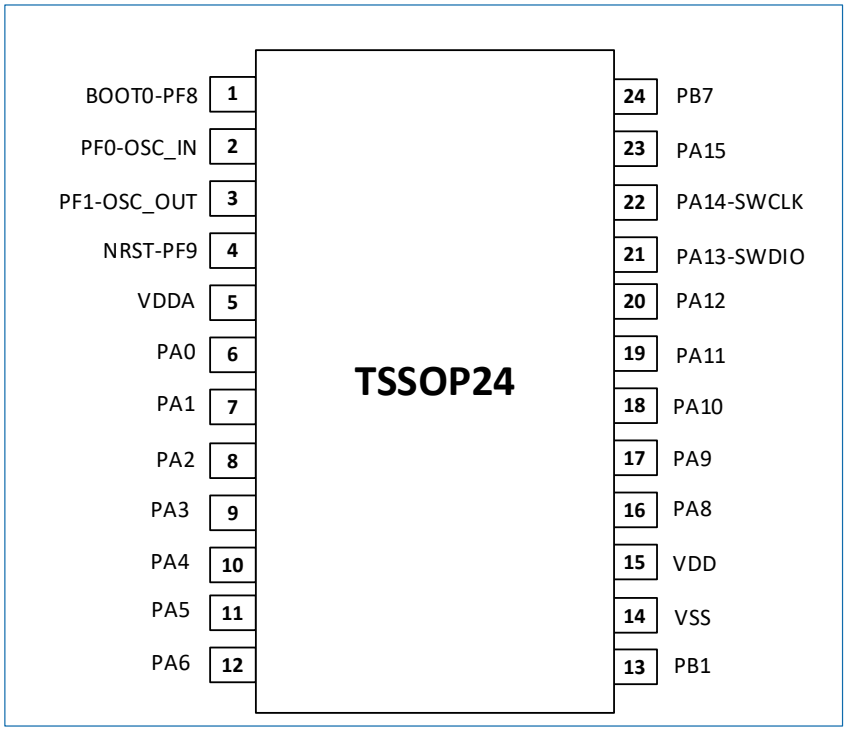

Figure 6-5 TSSOP24 package pinout

6.6 Pin descriptions

Table 6-1 Pin description of each package

LQFP48_1[4]	LQFP48_2[4]	LQFP44	LQFP32_1[4]	LQFP32_2[4]	LQFP32_3[4]	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type[1]	5 V-tolerant	Alternate Function	Additional Function
-	-	-	-	-	-	0	-	VSS	S	-	Digital ground (Pin 0 is the thermal pad on the QFN package bottom.)	
-	1	-	-	-	1	1	-	VDD	S	-	Digital power supply	
1	-	-	1	1	-	-	-	PC12	I/O	FT	TIM1_ETR UART1_TX/UART1_RX[3] UART3_TX/UART3_RX UART4_TX/UART4_RX UART5_TX/UART5_RX UART6_TX/UART6_RX TIM1_CH4	
2	2	1	-	-	-	-	-	PC13	I/O	FT	UART1_RX/UART1_TX UART2_RX/UART2_TX UART3_RX/UART3_TX UART4_RX/UART4_TX UART5_RX/UART5_TX UART6_RX/UART6_TX TIM1_BKIN	EXTIN13
3	3	2	-	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	-	TIM2_ETR TIM2_CH1 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH1	OSC32_IN LSE_CKI EXTIN14
4	4	3	-	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	-	TIM2_CH4 Trace_TX UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH1N	OSC32_OUT EXTIN15
5	5	4	2	2	2	2	2	PF0-OSC_IN (PF0)	I/O	-	I2C1_SDA/I2C1_SCL[3] TIM2_CH1 TIM2_ETR UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH2	OSC_IN HSE_CKI
6	6	5	3	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	-	I2C1_SCL/I2C1_SDA TIM2_CH2 Trace_TX UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH2N	OSC_OUT

LQFP48_1[4]	LQFP48_2[4]	LQFP44	LQFP32_1[4]	LQFP32_2[4]	LQFP32_3[4]	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type[1]	5 V-tolerant	Alternate Function	Additional Function
7	7	6	4	4	4	4	4	NRST_PF9 (NRST)	I/O	FT	TIM2_CH3 UART1_TX/UART1_RX UART2_TX/UART2_RX UART3_TX/UART3_RX UART4_TX/UART4_RX UART5_TX/UART5_RX UART6_TX/UART6_RX TIM1_BKIN	EXTIN9
8	8	7	-	-	-	-		VSSA	S		Analog ground	
9	9	8	5	5	5	5	5	VDDA	S		Analog power supply	
10	10	9	6	6	6	6	6	PA0	I/O	-	TIM2_ETR TIM2_CH1 Trace_TX UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3 CAN_RX	ADC_IN0 OAMP1_INP3 OAMP2_INP3 COMP1_INP1 CKI_4 EXTIN0
11	11	10	7	7	7	7	7	PA1	I/O	-	CM0_TXEV TIM2_CH2 TIM15_CH1N COMP1_OUT UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N CAN_TX	ADC_IN1 OAMP1_OUT COMP1_INN1 EXTIN1
12	12	11	8	8	8	8	8	PA2	I/O	-	TIM15_CH1 TIM2_CH3 TIM1_ETR COMP2_OUT UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH4 CAN_RX	ADC_IN2 OAMP1_INN0 COMP2_INN1 EXTIN2
13	13	12	9	9	9	9	9	PA3	I/O	-	TIM15_CH2 TIM2_CH4 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH1 CAN_TX	ADC_IN3 OAMP1_INP2 OAMP2_INP2 COMP2_INP1 EXTIN3
14	14	13	10	10	10	10	10	PA4	I/O	-	SPI1_NSS TIM14_CH1 UART1_TX/UART1_RX UART2_CTS	ADC_IN4 OAMP1_INP1 OAMP2_INP1 COMP1_INN2

LQFP48_1(4)	LQFP48_2(4)	LQFP44	LQFP32_1(4)	LQFP32_2(4)	LQFP32_3(4)	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
											UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH1N CAN_RX	COMP2_INN2 COMP3_INP1 CKI_1 EXTIN4
15	15	14	11	11	11	11	11	PA5	I/O	-	SPI1_SCK TIM2_ETR TIM2_CH1 UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH2 CAN_TX	ADC_IN5 OAMP2_INN0 COMP1_INN3 COMP2_INN3 COMP3_INN3 EXTIN5
16	16	15	12	12	12	12	12	PA6	I/O	-	SPI1_MISO TIM3_CH1 TIM2_CH2 TIM16_CH1 CM0_TXEV COMP1_OUT UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH2N CAN_RX	ADC_IN6 OAMP2_OUT EXTIN6
17	17	16	13	13	13	13	-	PA7	I/O	-	SPI1_MOSI TIM3_CH2 RCC_MCO TIM2_CH3 TIM14_CH1 CM0_TXEV UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH3 CAN_TX	ADC_IN7 OAMP1_INP0 OAMP2_INP0 COMP1_INP2 COMP2_INP2 COMP3_INP2 EXTIN7
18	18	17	14	14	14	14	-	PB0	I/O	-	CM0_TXEV TIM3_CH3 TIM2_CH4 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3N	ADC_IN8 COMP3_INN2 EXTIN0
19	19	18	15	15	15	15	13	PB1	I/O	-	TIM14_CH1 TIM3_CH4 Trace_TX COMP2_OUT COMP3_OUT	ADC_IN9 COMP3_INN1 EXTIN1

LQFP48_1(4)	LQFP48_2(4)	LQFP44	LQFP32_1(4)	LQFP32_2(4)	LQFP32_3(4)	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
											UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH1	
20	20	19	-	-	-	-	-	PB2	I/O	-	TIM2_ETR TIM2_CH1 I2C1_SMBA UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH1N	ADC_IN10 OAMP1_INN1 COMP1_INP3 EXTIN2
21	21	20	-	-	-	-	-	PB10	I/O	-	I2C1_SCL/I2C1_SDA TIM2_CH2 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH2 CAN_RX	ADC_IN11 OAMP2_INN1 COMP2_INP3 EXTIN10
22	22	-	-	-	-	-	-	PB11	I/O	-	CM0_TXEV I2C1_SDA/I2C1_SCL TIM2_CH3 UART1_RX/UART1_TX UART2_RX/UART2_TX UART3_RX/UART3_TX UART4_RX/UART4_TX UART5_RX/UART5_TX UART6_RX/UART6_TX TIM1_CH2N CAN_TX	ADC_IN12 COMP3_INP3 EXTIN11
23	23	21	16	16	16	16	14	VSS	S		Ground	
24	24	22	17	17	17	17	15	VDD	S		Digital power supply	
25	25	23	-	-	-	-	-	PB12	I/O	-	SPI1_NSS CM0_TXEV TIM2_CH1 TIM2_ETR TIM15_BKIN COMP1_OUT UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3 CAN_RX	ADC_IN13 EXTIN12
26	26	24	-	-	-	-	-	PB13	I/O	-	SPI1_SCK TIM2_CH2 COMP2_OUT UART1_RX/UART1_TX UART2_RTS	EXTIN13

LQFP48_1(4)	LQFP48_2(4)	LQFP44	LQFP32_1(4)	LQFP32_2(4)	LQFP32_3(4)	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
											UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N CAN_TX	
27	27	25	-	-	-	-	-	PB14	I/O	-	SPI1_MISO TIM15_CH1 TIM2_CH3 TIM1_ETR COMP3_OUT UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH4	EXTIN14
28	28	26	-	-	-	-	-	PB15	I/O	FT	SPI1_MOSI TIM15_CH2 TIM2_CH4 TIM15_CH1N UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_BKIN	EXTIN15
29	29	27	18	18	18	18	16	PA8	I/O	FT	RCC_MCO CM0_TXEV UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH1 CAN_RX	EXTIN8
30	30	28	19	19	19	19	17	PA9	I/O	FT	TIM15_BKIN TIM2_ETR TIM2_CH1 I2C1_SCL/I2C1_SDA RCC_MCO UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH1N CAN_TX	EXTIN9
31	31	29	20	20	20	20	18	PA10	I/O	FT	EXT_TRIG TIM2_CH2 I2C1_SDA/I2C1_SCL Trace_TX UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX	EXTIN10

LQFP48_1(4)	LQFP48_2(4)	LQFP44	LQFP32_1(4)	LQFP32_2(4)	LQFP32_3(4)	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
											UART5_CTS UART6_TX/UART6_RX TIM1_CH2 CAN_RX	
32	32	30	21	21	21	21	19	PA11	I/O	FT	CM0_TXEV UART1_CTS TIM2_CH3 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH2N CAN_TX	EXTIN11
33	33	31	22	22	22	22	20	PA12	I/O	FT	CM0_TXEV TIM2_CH4 UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS UART5_TX/UART5_RX UART6_CTS TIM1_CH3 CAN_RX	EXTIN12
34	34	32	23	23	23	23	21	PA13-SWDIO (SWDIO)	I/O	FT	CM0_SWD IRTIM_IROUT EXT_TRIG UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N	CKI_2 EXTIN13
35	35	33	-	-	-	-	-	PF6	I/O	FT	I2C1_SCL/I2C1_SDA TIM1_ETR UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH4	EXTIN6
36	36	34	-	-	-	-	-	PF7	I/O	FT	I2C1_SDA/I2C1_SCL EXT_TRIG UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_BKIN	EXTIN7
37	37	35	24	24	24	24	22	PA14-SWCLK (SWCLK)	I/O	FT	CM0_SWCLK Trace_TX TIM1_ETR UART1_TX/UART1_RX UART2_CTS UART3_TX/UART3_RX UART4_CTS	CKI_3 EXTIN14

LQFP48_1(4)	LQFP48_2(4)	LQFP44	LQFP32_1(4)	LQFP32_2(4)	LQFP32_3(4)	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
											UART5_TX/UART5_RX UART6_CTS TIM1_CH4	
38	38	36	25	25	25	25	23	PA15	I/O	FT	SPI1_NSS TIM2_ETR TIM2_CH1 CM0_TXEV EXT_TRIG Trace_TX UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3N CAN_TX	EXTIN15
39	39	37	26	26	26	26	-	PB3	I/O	FT	SPI1_SCK CM0_TXEV TIM2_CH2 UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_RX UART5_CTS UART6_TX/UART6_RX TIM1_CH1 CAN_RX	EXTIN3
40	40	38	27	27	27	27	-	PB4	I/O	FT	SPI1_MISO TIM3_CH1 CM0_TXEV TIM2_CH3 TIM3_ETR UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH1N CAN_TX	EXTIN4
41	41	39	28	28	28	28	-	PB5	I/O	FT	SPI1_MOSI TIM3_CH2 TIM16_BKIN I2C1_SMBA TIM2_CH4 UART1_TX/UART1_RX UART2_RX/UART2_TX UART3_TX/UART3_RX UART4_RX/UART4_TX UART5_TX/UART5_RX UART6_RX/UART6_TX TIM1_CH2 CAN_RX	EXTIN5
42	42	40	29	29	29	29	-	PB6	I/O	FT	I2C1_SCL/I2C1_SDA TIM16_CH1N UART1_TX/UART1_RX UART2_CT UART3_TX/UART3_RX UART4_CTS	EXTIN6

LQFP48_1(4)	LQFP48_2(4)	LQFP44	LQFP32_1(4)	LQFP32_2(4)	LQFP32_3(4)	QFN32	TSSOP24	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
											UART5_TX/UART5_RX UART6_CTS TIM1_CH2N CAN_TX	
43	43	41	30	30	30	30	24	PB7	I/O	FT	I2C1_SDA/I2C1_SCL TIM2_CH2 EXT_TRIG COMP3_OUT UART1_RX/UART1_TX UART2_RTS UART3_RX/UART3_TX UART4_RTS UART5_RX/UART5_TX UART6_RTS TIM1_CH3 CAN_RX	EXTIN7
44	44	42	31	31	31	31	-	BOOT0(2)-PF8 (BOOT0)	I/O	FT	TIM2_CH3 TIM3_CH3 Trace_TX UART1_CTS UART2_TX/UART2_RX UART3_CTS UART4_TX/UART4_R UART5_CTS UART6_TX/UART6_RX TIM1_CH3N	BOOT0
45	45	43	-	-	-	-	-	PB8	I/O	FT	I2C1_SCL/I2C1_SDA TIM16_CH1 UART1_RTS UART2_RX/UART2_TX UART3_RTS UART4_RX/UART4_TX UART5_RTS UART6_RX/UART6_TX TIM1_CH3 CAN_RX	EXTIN8
46	46	44	32	-	-	-	-	PB9	I/O	FT	IRTIM_IROUT I2C1_SDA/I2C1_SCL CM0_TXEV UART1_RX/UART1_TX UART2_TX/UART2_RX UART3_RX/UART3_TX UART4_TX/UART4_RX UART5_RX/UART5_TX UART6_TX/UART6_RX TIM1_CH3N CAN_TX	EXTIN9
47	47	-	-	32	32	32	-	VSS	S		Ground	
48	48	-	-	-	-	-	-	VDD	S		Digital power supply	

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). By default, the Boot0 pin has a 50 kΩ pull-down resistor.

(3). The functions of UART1/2/3/4/5/6 RX and TX pins can be exchanged by using the software, so do the functions of I2C1 SDA and SCL pins.

(4). The following table lists the relationships between different packages and part numbers:

Table 6-2 Relationships between packages and part numbers

Package	Part Number
LQFP48_1	HK32ASPIN021C8T7
LQFP48_2	HK32ASPIN022C8T7
LQFP32_1	HK32ASPIN020K8T7
LQFP32_2	HK32ASPIN021K8T7
LQFP32_3	HK32ASPIN022K8T7

Note:

- Unless otherwise specified, all I/Os are configured in input floating mode during and after resets.
- For details about alternate functions, see section "6.7 Alternate function table".

6.7 Alternate function table

Table 6-3 Alternate function table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0/AIN0		TIM2_ETR	TIM2_CH1			Trace_TX			UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH3	CAN_RX
PA1/AIN1	CM0_TXEV		TIM2_CH2			TIM15_CH1N		COMP1_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3N	CAN_TX
PA2/AIN2	TIM15_CH1		TIM2_CH3				TIM1_ETR	COMP2_OUT	UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH4	CAN_RX
PA3/AIN3	TIM15_CH2		TIM2_CH4						UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH1	CAN_TX
PA4/AIN4	SPI1_NSS				TIM14_CH1				UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH1N	CAN_RX
PA5/AIN5	SPI1_SCK	TIM2_ETR	TIM2_CH1						UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH2	CAN_TX
PA6/AIN6	SPI1_MISO	TIM3_CH1	TIM2_CH2			TIM16_CH1	CM0_TXEV	COMP1_OUT	UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH2N	CAN_RX
PA7/AIN7	SPI1_MOSI	TIM3_CH2	RCC_MCO	TIM2_CH3	TIM14_CH1		CM0_TXEV		UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH3	CAN_TX
PA8	RCC_MCO			CM0_TXEV					UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH1	CAN_RX
PA9	TIM15_BKIN	TIM2_ETR	TIM2_CH1		I2C1_SCL/I2C1_SDA	RCC_MCO			UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH1N	CAN_TX
PA10			EXT_TRIG	TIM2_CH2	I2C1_SDA/I2C1_SCL	Trace_TX			UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH2	CAN_RX
PA11	CM0_TXEV	UART1_CTS	TIM2_CH3						UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH2N	CAN_TX
PA12	CM0_TXEV	UART1_RTS	TIM2_CH4						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH3	CAN_RX
PA13_SWDIO	CM0_SWD	IRTIM_IROUT	EXT_TRIG						UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3N	
PA14_SWCLK	CM0_SWCLK					Trace_TX	TIM1_ETR		UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH4	
PA15	SPI1_NSS	TIM2_ETR	TIM2_CH1	CM0_TXEV	EXT_TRIG	Trace_TX			UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3N	CAN_TX
PB0/AIN8	CM0_TXEV	TIM3_CH3	TIM2_CH4						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH3N	
PB1/AIN9	TIM14_CH1	TIM3_CH4				Trace_TX	COMP2_OUT	COMP3_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH1	
PB2/AIN10		TIM2_ETR	TIM2_CH1	I2C1_SMBA					UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH1N	
PB3	SPI1_SCK	CM0_TXEV	TIM2_CH2						UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH1	CAN_RX
PB4	SPI1_MISO	TIM3_CH1	CM0_TXEV	TIM2_CH3	TIM3_ETR				UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH1N	CAN_TX
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	TIM2_CH4				UART1_TX/UART1_RX	UART2_RX/UART2_TX	UART3_TX/UART3_RX	UART4_RX/UART4_TX	UART5_TX/UART5_RX	UART6_RX/UART6_TX	TIM1_CH2	CAN_RX
PB6		I2C1_SCL/I2C1_SDA	TIM16_CH1N						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH2N	CAN_TX
PB7		I2C1_SDA/I2C1_SCL	TIM2_CH2		EXT_TRIG			COMP3_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3	CAN_RX
PB8		I2C1_SCL/I2	TIM16_CH1						UART1_RTS	UART2_RX/	UART3_RTS	UART4_RX/	UART5_RTS	UART6_RX/	TIM1_CH3	CAN_RX

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		C1_SDA								UART2_TX		UART4_TX		UART6_TX		
PB9	IRTIM_IROUT	I2C1_SDA/I2C1_SCL		CM0_TXEV					UART1_RX/UART1_TX	UART2_TX/UART2_RX	UART3_RX/UART3_TX	UART4_TX/UART4_RX	UART5_RX/UART5_TX	UART6_TX/UART6_RX	TIM1_CH3N	CAN_TX
PB10/AIN11		I2C1_SCL/I2C1_SDA	TIM2_CH2						UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH2	CAN_RX
PB11/AIN12	CM0_TXEV	I2C1_SDA/I2C1_SCL	TIM2_CH3						UART1_RX/UART1_TX	UART2_RX/UART2_TX	UART3_RX/UART3_TX	UART4_RX/UART4_TX	UART5_RX/UART5_TX	UART6_RX/UART6_TX	TIM1_CH2N	CAN_TX
PB12/AIN13	SPI1_NSS	CM0_TXEV	TIM2_CH1	TIM2_ETR		TIM15_BKIN		COMP1_OUT	UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH3	CAN_RX
PB13/AIN14	SPI1_SCK		TIM2_CH2					COMP2_OUT	UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH3N	CAN_TX
PB14/AIN15	SPI1_MISO	TIM15_CH1	TIM2_CH3				TIM1_ETR	COMP3_OUT	UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH4	
PB15	SPI1_MOSI	TIM15_CH2	TIM2_CH4	TIM15_CH1N					UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_BKIN	
PC12							TIM1_ETR		UART1_TX/UART1_RX	UART2_TX/UART2_RX	UART3_TX/UART3_RX	UART4_TX/UART4_RX	UART5_TX/UART5_RX	UART6_TX/UART6_RX	TIM1_CH4	
PC13									UART1_RX/UART1_TX	UART2_RX/UART2_TX	UART3_RX/UART3_TX	UART4_RX/UART4_TX	UART5_RX/UART5_TX	UART6_RX/UART6_TX	TIM1_BKIN	
PC14_OSC32_IN		TIM2_ETR	TIM2_CH1						UART1_TX/UART1_RX	UART2_CTS	UART3_TX/UART3_RX	UART4_CTS	UART5_TX/UART5_RX	UART6_CTS	TIM1_CH1	
PC15_OSC32_OUT			TIM2_CH4			Trace_TX			UART1_RX/UART1_TX	UART2_RTS	UART3_RX/UART3_TX	UART4_RTS	UART5_RX/UART5_TX	UART6_RTS	TIM1_CH1N	
PF0_OSC_IN		I2C1_SDA/I2C1_SCL	TIM2_CH1	TIM2_ETR					UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH2	
PF1_OSC_OUT		I2C1_SCL/I2C1_SDA	TIM2_CH2			Trace_TX			UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_CH2N	
PF6		I2C1_SCL/I2C1_SDA					TIM1_ETR		UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH4	
PF7		I2C1_SDA/I2C1_SCL			EXT_TRIG				UART1_RTS	UART2_RX/UART2_TX	UART3_RTS	UART4_RX/UART4_TX	UART5_RTS	UART6_RX/UART6_TX	TIM1_BKIN	
BOOT0-PF8			TIM2_CH3	TIM3_CH3		Trace_TX			UART1_CTS	UART2_TX/UART2_RX	UART3_CTS	UART4_TX/UART4_RX	UART5_CTS	UART6_TX/UART6_RX	TIM1_CH3N	
NRST_PF9			TIM2_CH3						UART1_TX/UART1_RX	UART2_TX/UART2_RX	UART3_TX/UART3_RX	UART4_TX/UART4_RX	UART5_TX/UART5_RX	UART6_TX/UART6_RX	TIM1_BKIN	

(1). The functions of UART1/2/3/4/5/6 RX and TX pins can be exchanged by using the software, so do the functions of I2C1 SDA and SCL pins.

7 Packages

7.1 Package outlines

7.1.1 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

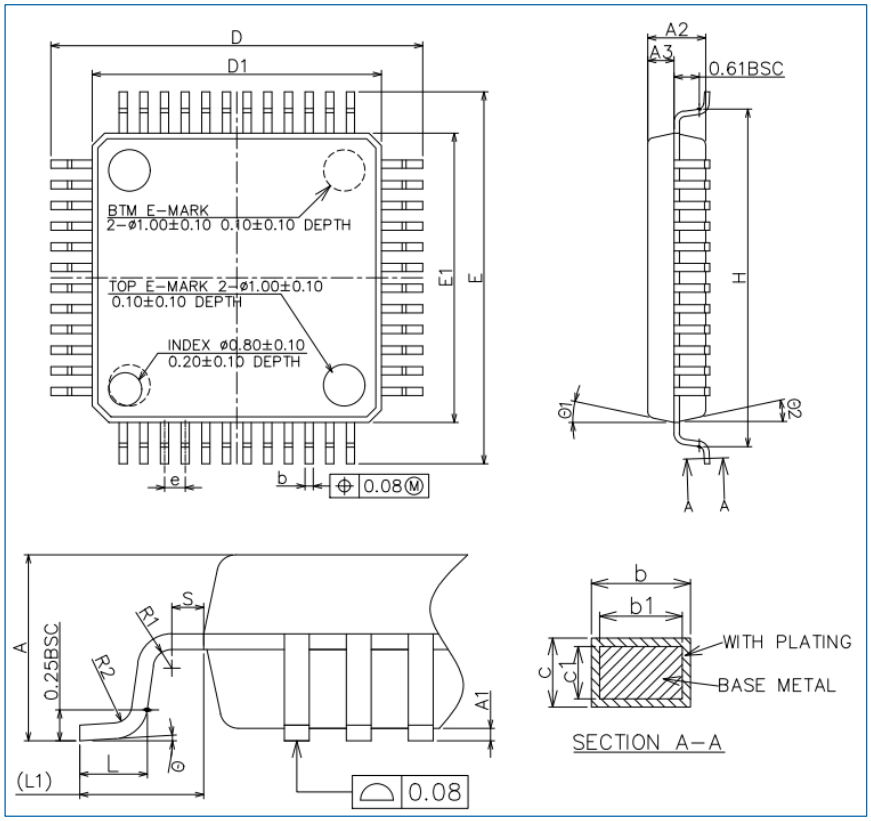

Figure 7-1 LQFP48 package outline

Table 7-1 LQFP48 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.18	-	0.27	0.0071	-	0.0106
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.40	0.50	0.60	0.0157	0.0197	0.0236
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.2	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP44

LQFP44 is a 10 mm × 10 mm, 0.8 mm pitch package.

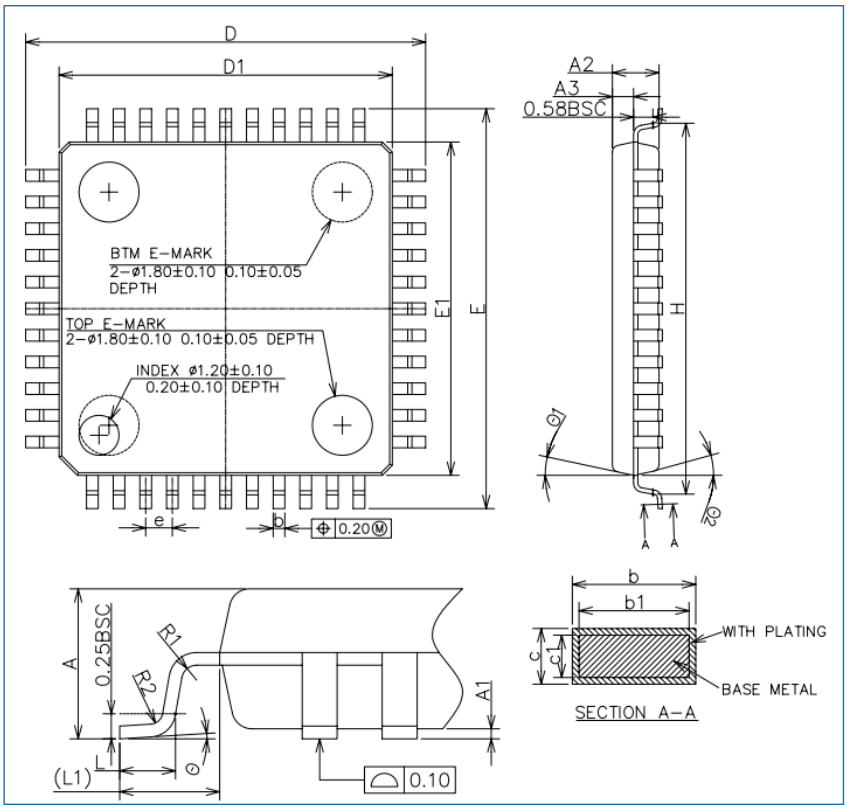

Figure 7-2 LQFP44 package outline

Table 7-2 LQFP44 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	11.95	12.00	12.05	0.4705	0.4724	0.4744
D1	9.9	10.00	10.10	0.3898	0.3937	0.3976
E	11.95	12.00	12.05	0.4705	0.4724	0.4744
E1	9.90	10.00	10.10	0.3898	0.3937	0.3976
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	11.09	11.13	11.17	0.4366	0.4382	0.4398
L	0.53	-	0.70	0.0209	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	-	0.15	-	-	0.0059	-
R2	-	0.13	-	-	0.0051	-
θ	0°	3.5°	7°	0.0079	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.3 LQFP32

LQFP32 is a 7 mm × 7 mm, 0.8 mm pitch package.

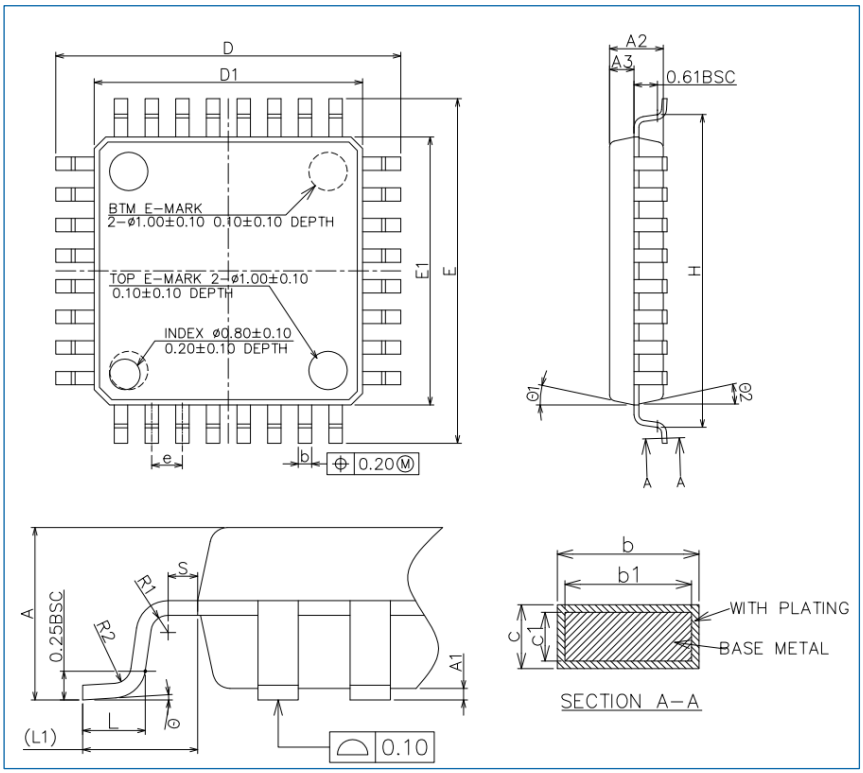

Figure 7-3 LQFP32 package outline

Table 7-3 LQFP32 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.4 QFN32

QFN32 is a 5 mm × 5 mm, 0.5 mm pitch package.

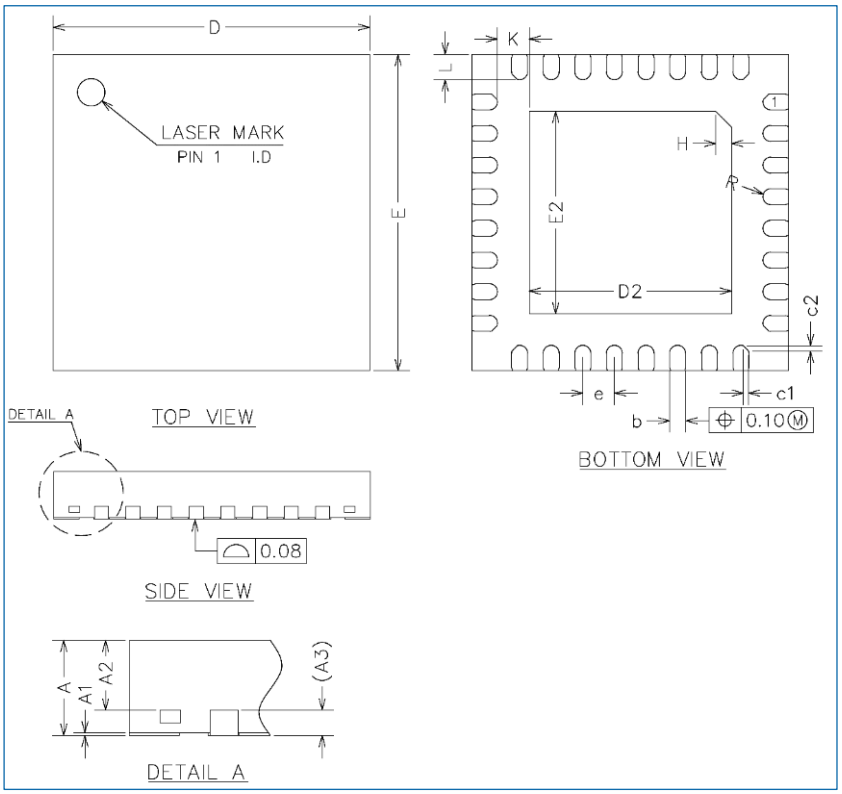

Figure 7-4 QFN32 package outline

Table 7-4 QFN32 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF(1)		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.10	3.20	3.30
E2	3.10	3.20	3.30
e	0.40	0.50	0.60
H	0.25REF		
K	0.50REF		
L	0.35	0.40	0.45
R	0.11	-	-
c1	-	0.08	-
c2	-	0.08	-

(1). REF indicates a reference value.

7.1.5 TSSOP24

TSSOP24 is a 7.8 mm × 4.4 mm, 0.65 mm pitch package.

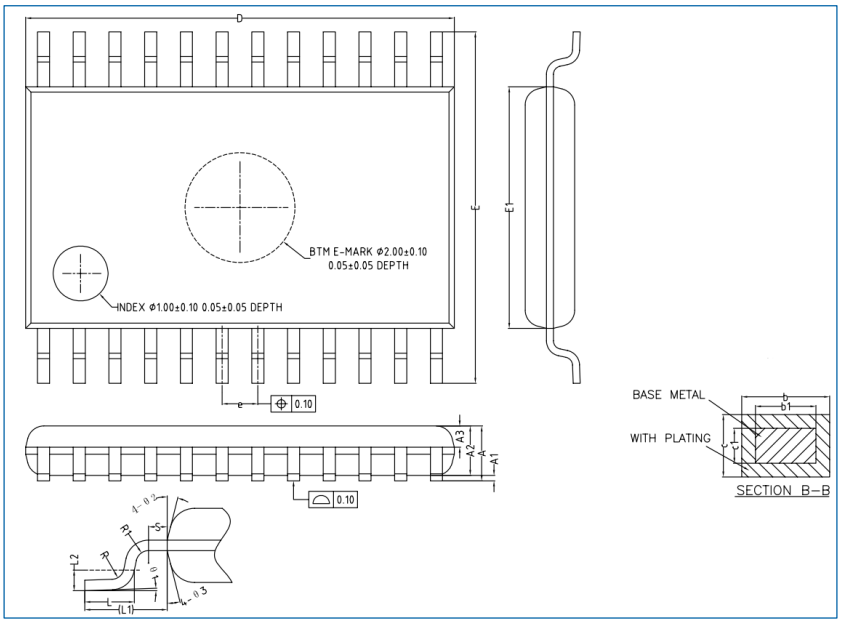

Figure 7-5 TSSOP24 package outline

Table 7-5 TSSOP24 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.0472
A1	0.05	-	0.15	0.0020	-	0.0059
A2	0.80	0.90	1.00	0.0315	0.0354	0.0394
b	0.20	-	0.29	0.0079	-	0.0114
b1	0.19	0.22	0.25	0.0075	0.0087	0.0098
c	0.10	-	0.19	0.0039	-	0.0075
c1	0.10	0.13	0.15	0.0039	0.0051	0.0059
D	7.70	7.80	7.90	0.3031	0.3071	0.3110
E	6.20	6.40	6.60	0.2441	0.2520	0.2598
E1	4.30	4.40	4.50	0.1693	0.1732	0.1772
e	0.55	0.65	0.75	0.0217	0.0256	0.0295
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
L2	-	0.25		0.0000	0.0098	0.0000
R	0.09	-	-	0.0035	-	-
R1	0.09	-	-	0.0035	-	-
S	0.20	-	-	0.0079	-	-
θ	0°	-	8°	-	-	-
θ1	12°	14°	16°	-	-	-
θ2	12°	14°	16°	-	-	-
θ3	12°	14°	16°	-	-	-

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-6 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP48 marking

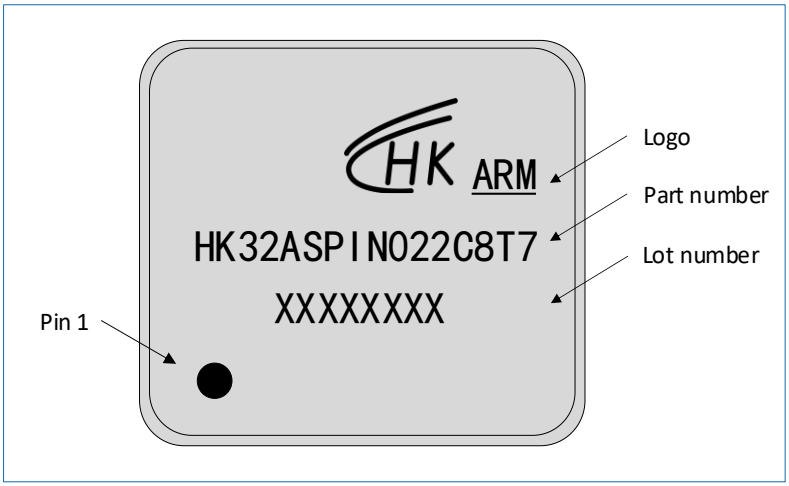

Figure 7-6 LQFP48 HK32ASPIN022C8T7 marking example

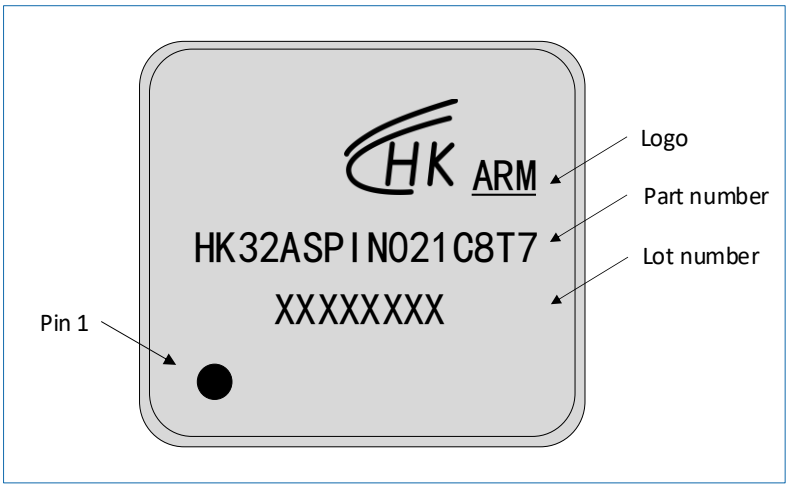

Figure 7-7 LQFP48 HK32ASPIN021C8T7 marking example

7.2.2 LQFP44 marking

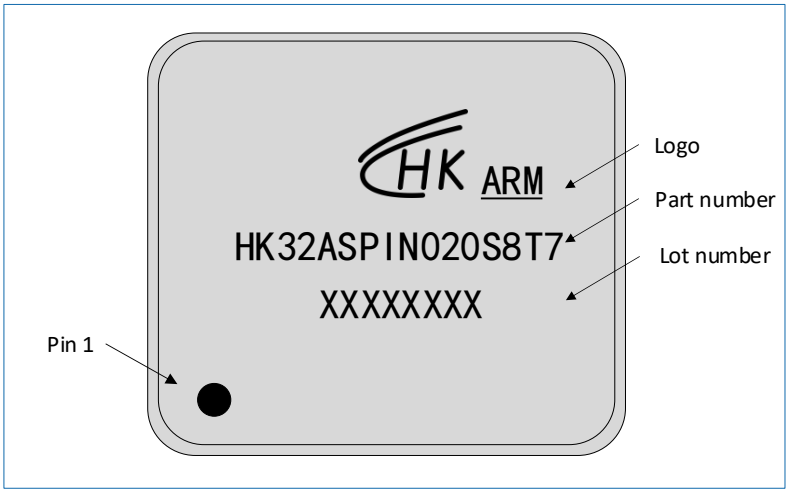

Figure 7-8 LQFP44 HK32ASPIN020S8T7 marking example

7.2.3 LQFP32 marking

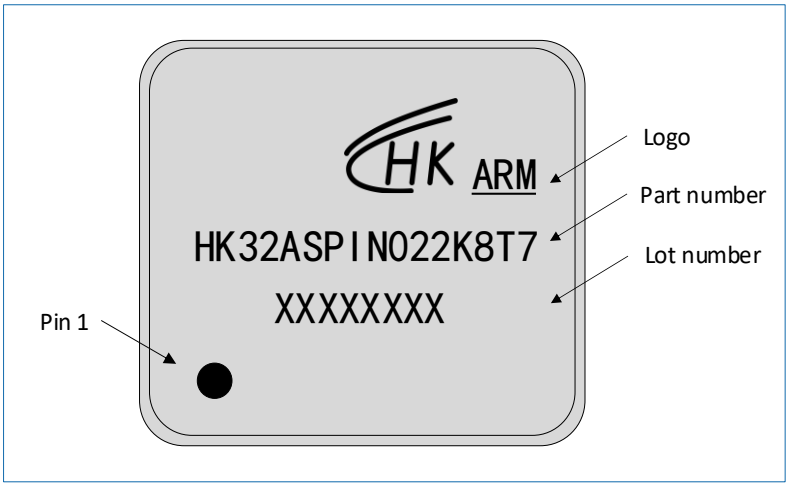

Figure 7-9 LQFP32 HK32ASPIN022K8T7 marking example

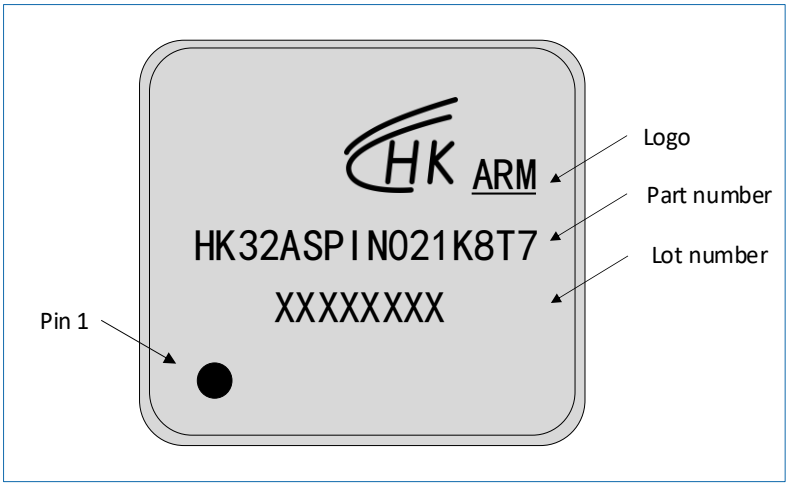

Figure 7-10 LQFP32 HK32ASPIN021K8T7 marking example

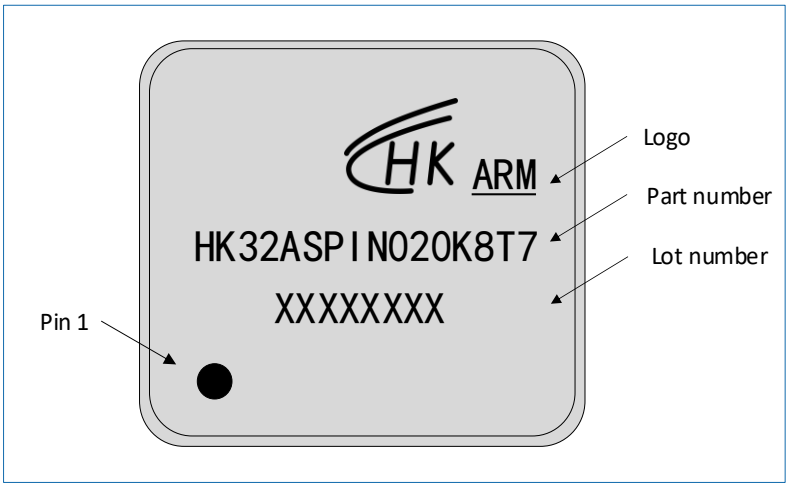

Figure 7-11 LQFP32 HK32ASPIN020K8T7 marking example

7.2.4 QFN32 marking

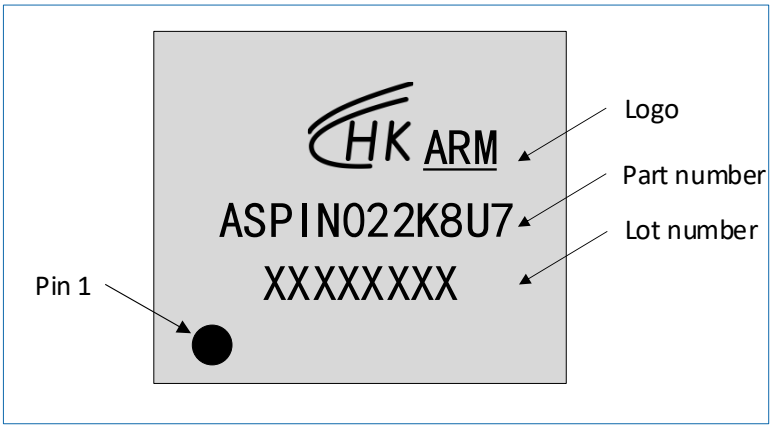

Figure 7-12 QFN32 HK32ASPIN022K8U7 marking example

7.2.5 TSSOP24 marking

Figure 7-13 TSSOP24 HK32ASPIN020E8P7 marking example

8 Ordering information

8.1 Device numbering conventions

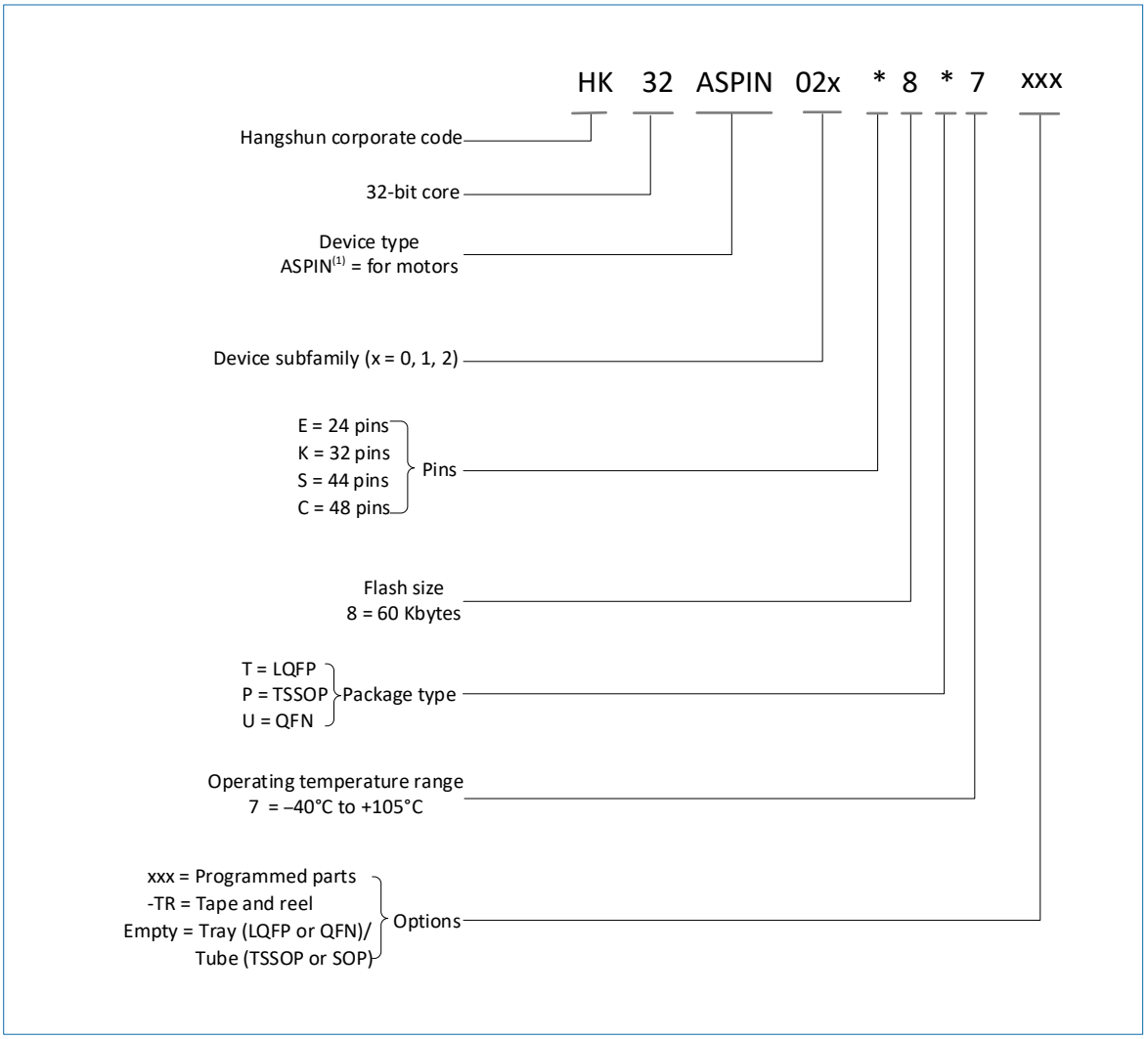

Figure 8-1 Device numbering conventions

8.2 Packaging information

Table 8-1 Packaging information

Package	Part Number	Shipping Option	Remarks
LQFP48	HK32ASPIN021C8T7	Tray	The pin descriptions of the two part numbers in the LQFP48 package are slightly different. For details, see Figure 6-1.
	HK32ASPIN021C8T7-TR	Tape and reel	
	HK32ASPIN022C8T7	Tray	
	HK32ASPIN022C8T7-TR	Tape and reel	
LQFP44	HK32ASPIN020S8T7	Tray	-
	HK32ASPIN020S8T7-TR	Tape and reel	
LQFP32	HK32ASPIN020K8T7	Tray	The pin descriptions of the three part numbers in the LQFP32 package are slightly different. For details, see Figure 6-3.
	HK32ASPIN020K8T7-TR	Tape and reel	
	HK32ASPIN021K8T7	Tray	
	HK32ASPIN021K8T7-TR	Tape and reel	
	HK32ASPIN022K8T7	Tray	
	HK32ASPIN022K8T7-TR	Tape and reel	
QFN32	HK32ASPIN022K8U7	Tray	-
	HK32ASPIN022K8U7-TR	Tape and reel	
TSSOP24	HK32ASPIN020E8P7	Tube	-
	HK32ASPIN020E8P7-TR	Tape and reel	

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EXTI	Extended Interrupt/Event Controller
GPIO	General-purpose Input/Output
HSE	High-speed External (clock signal)
I2C	Inter-integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PGA	Programmable Gain Amplifier
PLL	Phase-locked Loop
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information


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Shenzhen Hangshun Chip Technology R&D Co., Ltd.

TEL: +86-755-83247667

Website: www.hsxp-hk.com