



# HK32ASAFE010xB Datasheet

Version: 1.0

Release Date: 2023-06-09

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# Preface

## Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32ASAFE010xB series microcontrollers (MCUs). This document helps you quickly understand the characteristics and functions of HK32ASAFE010xB.

## Audience

This document is intended for:

- HK32ASAFE010xB developers
- HK32ASAFE010xB testers
- HK32ASAFE010xB users

## Release Notes

This document is applicable to HK32ASAFE010xB series MCUs.

## Revision History

| Version | Date       | Description          |
|---------|------------|----------------------|
| 1.0     | 2023/06/09 | The initial release. |

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## 1 Introduction

This document is the datasheet for HK32ASAFE010xB series MCUs. HK32ASAFE010xB is a family of MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun) for a wide range of purposes. This MCU family includes:

- HK32ASAFE010FBP6
- HK32ASAFE010GBU6
- HK32ASAFE010KBU6
- HK32ASAFE010KBT6
- HK32ASAFE010CBT6
- HK32ASAFE010RBT6

For more details of HK32ASAFE010xB, see *HK32ASAFE010xB User Manual*.

## 2 Product overview

HK32ASAFE010xB adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 96 MHz and has 124 Kbytes of Flash and 10 Kbytes of SRAM. You can configure the Flash controller register to remap interrupt vectors in the main Flash.

HK32ASAFE010xB supports conventional Flash readout protection (RDP) Level 0, Level 1, and Level 2 and provides the patented Flash code encryption function of Hangshun.

To meet the security requirements of various applications, HK32ASAFE010xB provides the cyclic redundancy check (CRC), Advanced Encryption Standard 128 (AES128), hash, and True Random Number Generator (TRNG) hardware units. These hardware units can be used to encrypt and decrypt Flash data.

HK32ASAFE010xB incorporates a wide selection of communication interfaces:

- 2 × USARTs and 1 × LPUART (up to 12 Mbit/s)

The USARTs support synchronous and asynchronous full-duplex or half-duplex communication, multiprocessor communication, LIN protocol, Smart Card protocol, and IrDA SIR ENDEC. The RX and TX pins can be exchanged by using the software. The USARTs and LPUART can wake up the MCU from Stop mode when receiving data.

- Up to 2 × high-speed SPIs/I2Ss (up to 18 Mbit/s)

The SPIs/I2Ss support the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, automatic CRC, and I2S protocol.

- Up to 2 × high-speed I2Cs (up to 1 Mbit/s)

The I2Cs support the 1 Mbit/s, 400 Kbit/s, and 100 Kbit/s transmission rates, master/slave mode, multimaster mode, 7-bit/10-bit addressing, and SMBus protocol. The I2Cs can wake up the MCU from Stop mode when receiving data.

HK32ASAFE010xB embeds a 16-bit advanced PWM timer (four PWM output channels in total, three of which have complementary PWM outputs with programmable inserted dead-times), a 32-bit and five 16-bit general-purpose PWM timers (up to four PWM output channels), a basic timer, and a 16-bit low-power timer.

HK32ASAFE010xB also incorporates the analog circuitry: a 12-bit ADC (16 analog signal input channels in total, differential pair input supported; sampling rate of up to 1 MSPS), a power-on reset (POR)/power-down reset (PDR) circuit, an internal reference voltage obtained from internal ADC sampling, and a  $1/2 V_{BAT}$  voltage divider circuit.

HK32ASAFE010xB integrates the division and square root hardware unit, which provides higher performance than software and faster responses to external interrupts.

Except for the power pin, ground pin, and NRST pin, all the other pins of HK32ASAFE010xB can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32ASAFE010xB operates in the  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  temperature range, from a 1.8 V to 3.6 V power supply. It meets the environmental requirements of most applications.

With its extensive range of peripherals, HK32ASAFE010xB is suitable for various applications:

- Programmable controllers, printers, and scanners
- Motor-driven devices and speed control
- Internet of Things (IoT) terminals, such as water meters, electricity meters, and gas meters
- Drone control, gimbal control
- Toys
- Household appliances
- Intelligent robots

- Smartwatches and fitness trackers
- Electronic toll collection (ETC)

## 2.1 Features

- CPU core
  - ARM® Cortex® -M0
  - Maximum frequency: 96 MHz
  - 24-bit SysTick timer
  - Supports the remapping of interrupt vectors (by configuring the Flash controller register)
- Operating voltage range
  - Single power domain (main power supply  $V_{DD}$ ): 1.8 V to 3.6 V
  - Backup power supply  $V_{BAT}$ : 1.8 V to 3.6 V
- Operating temperature range:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- Typical operating current
  - Run mode: 6.1 mA@96 MHz; 1.6 mA@8 MHz
  - Sleep mode: 4.7 mA@96 MHz
  - Stop mode:
    - LDO full-speed: 0.7 mA@3.3 V
    - LDO low-power: 60  $\mu\text{A}$ @3.3 V
  - Standby mode: 1.6  $\mu\text{A}$ @3.3 V
  - Shutdown mode: 0.4  $\mu\text{A}$ @3.3 V
- Memory
  - Up to 124 Kbytes of Flash
    - No wait states to access Flash when the CPU frequency is 24 MHz or lower
    - Separate read and write protection for Flash data
    - Encryption for instructions and data stored in the Flash, preventing the damage caused by physical attacks
  - 10-Kbyte SRAM
- Data security
  - CRC hardware implementation unit
  - Multiple encryption modules including AES and hash modules
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz, typical value: 8 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): configurable to 8 MHz/14 MHz/56 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL clock
  - Chip pin input clock (EXTCLK)
- Reset
  - External pin reset
  - POR/PDR



- Software reset
- IWDG and WWDG reset
- Low-power mode reset
- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detecting voltage
  - Rising edge and falling edge detection configurable
- GPIO
  - Up to 55 GPIO pins
  - Each GPIO pin can be used as an external interrupt input
  - Provide the drive current of up to 40 mA
- Data communication interface
  - 2 × USARTs: support synchronous transmission corresponding to SPI master mode and support modem operations. Provide the ISO7816 interface, LIN, IrDA capability, automatic baud rate detection, and the wakeup feature.
  - 1 × LPUART: supports asynchronous serial communication, single-wire half-duplex communication, modem operations (CTS/RTS), and multiprocessor communication in the lowest-power mode.
  - Up to 2 × high-speed SPIs: support 4-bit to 16-bit programmable data frames, I2S multiplexed.
  - Up to 2 × I2Cs: can operate in fast mode plus (1 Mbit/s) and support SMBus and PMBus. Can wake up the MCU from Stop mode when receiving data.
  - 1 × CAN: compliant with Specification 2.0A and 2.0B (active).
- Timer and PWM generator
  - 1 × 16-bit advanced timer: with the break function and four PWM outputs in total, three of which have complementary PWM outputs with programmable inserted dead-times
  - 1 × 32-bit and 5 × 16-bit general-purpose timers: TIM2/TIM3/TIM14/TIM15/TIM16/TIM17
  - 1 × 16-bit basic timer: TIM6
  - 1 × low-power timer: LPTIM
- On-chip analog circuitry
  - 1 × 12-bit SAR ADC (up to 16 analog input channels)
  - Maximum frequency: 1 MSPS
  - Supports automatic continuous conversion and scan conversion
- DMA controller (7-channel)
  - Can be triggered by peripherals such as the timer, ADC, SPI, I2C, USART, AES, and hash
- Temperature sensor
  - The analog output is connected to an independent ADC channel.
- CPU trace and debug
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Division and square root (DVSQ) calculation unit
  - Supports 32-bit fixed point division, with the quotient and remainder calculated
  - Supports 32-bit fixed point high-precision root calculation

- RTC
  - Supports the alarm function
  - Periodically wakes up the MCU from Stop or Standby mode
- 96-bit unique ID (UID) of each MCU
- Reliability
  - Passed HBM6000V/CDM2000V/MM200V/LU200mA level tests.

## 2.2 Device overview

Table 2-1 HK32ASAFE010xB series features

| Feature                  |                       | HK32ASAFE<br>010FBP6  | HK32ASAFE<br>010GBU6 | HK32ASAFE<br>010KBU6 | HK32ASAFE<br>010KBT6 | HK32ASAFE<br>010CBT6 | HK32ASAFE<br>010RBT6 |
|--------------------------|-----------------------|---|----------------------|----------------------|----------------------|----------------------|----------------------|
| Operating voltage        | Main power supply     | 1.8 V to 3.6 V  |                      |                      |                      |                      |                      |
|                          | Backup power supply   | 1.8 V to 3.6 V  |                      |                      |                      |                      |                      |
| Operating temperature    |                       | -40°C to +105°C   |                      |                      |                      |                      |                      |
| Memory                   | Flash (Kbyte)         | 124   |                      |                      |                      |                      |                      |
|                          | SRAM                  | 10 Kbytes   |                      |                      |                      |                      |                      |
| CPU                      | Core                  | Cortex®-M0  |                      |                      |                      |                      |                      |
|                          | Frequency             | 96 MHz  |                      |                      |                      |                      |                      |
| DMA                      |                       | 7-channel (handles the ADC/SPI/I2C/USART/timer/AES/hash requests) |                      |                      |                      |                      |                      |
| DVSQ                     |                       | 1   |                      |                      |                      |                      |                      |
| Clock                    | LSI                   | 40 kHz  |                      |                      |                      |                      |                      |
|                          | HSI                   | Configurable to 8 MHz/14 MHz/56 MHz (default: 56 MHz)             |                      |                      |                      |                      |                      |
|                          | PLL clock             | Supported   |                      |                      |                      |                      |                      |
|                          | HSE                   | 8 MHz – 32 MHz  |                      |                      |                      |                      |                      |
|                          | LSE                   | 32.768 kHz  |                      |                      |                      |                      |                      |
| Timer                    | Advanced timer        | TIM1 (16-bit)   |                      |                      |                      |                      |                      |
|                          | General-purpose timer | 32-bit: TIM2<br>16-bit: TIM3/TIM14/TIM15/TIM16/TIM17              |                      |                      |                      |                      |                      |
|                          | Basic timer           | TIM6 (16-bit)   |                      |                      |                      |                      |                      |
|                          | Low-power timer       | LPTIM (16-bit)  |                      |                      |                      |                      |                      |
|                          | SysTick timer         | 1   |                      |                      |                      |                      |                      |
|                          | RTC                   | 1   |                      |                      |                      |                      |                      |
|                          | IWDG                  | 1   |                      |                      |                      |                      |                      |
|                          | WWDG                  | 1   |                      |                      |                      |                      |                      |
| Peripheral communication | USART                 | 2   |                      |                      |                      |                      |                      |
|                          | LPUART                | 1   |                      |                      |                      |                      |                      |
|                          | I2C                   | 1   | 1                    | 2                    | 2                    | 2                    | 2                    |
|                          | SPI/I2S               | 1   | 1                    | 2                    | 2                    | 2                    | 2                    |
|                          | CAN (2.0A/2.0B)       | 1   |                      |                      |                      |                      |                      |
| ADC                      | Channels              | 9   | 10                   | 10                   | 10                   | 10                   | 16                   |

| Feature        |                     | HK32ASAFE<br>010FBP6             | HK32ASAFE<br>010GBU6 | HK32ASAFE<br>010KBU6 | HK32ASAFE<br>010KBT6 | HK32ASAFE<br>010CBT6 | HK32ASAFE<br>010RBT6 |
|----------------|---------------------|----------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
|                | Reference selection | External reference voltage input |                      |                      |                      |                      |                      |
|                | ADC sampling rate   | 1 MSPS                           |                      |                      |                      |                      |                      |
|                | ADC accuracy        | 12-bit                           |                      |                      |                      |                      |                      |
| Info. security | CRC                 | 1                                |                      |                      |                      |                      |                      |
|                | 96-bit UID          | 1                                |                      |                      |                      |                      |                      |
|                | Encryption module   | AES128                           |                      |                      |                      |                      |                      |
|                | Hash                | SHA256                           |                      |                      |                      |                      |                      |
|                | TRNG                | 1                                |                      |                      |                      |                      |                      |
| PVD            | 1                   |                                  |                      |                      |                      |                      |                      |
| GPIO           | 15                  | 23                               | 27                   | 25                   | 39                   | 55                   |                      |
| Package        | TSSOP20             | QFN28                            | QFN32                | LQFP32               | LQFP48               | LQFP64               |                      |

### 3 Function description

#### 3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor that provides an MCU platform featuring low cost and low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M0 core, the HK32ASAFE010xB family is compatible with ARM tools and software.

The block diagram of HK32ASAFE010RBT6 is as follows:

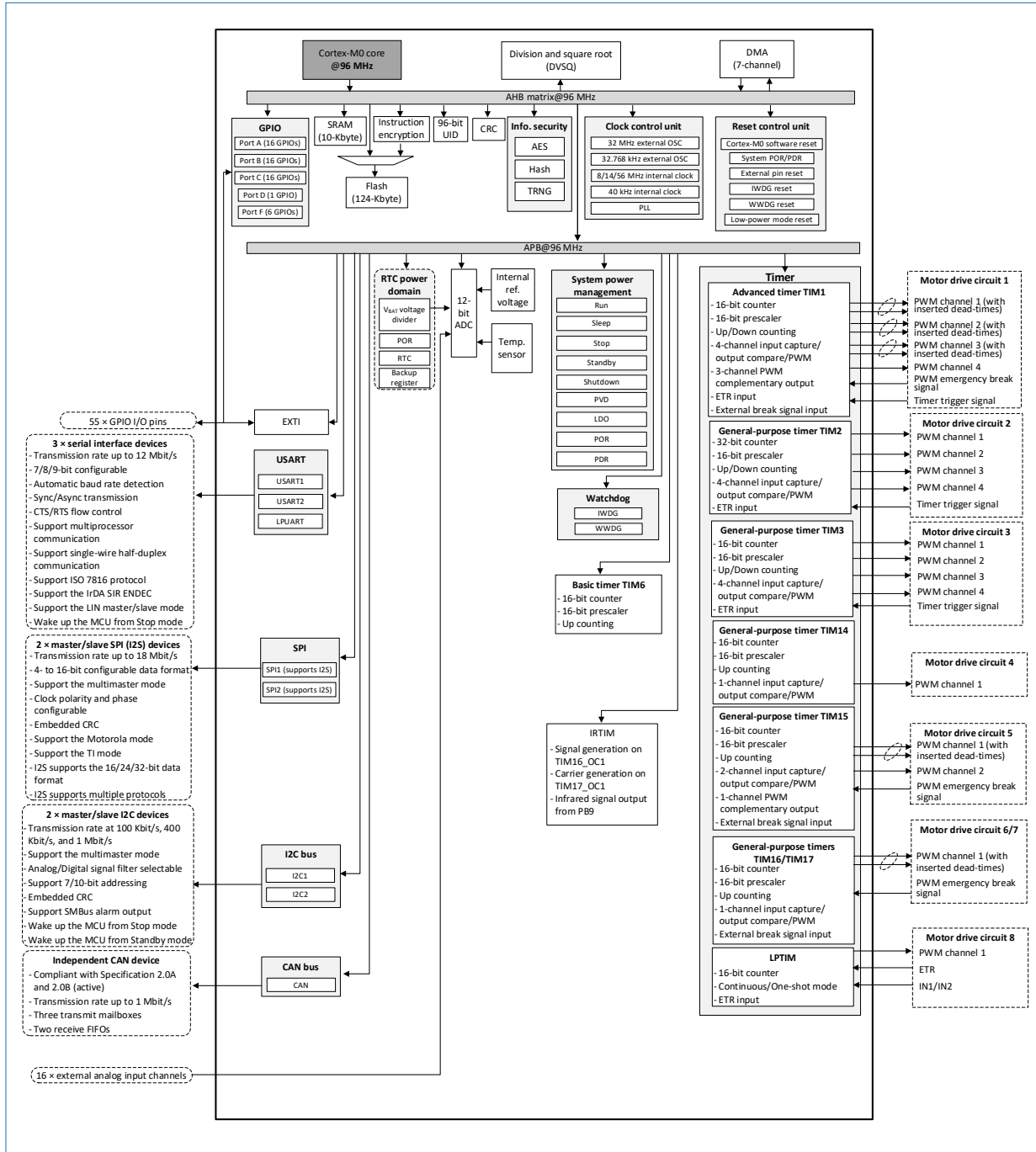


Figure 3-1 HK32ASAFE010RBT6 block diagram

## 3.2 Memory mapping

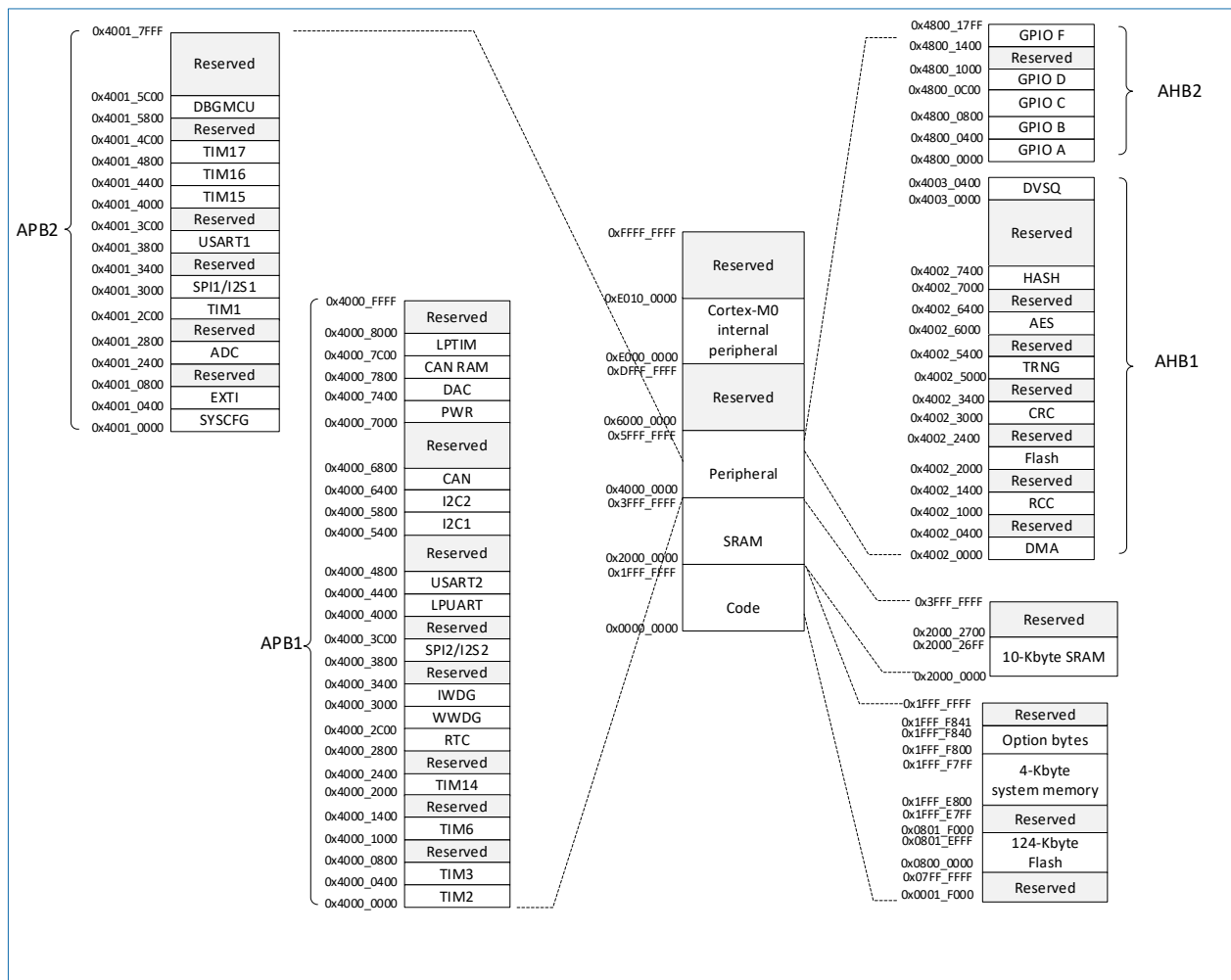


Figure 3-2 HK32ASAFE010xB memory mapping

## 3.3 Flash

HK32ASAFE010xB integrates a Flash memory of 124 Kbytes to store programs and data.

## 3.4 SRAM

HK32ASAFE010xB integrates a 10-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait state, meeting the requirements of most applications.

## 3.5 Resets

### 3.5.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC\_CSR and the registers in the backup domain. You can identify the reset source by checking reset status flags in the RCC\_CSR register.

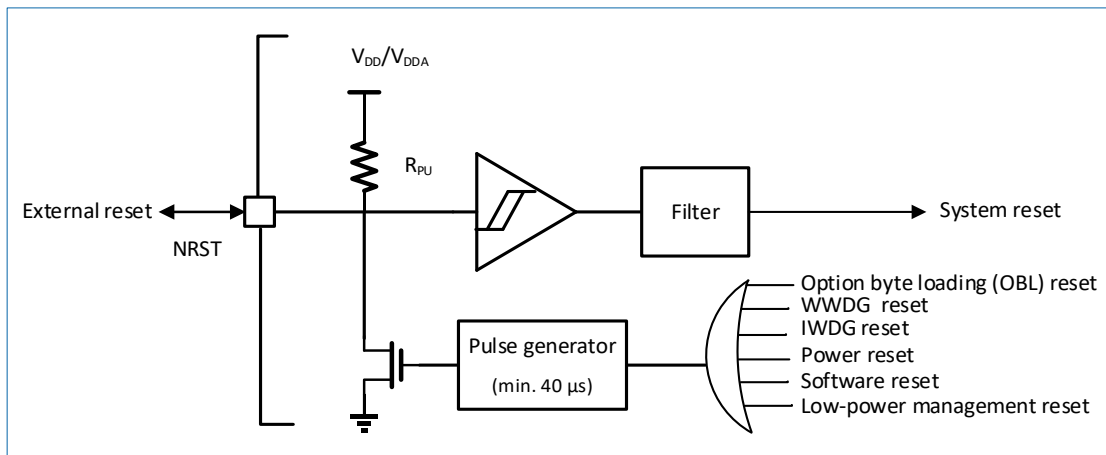


Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex<sup>®</sup>-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset
- Option byte loading (OBL) reset

The reset sources finally act on the NRST pin. The NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004.

The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 μs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

### 3.5.2 Power reset

A power reset is generated when any of the following events occurs:

- POR/PDR
- Exit from Standby mode

The power reset resets all registers, except for the registers in the backup domain.

HK32ASAFE010xB MCUs contain the POR/PDR circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the 1.8 V threshold. When  $V_{DD}$  is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

### 3.6 Clocks and clock tree

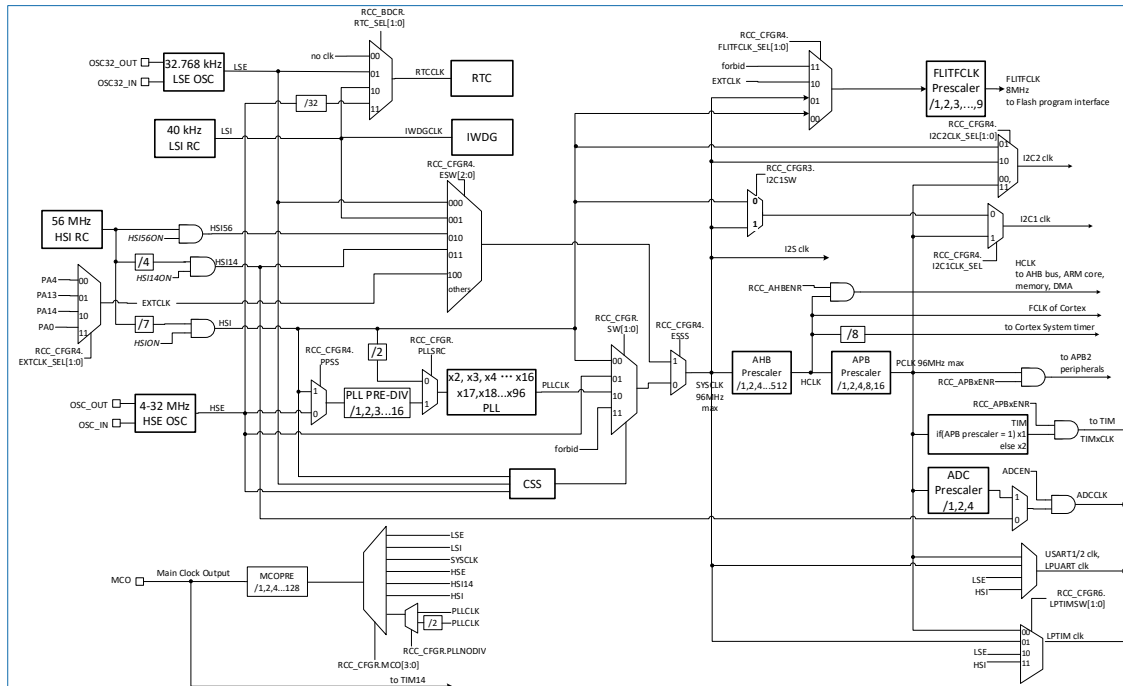


Figure 3-4 Clock tree of HK32ASAFE010xB

As Figure 3-4 shows, HSI and HSI14 are generated by the same internal oscillator operating at 56 MHz. Therefore, when HSI or HSI14 is used, disabling the other clock cannot reduce power consumption. HSI/HSE can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI together with PLL to configure different system clock frequencies.

HK32ASAFE010xB MCUs use SYSClk as the CPU clock when they start. The 56 MHz clock output by the internal oscillator, or the prescaled HSI or HSI14 can be used as the SYSClk.

HK32ASAFE010xB provides more clock sources for the system clock and offers convenient, flexible, and diverse operating modes to customers. The following clocks can act as the system clock:

- HSI56 oscillator
- HSI14 oscillator
- HSI oscillator
- LSI oscillator
- LSE oscillator
- HSE oscillator
- EXTCLK external clock
- PLL

PCLK can act as the I2C clock source.

### 3.7 Power supply scheme

- $V_{DD} = 1.8\text{ V to }3.6\text{ V}$ . The  $V_{DD}$  pin supplies power to I/O pins and internal low dropout regulators (LDOs).
- $V_{DDA} = 1.8\text{ V to }3.6\text{ V}$ . The  $V_{DDA}$  pin supplies power to the analog circuitry, such as the ADC and temperature sensor.
- $V_{BAT} = 1.8\text{ V to }3.6\text{ V}$ . When  $V_{DD}$  is powered off,  $V_{BAT}$  supplies power to the RTC, external 32.768 kHz oscillator, and backup registers.

### 3.8 Boot modes

The Boot0 pin and its configuration bit are used to select the system boot mode:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. You can reprogram the Flash by using the bootloader program via the USART1 PA9/PA10 pin or USART2 PA14/PA15 pin.

### 3.9 PVD

HK32ASAFE010xB integrates a programmable voltage detector (PVD). The PVD monitors  $V_{DD}$  and compares it with the  $V_{PVD}$  threshold. When  $V_{DD}$  is below or over the  $V_{PVD}$  threshold, an interrupt is generated, and the interrupt program may send a warning message or set the MCU in the safe state. The PVD is enabled by setting the register.

### 3.10 Low-power modes

HK32ASAFE010xB supports multiple power consumption modes.

- Run mode  
In Run mode, the CPU runs at full speed.
- Sleep mode  
In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.
- Stop mode  
In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the HSI RC oscillator, and the HSE crystal oscillator are disabled. MCUs can be woken up from Stop mode by any EXTI line. The EXTI line source can be any of the 16 external I/O pins, a PVD output, or an RTC alarm signal.
- Standby mode  
In Standby mode, the MCU achieves the lowest power consumption. The internal LDO is off, so the entire 1.2 V domain is powered off. The PLL, HSI RC oscillator, and HSE crystal oscillator are disabled. The SRAM and register content is lost while the register content in the backup domain is retained. The Standby circuitry works as normal.  
MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.
- Shutdown mode  
In Shutdown mode, the MCU achieves extremely low power consumption as in Standby mode. All internal LDO power supplies (including the power supply of the backup domain) and all clock sources are off, except for the shutdown wakeup circuitry. MCUs exit from Shutdown mode when an external reset on the NRST pin, an IWDG reset, or a rising edge on the WKUP pin occurs. The backup domain is off, so the MCU cannot be woken up by an RTC alarm.

Table 3-1 Operating modes and power consumption

| Operating Mode | Power Consumption                                 | Wakeup Time                 |
|----------------|---|-----------------------------|
| Run mode       | Power consumption 1.6 mA/8 MHz@3.3 V              | -                           |
| Sleep mode     | Power consumption 1.3 mA/8 MHz@3.3 V              | 4.7 $\mu$ s                 |
| Stop mode      | Static power consumption 60 $\mu$ A@3.3 V         | 132 $\mu$ s (fastest speed) |
| Standby mode   | Static power consumption 1.6 $\mu$ A@3.3 V        | 152 $\mu$ s                 |
| Shutdown mode  | Lowest static power consumption 0.4 $\mu$ A@3.3 V | 364 $\mu$ s                 |

The conditions for entering and exiting low-power modes are listed in the following table:



Table 3-2 Conditions for entering and exiting low-power modes

| Operating Mode | Entry   | Exit   |
|----------------|---|--|
| Sleep          | 1. Set PWR_CR:LPDS = 0.<br>2. The software executes WFI/WFE instructions.   | Any IRQ interrupt/event, including the SysTick timer.        |
| Stop           | 1. Set PWR_CR:PDDS = 0.<br>2. Set the SLEEPDEEP bit in the Cortex-M0 system control register. The software executes WFI/WFE instructions.   | Any EXTI line.   |
| Standby        | 1. Set PWR_CR:LPDS = 0.<br>2. Set PWR_CR:PDDS = 1.<br>3. Set the SLEEPDEEP bit in the Cortex-M0 system control register. The software executes WFI/WFE instructions.                              | Three polarity-configurable external pins, or the RTC alarm. |
| Shutdown       | 1. Set PWR_CR:LPDS = 0.<br>2. Set PWR_CR:PDDS = 1.<br>3. Set PWR_CSR2:SHDS = 1.<br>4. Set the SLEEPDEEP bit in the Cortex-M0 system control register. The software executes WFI/WFE instructions. | Three polarity-configurable external pins.                   |

### 3.11 NVIC

HK32ASAFE010xB incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 32 maskable interrupt channels (including 16 Cortex<sup>®</sup>-M0 interrupt lines) and four interrupt priorities.

- The closely coupled NVIC ensures low latency during interrupt processing.
- The interrupt vector entry address is directly passed to the core.
- Provides the closely coupled NVIC interface.
- Supports the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- Saves the processor state automatically.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

Table 3-3 NVIC

| Position | Priority | Name         | Description | Address  |
|----------|----------|--------------|-------------|--|
| -        | -        | -            | Reserved    | 0x0000_0000  |
| -        | -3       | Fixed        | Reset       | 0x0000_0004  |
| -        | -2       | Fixed        | NMI         | Non-maskable interrupt. The RCC clock security system (CSS) is connected to the NMI vector.<br>0x0000_0008 |
| -        | -1       | Fixed        | HardFault   | All classes of faults<br>0x0000_000C   |
| -        | 3        | Configurable | SVCall      | System service call via SWI instruction<br>0x0000_002C   |
| -        | 5        | Configurable | PendSV      | Pendable request for system service<br>0x0000_0038   |
| -        | 6        | Configurable | SysTick     | SysTick timer<br>0x0000_003C   |
| 0        | 7        | Configurable | WWDG        | Window watchdog interrupt<br>0x0000_0040   |
| 1        | 8        | Configurable | PVD         | PVD interrupt (through EXTI line 16)<br>0x0000_0044  |
| 2        | 9        | Configurable | RTC         | RTC interrupt (through EXTI line 17, 19, and 20)<br>0x0000_0048  |
| 3        | 10       | Configurable | Flash       | Flash global interrupt<br>0x0000_004C  |
| 4        | 11       | Configurable | RCC         | RCC global interrupt<br>0x0000_0050  |
| 5        | 12       | Configurable | EXTIO_1     | EXTI Line[1:0] interrupts<br>0x0000_0054   |

| Position | Priority |              | Name            | Description  | Address     |
|----------|----------|--------------|-----------------|--|-------------|
| 6        | 13       | Configurable | EXTI2_3         | EXTI Line[3:2] interrupts                            | 0x0000_0058 |
| 7        | 14       | Configurable | EXTI4_15        | EXTI Line[15:4] interrupts                           | 0x0000_005C |
| 8        | 15       | Configurable | LPUART_IRQ      | LPUART interrupt (through EXTI line 28)              | 0x0000_0060 |
| 9        | 16       | Configurable | DMA_CH1         | DMA channel 1 global interrupt                       | 0x0000_0064 |
| 10       | 17       | Configurable | DMA_CH2_3       | DMA channel 2/3 interrupt                            | 0x0000_0068 |
| 11       | 18       | Configurable | DMA_CH4_7       | DMA channel 4/5/6/7 interrupt                        | 0x0000_006C |
| 12       | 19       | Configurable | ADC             | ADC interrupt (through EXTI line 21, 22, 30, and 31) | 0x0000_0070 |
| 13       | 20       | Configurable | TIM1_BRK_UP_TRG | TIM1 break, update, and trigger interrupt            | 0x0000_0074 |
| 14       | 21       | Configurable | TIM1_CC         | TIM1 capture/compare interrupt                       | 0x0000_0078 |
| 15       | 22       | Configurable | TIM2            | TIM2 global interrupt                                | 0x0000_007C |
| 16       | 23       | Configurable | TIM3            | TIM3 global interrupt                                | 0x0000_0080 |
| 17       | 24       | Configurable | TIM6            | TIM6 global interrupt                                | 0x0000_0084 |
| 18       | 25       | Configurable | LPTIM           | LPTIM global interrupt (through EXTI line 29)        | 0x0000_0088 |
| 19       | 26       | Configurable | TIM14           | TIM14 global interrupt (through EXTI line 32)        | 0x0000_008C |
| 20       | 27       | Configurable | TIM15           | TIM15 global interrupt                               | 0x0000_0090 |
| 21       | 28       | Configurable | TIM16           | TIM16 global interrupt (through EXTI line 33)        | 0x0000_0094 |
| 22       | 29       | Configurable | TIM17           | TIM17 global interrupt                               | 0x0000_0098 |
| 23       | 30       | Configurable | I2C1            | I2C1 global interrupt (through EXTI line 23)         | 0x0000_009C |
| 24       | 31       | Configurable | I2C2            | I2C2 global interrupt (through EXTI line 24)         | 0x0000_00A0 |
| 25       | 32       | Configurable | SPI1            | SPI1 global interrupt (through EXTI line 34)         | 0x0000_00A4 |
| 26       | 33       | Configurable | SPI2            | SPI2 global interrupt (through EXTI line 35)         | 0x0000_00A8 |
| 27       | 34       | Configurable | USART1          | USART1 global interrupt (through EXTI line 25)       | 0x0000_00AC |
| 28       | 35       | Configurable | USART2          | USART2 global interrupt (through EXTI line 26)       | 0x0000_00B0 |
| 29       | 36       | Configurable | AES_TRNG_HASH   | AES, TRNG, and hash interrupt                        | 0x0000_00B4 |
| 30       | 37       | Configurable | CAN             | CAN global interrupt                                 | 0x0000_00B8 |
| 31       | 38       | Configurable | DVSQ            | DVSQ global interrupt                                | 0x0000_00BC |

### 3.12 EXTI

The extended interrupt/event controller (EXTI) manages 27 interrupt lines that are used to generate interrupt/event requests and wake up the system through edge detection. The trigger event of each EXTI line can be configured and masked independently. The trigger event can be a rising edge, a falling edge, or both. The pending register stores the status of each interrupt request. EXTI can detect external interrupt line signals whose pulse width is shorter than the internal clock period. Up to 55 GPIOs can be connected to up to 16 external interrupt lines.

The EXTI lines from EXTI 0 to EXTI 15 are connected to I/O pins. The connections of the other EXTI lines are as follows:

- EXTI 16 connected to the PVD output
- EXTI 17 connected to the RTC alarm event
- EXTI 19 connected to the RTC tamper detection and timestamp event
- EXTI 20 connected to the RTC wakeup event
- EXTI 23 connected to the I2C1 wakeup event

- EXTI 24 connected to the I2C2 wakeup event
- EXTI 25 connected to the USART1 wakeup event
- EXTI 26 connected to the USART2 wakeup event
- EXTI 28 connected to the LPUART wakeup event
- EXTI 29 connected to the LPTIM wakeup event
- EXTI 31 connected to the ADC AWD event

EXTI lines from EXTI 23 to EXTI 26, from EXTI 28 to EXTI 29, and EXTI 31 are connected to internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). These EXTI lines detect the rising edge of events in only Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system. The corresponding interrupt control bit and status bit are stored in the peripheral from which events are generated.

### 3.13 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and an 8-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can work as a watchdog to reset the system when a problem occurs or as a free-running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG\_WINR register to use IWDG in window mode.

### 3.14 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

### 3.15 SysTick timer

The SysTick timer is a dedicated standard downcounter for the operating system. Its features include:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

### 3.16 Timer

Each HK32ASAFE010xB MCU has an advanced timer, six general-purpose timers, a basic timer, and a low-power timer. The features of the timers are listed in the following table.

Table 3-4 Features of the timers

| Type                  | Timer | Counter Resolution | Counter Type      | Prescaler Factor | DMA Request | Break Input | Capture/Compare Channels | Complementary Outputs |
|-----------------------|-------|--------------------|-------------------|------------------|-------------|-------------|--------------------------|-----------------------|
| Advanced timer        | TIM1  | 16-bit             | Up, down, up/down | 0 – 0xFFFF       | Yes         | Yes         | 4                        | 3                     |
| General-purpose timer | TIM2  | 32-bit             | Up, down, up/down | 0 – 0xFFFF       | Yes         | No          | 4                        | No                    |

| Type            | Timer | Counter Resolution | Counter Type      | Prescaler Factor | DMA Request | Break Input | Capture/ Compare Channels | Complementary Outputs |
|-----------------|-------|--------------------|-------------------|------------------|-------------|-------------|---------------------------|-----------------------|
|                 | TIM3  | 16-bit             | Up, down, up/down | 0 – 0xFFFF       | Yes         | No          | 4                         | No                    |
|                 | TIM14 | 16-bit             | Up                | 0 – 0xFFFF       | No          | No          | 1                         | No                    |
|                 | TIM15 | 16-bit             | Up                | 0 – 0xFFFF       | Yes         | Yes         | 2                         | 1                     |
|                 | TIM16 | 16-bit             | Up                | 0 – 0xFFFF       | Yes         | Yes         | 1                         | 1                     |
|                 | TIM17 | 16-bit             | Up                | 0 – 0xFFFF       | Yes         | Yes         | 1                         | 1                     |
| Basic timer     | TIM6  | 16-bit             | Up                | 0 – 0xFFFF       | Yes         | No          | No                        | No                    |
| Low-power timer | LPTIM | 16-bit             | Up                | 1/2/4/..... /128 | No          | No          | 1                         | No                    |

### 3.16.1 Basic timer

HK32ASAFE010xB integrates a basic timer TIM6.

TIM6 embeds a 16-bit upcounter and a 16-bit prescaler.

### 3.16.2 General-purpose timer

HK32ASAFE010xB integrates six general-purpose timers.

- TIM2 and TIM3

TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have four independent channels respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output. In the LQFP64 package, up to 12 channels are available for input capture, output compare, and PWM output.

TIM2 and TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14 and TIM15

TIM14 and TIM15 are based on a 16-bit auto-reload upcounter and a 16-bit prescaler respectively. TIM14 has one channel for input capture, output compare, PWM output, and one-pulse mode output. TIM15 has two channels, one of which is for complementary output. In debug mode, the counter can be frozen. TIM15 can generate DMA requests but TIM14 cannot.

- TIM16 and TIM17

TIM16 and TIM17 are based on a 16-bit auto-reload upcounter and a 16-bit prescaler respectively. TIM16 and TIM17 have a channel respectively for input capture, output compare, PWM output, and one-pulse mode output. TIM16 and TIM17 both have complementary outputs with programmable inserted dead-times and can generate independent DMA requests. In debug mode, the counter can be frozen.

### 3.16.3 Advanced timer

HK32ASAFE010xB integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose

timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output
- Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0–100%). Many functions of TIM1 are the same as those of general-purpose timers. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

### 3.16.4 Low-power timer

HK32ASAFE010xB has a 16-bit low-power timer LPTIM.

LPTIM can work in Sleep mode and Stop mode. If no internal clock source is available, LPTIM can provide the pulse counter function. LPTIM can wake up the system from low-power modes.

The flexible clock schemes provided by LPTIM can minimize the power consumption of the system.

LPTIM has the following functions:

- 16-bit upcounter
- Prescaler (1/2/4/8/16/32/64/128)
- Clock sources for selection
- 16-bit auto-reload register
- 16-bit compare register
- Continuous/One-shot mode
- Software/Hardware input trigger configurable
- Programmable digital filter
- Configurable output mode

### 3.17 IRTIM

An infrared interface (IRTIM) is embedded in each HK32ASAFE010xB MCU. The IRTIM works with infrared LEDs to provide the remote control function. To generate infrared remote control signals, you must enable the IRTIM (PB9) and configure TIM16 channel 1 (TIM16\_OC1) and TIM17 channel 1 (TIM17\_OC1).

The infrared receiver function can be implemented by setting TIM16 channel 1 and TIM17 channel 1 to the basic input capture mode.

### 3.18 I2C

Up to two I2C bus interfaces are embedded in HK32ASAFE010xB MCUs. Each I2C bus interface has an output drive of 30 mA and can operate in master or slave mode at one of the following speeds:

- Standard mode (up to 100 Kbit/s)
- Fast mode (up to 400 Kbit/s)
- Fast mode plus (up to 1 Mbit/s)

The I2C bus interfaces support the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave).

The I2C interfaces embed hardware CRC generation/verification.

The I2C interfaces are compatible with SMBus 2.0 and PMBus 1.1. The address resolution protocol (ARP) capability, host notify protocol, hardware CRC (packet error checking, PEC) generation/verification, timeout verification, and alert protocol management are supported.

The I2C interfaces have a clock independent of the CPU clock domain, so they can wake up the MCU from Stop mode when the address is matched.

The I2C interfaces have an analog filter and a digital filter. The following table lists the features of the filters:

Table 3-5 Programmable analog noise filter and digital noise filter

|                        | Analog Filter  | Digital Filter  |
|------------------------|--|---|
| Suppressed pulse width | ≥ 50 ns  | Programmable length from 1 to 15 I2C peripheral clock periods   |
| Advantage              | Available in Stop mode   | <ul style="list-style-type: none"> <li>Extra filtering capability, standard requirements</li> <li>Stable programmable length</li> </ul> |
| Disadvantage           | Performance changes along with the temperature, voltage, and process | When the digital filter is enabled, I2C cannot wake up the MCU from Stop mode even if the address is matched.                           |

### 3.19 USART

Two universal synchronous/asynchronous receivers/transmitters (USART1 and USART2) are embedded in each HK32ASAFE010xB MCU. They can communicate at up to 12 Mbit/s.

The USARTs provide hardware management for the CTS, RTS, and RS485 DE signals. The USARTs support the multiprocessor communication mode, host synchronous communication mode, and single-wire half-duplex communication mode. The USARTs also support Smart Card communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability, and automatic baud rate detection. The USARTs can be served by the DMA controller.

The USARTs have a clock independent of the CPU clock domain, so they can wake up the MCU from Stop mode.

Table 3-6 USART1/USART2 features

| Feature                                      | USART1/USART2 |
|--|---------------|
| Modem hardware flow control                  | Supported     |
| DMA continuous transmission                  | Supported     |
| Multiprocessor communication                 | Supported     |
| Synchronous mode                             | Supported     |
| Smart Card mode                              | Supported     |
| Single-wire half-duplex communication        | Supported     |
| IrDA SIR ENDEC                               | Supported     |
| LIN mode                                     | Supported     |
| Dual clock domains and wakeup from Stop mode | Supported     |
| Receiver timeout interrupt                   | Supported     |
| Modbus communication                         | Supported     |
| Automatic baud rate detection                | Supported     |
| Driver enable                                | Supported     |

### 3.20 LPUART

HK32ASAFE010xB incorporates a low-power universal asynchronous receiver/transmitter (LPUART) which can communicate at up to 10 Mbit/s. The LPUART supports asynchronous serial communication, single-wire half-duplex communication, and modem operations (CTS/RTS) in low-power mode. It also supports multiprocessor communication.

The LPUART has a clock independent of the CPU clock domain. It can wake up the MCU from Stop mode at a baud rate of up to 4.8 Kbit/s when any of the following events occurs:

- Start bit detection event
- Interrupt of receiving any data frame
- Receiving specific programming data frame

When using the 32.768 kHz LSE, the LPUART can communicate at up to 9600 baud. In Stop mode, the LPUART waits for incoming frames at extremely low power consumption. If the LPUART uses a faster clock, it can communicate at a higher baud rate.

The LPUART can be served by the DMA controller.

### 3.21 SPI/I2S

Up to two SPI interfaces operating at up to 18 Mbit/s are embedded in HK32ASAFE010xB MCUs. The SPI interfaces support master and slave modes and full-duplex or half-duplex communication. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4- to 16-bit.

Table 3-7 SPI1/SPI2 features

| SPI Feature              | SPI1/SPI2 |
|--------------------------|-----------|
| Hardware CRC calculation | Supported |
| RX/TX FIFO               | Supported |
| NSS pulse mode           | Supported |
| I2S mode                 | Supported |
| TI mode                  | Supported |

The standard I2S interfaces (with SPI multiplexed) provide four types of audio standards and can operate in master/slave half-duplex communication mode. The I2S interfaces have dedicated signals for data synchronization. The data format can be 16-bit, 24-bit, or 32-bit and the I2S interfaces can operate with 16- or 32-bit resolution. The I2S interfaces can be set to an audio sampling frequency from 8 kHz to 192 kHz by the 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components.

Table 3-8 I2S features

| I2S Feature                         | I2S       |
|-------------------------------------|-----------|
| Half-duplex mode                    | Supported |
| Master/Slave mode configurable      | Supported |
| 8-bit programmable linear prescaler | Supported |
| Data format programmable            | Supported |
| Clock polarity programmable         | Supported |
| I2S protocol                        | Supported |
| DMA transmission                    | Supported |
| Driving external audio components   | Supported |

### 3.22 GPIO

Each GPIO pin can be configured as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or assigned to a peripheral alternate function by using the software. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current capable. I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

### 3.23 DMA

The 7-channel general-purpose DMA controller manages the data transfer from memories to memories, from devices to memories, and from memories to devices. The DMA controller supports circular buffer management, preventing the interrupt that occurs when the DMA controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by using the software. The length, source, and destination of data to be transferred can be independently set by using the software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, SDIO, and ADC.

### 3.24 ADC

The 12-bit analog-to-digital converter (ADC) has the following functions:

- Up to 16 external channels and three internal channels (temperature sensor, reference voltage, and  $V_{BAT}$ )

- Performs A/D conversion in single-channel or multi-channel scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.
- Can be served by the DMA controller.
- Supports the sampling of  $1/2 V_{BAT}$ .
- Can be triggered by external trigger sources.

The analog watchdog function can realize precise monitoring of one, some, or all selected channels. If the converted voltage exceeds the threshold set by the program, an interrupt is generated.

### 3.25 CAN

The CAN interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN interface has three transmit mailboxes and two 3-stage receive FIFOs. Each FIFO has 14 scalable filters.

### 3.26 RTC clock

In all operating modes of HK32ASAFE010xB (including the Standby mode), a real-time clock (RTC) and five backup registers are provided. The backup registers are 32-bit registers. They are used to store 20 bytes of user application data. The system reset and wakeup from the Standby mode do not reset backup registers.

The RTC has programmable periodic wakeup flags with the interrupt function.

The digital calibration feature compensates for deviation in the crystal oscillator accuracy.

After the RTC domain is reset, unexpected writes to all RTC registers are prevented.

As long as the power supply voltage of the MCU is within the operating range, the RTC keeps working in all modes of the MCU.

The RTC is an independent binary-coded decimal (BCD) timer/counter. It has the following features:

- Calendar with sub-seconds, seconds, minutes, hours (12- or 24-hour format), day of the week, day of the month, month, and year in BCD
- Automatic adjustment to the days of different months: 28 days, 29 days (leap year), 30 days, and 31 days. The adjustment for daylight saving time is also supported.
- Two programmable alarms that can wake up the MCU from Stop or Standby mode
- Programmable resolution and periodic wakeup from Stop or Standby mode
- Correction of 1 to 32,767 RTC clock pulses during runtime for synchronization between RTC and the main clock
- Reference clock detection: a more accurate secondary clock source (50 Hz or 60 Hz) that can improve calendar accuracy
- Digital calibration circuit with 1 ppm resolution for compensation of deviation in the crystal oscillator accuracy
- Two tamper detection pins with programmable filters Wakeup from Stop or Standby mode when any tamper event is detected
- Timestamp feature used for storage of calendar content. The timestamp feature can be triggered by the event on the timestamp pin or by the tamper event. MCUs can be woken up from Stop or Standby mode when any timestamp event is detected.

The RTC clock source can be:

- 32.768 kHz external crystal oscillator



- Low-power internal RC oscillator (typical frequency: 40 kHz)
- HSE divided by 32

## 3.27 Information security

### 3.27.1 AES128

HK32ASAFE010xB integrates an Advanced Encryption Standard 128 (AES128) unit compliant with Federal Information Processing Standards 197 (FIPS 197).

- Supports the Electronic Code Book (ECB) mode
  - Supports the 128-bit, 192-bit, and 256-bit keys for encryption
  - Encryption computation time:
    - 128-bit key: 57 clock periods
    - 192-bit key: 67 clock periods
    - 256-bit key: 77 clock periods
  - Decryption computation time:
    - 128-bit key: 57 clock periods
    - 192-bit key: 67 clock periods
    - 256-bit key: 77 clock periods
  - After calling a single decryption operation, enter the decryption key in the AES\_KEYRx register again. Even if the decryption key adopted in this decryption is the same as that of the previous decryption, you still need to enter the decryption key again.
- Supports the randomization of the AES clock by using TRNG.
- More convenient protection of the register content and easier resumption of the context when interrupts occur.
- Supports data transmission by using DMA (two DMA channels required)

### 3.27.2 Hash

The hash module is applicable to data authentication applications. It is compliant with the following protocols:

- Federal Information Processing Standards Publications 180-2 (FIPS PUB 180-2)
- Secure Hash Algorithm 256 (SHA-256)

The SHA-256 fast computation processing module is a slave peripheral attached to the AHB. It receives 32-bit data in words, half words, bytes, and bits. The SHA-256 module only supports data stored in little-endian mode.

The input data in little-endian mode is automatically converted to the big-endian mode adopted by SHA-256. The last input data in little-endian mode is automatically padded to fit the digest minimum block size of 512 bits (16 × 32 bits). The digest of the whole message is obtained by adding the 32-bit words of the digests of consecutive message blocks. The data flow can be automatically controlled by using DMA.

### 3.27.3 TRNG

The true random number generator (TRNG) provides a 32-bit random number based on continuous analog noise when the CPU reads data. TRNG has the following features:

- Provides 32-bit random numbers generated by the analog generator.
- The interval at which two random numbers are generated is 40 RNG\_CLK (48 MHz) periods.
- The entropy of RNG is monitored to identify exceptional behaviors (generation of stable values or stable value sequences).

- TRNG can be disabled to reduce system power consumption.

### 3.28 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32ASAFE010xB integrates a CRC hardware calculation unit. It is used to get a CRC code from an 8-, 16- or 32-bit data word by using a generator polynomial.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with a reference signature, which is generated at link time and stored at a specified memory location.

### 3.29 DVSQ calculation unit

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - The DVSQ calculation unit supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in the division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports divide-by-zero interrupt and overflow interrupt.

### 3.30 Internal reference voltage

The internal reference voltage  $V_{REFINT}$  provides a stable voltage output for the ADC.  $V_{REFINT}$  is internally connected to the ADC\_IN17 input channel. The  $V_{REFINT}$  memory address can only be read.

Table 3-9 Internal voltage benchmark value

| Value Name        | Description  | Memory Address          |
|-------------------|--|-------------------------|
| $V_{REFINT\_CAL}$ | The original data obtained under 25°C temperature. $V_{DDA} = 3.3\text{ V}$ ( $\pm 10\text{ mV}$ ) | 0x1FFF F7BA-0x1FFF F7BB |

### 3.31 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1\_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The temperature sensor is accurate, but it still needs to be calibrated to ensure the accuracy of overall temperature measurement. The temperature sensor offset of different MCUs varies based on the manufacturing processes of the MCUs. Therefore, uncalibrated temperature sensors are suited only for applications that measure temperature changes. All HK32ASAFE010xB MCUs are factory-calibrated to guarantee the measurement accuracy of the temperature sensors. The factory calibration data of temperature sensors is stored in the system memory and can only be read.

### 3.32 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32ASAFE010xB MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.

- To activate the boot processes that have the security mechanism.

### 3.33 Debug port

Based on the ARM SWJ-DP embedded in HK32ASAFE010xB, SWDIO/SWCLK functions are available.

## 4 Electrical characteristics

### 4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Note:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in [Table 4-1](#) to [Table 4-24](#) may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

#### 4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

| Symbol               | Description  | Min            | Max      | Unit |
|----------------------|--|----------------|----------|------|
| $V_{DD} - V_{SS}$    | External main power supply voltage (including $V_{DDA}$ and $V_{DD}$ ) | -0.3           | 3.75     | V    |
| $V_{IN}$             | Input voltage on pins  | $V_{SS} - 0.3$ | $V_{DD}$ |      |
| $ \Delta V_{DDX} $   | Variation between different power pins                                 | -              | 50       | mV   |
| $ V_{SSX} - V_{SS} $ | Variation between different ground pins                                | -              | 50       |      |

#### 4.1.2 Current characteristics

Table 4-2 Current characteristics

| Symbol                | Description   | Max  | Unit |
|-----------------------|---|------|------|
| $I_{VDD}$             | Total current into $V_{DD}/V_{DDA}$ (source) <sup>(1)</sup>       | 100  | mA   |
| $I_{VSS}$             | Total current from $V_{SS}$ (sink) <sup>(1)</sup>                 | -100 |      |
| $I_{IO}$              | Output current sunk by any I/O and control pin                    | 20   |      |
|                       | Output current sourced by any I/O and control pin                 | -40  |      |
| $I_{INJ(PIN)}^{(2)}$  | Injected current on pins <sup>(3)</sup>                           | ±5   |      |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (all I/Os and control pins) <sup>(4)</sup> | ±25  |      |

- (1). All power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must be connected to the external power supply within the permitted range all the time.
- (2). Negative injected current causes the analog performance of the device to fluctuate.
- (3). When  $V_{IN}$  is larger than  $V_{DD}$ , a positive injected current is induced; when  $V_{IN}$  is smaller than  $V_{SS}$ , a negative injected current is induced. The injected current must be within the permitted range.
- (4). If multiple I/Os have current injection simultaneously, the maximum  $\Sigma I_{INJ(PIN)}$  is the sum of the absolute instantaneous values of positive and negative injected currents.

#### 4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

| Symbol    | Description                  | Value       | Unit |
|-----------|------------------------------|-------------|------|
| $T_{STG}$ | Storage temperature range    | -45 to +125 | °C   |
| $T_J$     | Maximum junction temperature | 125         |      |

## 4.2 Operating conditions

### 4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

| Symbol      | Description                   | Min | Max | Unit |
|-------------|-------------------------------|-----|-----|------|
| $f_{HCLK}$  | Internal AHB clock frequency  | 0   | 96  | MHz  |
| $f_{PCLK1}$ | Internal APB1 clock frequency | 0   | 96  |      |
| $f_{PCLK2}$ | Internal APB2 clock frequency | 0   | 96  |      |

| Symbol                          | Description                | Min | Max | Unit |
|---------------------------------|----------------------------|-----|-----|------|
| V <sub>DD</sub>                 | Standard operating voltage | 1.8 | 3.6 | V    |
| V <sub>DDA</sub> <sup>(1)</sup> | Analog operating voltage   | 1.8 | 3.6 | V    |
| T                               | Operating temperature      | -40 | 105 | °C   |

(1). V<sub>DDA</sub> can be lower than V<sub>DD</sub>. For example, V<sub>DD</sub> = 3.6 V, V<sub>DDA</sub> = 3.3 V; V<sub>DD</sub> = 3.3 V, V<sub>DDA</sub> = 2.5 V.

## 4.2.2 PVD characteristics

Table 4-5 PVD characteristics

| Symbol           | Parameter  | Condition      | Min  | Typ  | Max  | Unit |
|------------------|--|----------------|------|------|------|------|
| V <sub>PVD</sub> | Programmable voltage detector level selection (V <sub>DD</sub> rising edge)  | PLS[2:0] = 000 | 2.10 | 2.23 | 2.36 | V    |
|                  |  | PLS[2:0] = 001 | 2.19 | 2.33 | 2.47 |      |
|                  |  | PLS[2:0] = 010 | 2.31 | 2.43 | 2.55 |      |
|                  |  | PLS[2:0] = 011 | 2.40 | 2.53 | 2.66 |      |
|                  |  | PLS[2:0] = 100 | 2.49 | 2.63 | 2.77 |      |
|                  |  | PLS[2:0] = 101 | 2.60 | 2.74 | 2.88 |      |
|                  |  | PLS[2:0] = 110 | 2.68 | 2.84 | 3.00 |      |
|                  | Programmable voltage detector level selection (V <sub>DD</sub> falling edge) | PLS[2:0] = 000 | 2.11 | 2.21 | 2.31 |      |
|                  |  | PLS[2:0] = 001 | 2.21 | 2.31 | 2.41 |      |
|                  |  | PLS[2:0] = 010 | 2.31 | 2.41 | 2.51 |      |
|                  |  | PLS[2:0] = 011 | 2.40 | 2.51 | 2.62 |      |
|                  |  | PLS[2:0] = 100 | 2.50 | 2.61 | 2.72 |      |
|                  |  | PLS[2:0] = 101 | 2.59 | 2.71 | 2.83 |      |
|                  |  | PLS[2:0] = 110 | 2.69 | 2.81 | 2.93 |      |
| PLS[2:0] = 111   | 2.78   | 2.91           | 3.04 |      |      |      |

## 4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

| Symbol                               | Parameter         | Condition                   | Min | Typ  | Max  | Unit |
|--------------------------------------|-------------------|-----------------------------|-----|------|------|------|
| V <sub>POR/PDR</sub> <sup>(1)</sup>  | POR/PDR threshold | Falling edge <sup>(2)</sup> | -   | 1.70 | -    | V    |
|                                      |                   | Rising edge                 | -   | 1.64 | -    | V    |
| V <sub>PDRhyst</sub>                 | PDR hysteresis    | -                           | -   | 60   | -    | mV   |
| t <sub>RSTTEMPO</sub> <sup>(3)</sup> | Reset duration    | -                           | 3.0 | 3.50 | 4.50 | ms   |

(1) PDR is based on the monitoring of V<sub>DD</sub> and V<sub>DDA</sub>. POR is based on the monitoring of only V<sub>DD</sub>.

(2) The actual performance value is guaranteed to be smaller than the minimum V<sub>POR/PDR</sub> value.

(3) The value is guaranteed in design.

## 4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

| Symbol              | Parameter                  | Condition      | Min  | Typ | Max  | Unit |
|---------------------|----------------------------|----------------|------|-----|------|------|
| V <sub>REFINT</sub> | Internal reference voltage | -40°C to 105°C | 1.15 | 1.2 | 1.23 | V    |

## 4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

| Mode | Condition   | Parameter         | -40°C,<br>V <sub>DD</sub> = 3.3 V | 25°C,<br>V <sub>DD</sub> = 3.3 V | 85°C,<br>V <sub>DD</sub> = 3.3 V | 105°C,<br>V <sub>DD</sub> = 3.3 V | Unit |
|------|---|-------------------|-----------------------------------|----------------------------------|----------------------------------|-----------------------------------|------|
| Run  | HCLK = 96 MHz,<br>seven wait states for<br>FLASH_LATENCY, APB clock enabled | Operating current | 10.636                            | 9.777                            | 10.301                           | 10.743                            | mA   |

| Mode                                       | Condition   | Parameter         | -40°C,<br>V <sub>DD</sub> = 3.3 V | 25°C,<br>V <sub>DD</sub> = 3.3 V | 85°C,<br>V <sub>DD</sub> = 3.3 V | 105°C,<br>V <sub>DD</sub> = 3.3 V | Unit |
|--|---|-------------------|-----------------------------------|----------------------------------|----------------------------------|-----------------------------------|------|
|  | HCLK = 96 MHz,<br>seven wait states for<br>FLASH_LATENCY, APB clock disabled          |                   | 6.933                             | 6.062                            | 6.578                            | 7.008                             | mA   |
|  | HCLK = HSE (8 MHz),<br>zero wait states for FLASH_LATENCY,<br>APB clock enabled       |                   | 2.857                             | 1.950                            | 2.433                            | 2.844                             | mA   |
|  | HCLK = HSE (8 MHz),<br>zero wait states for FLASH_LATENCY,<br>APB clock disabled      |                   | 2.543                             | 1.641                            | 2.122                            | 2.533                             | mA   |
|  | HCLK = LSE (32.768 kHz),<br>zero wait states for FLASH_LATENCY,<br>APB clock enabled  |                   | 0.995                             | 1.080                            | 1.567                            | 1.912                             | mA   |
|  | HCLK = LSE (32.768 kHz),<br>zero wait states for FLASH_LATENCY,<br>APB clock disabled |                   | 0.994                             | 1.078                            | 1.565                            | 1.908                             | mA   |
|  | HCLK = LSI (40 kHz),<br>zero wait states for FLASH_LATENCY,<br>APB clock enabled      |                   | 0.996                             | 1.080                            | 1.517                            | 1.914                             | mA   |
|  | HCLK = LSI (40 kHz),<br>zero wait states for FLASH_LATENCY,<br>APB clock disabled     |                   | 0.994                             | 1.079                            | 1.514                            | 1.909                             | mA   |
| Sleep                                      | HCLK = HSE (96 MHz),<br>APB clock disabled  | Operating current | 5.676                             | 4.786                            | 5.286                            | 5.710                             | mA   |
|  | HCLK = HSI (8 MHz),<br>APB clock disabled   | Operating current | 1.275                             | 1.363                            | 1.796                            | 2.191                             | mA   |
|  |   | Wakeup time       | -                                 | 4.7                              | -                                | -                                 | μs   |
|  | HCLK = LSE (32.768 kHz),<br>APB clock disabled  | Operating current | 0.993                             | 1.077                            | 1.561                            | 1.905                             | mA   |
| HCLK = LSI (40 kHz),<br>APB clock disabled | Operating current   | 0.993             | 1.077                             | 1.510                            | 1.905                            | mA                                |      |
| Stop                                       | LDO operating at full speed<br>HSE/HSI/LSE disabled<br>IWDG disabled                  | Operating current | 0.628                             | 0.688                            | 1.099                            | 1.487                             | mA   |
|  |   | Wakeup time       | -                                 | 20                               | -                                | -                                 | μs   |
|  | LDO in the low-power state<br>HSE/HSI/LSE disabled<br>IWDG disabled                   | Operating current | 18.227                            | 60.026                           | 393.768                          | 708.269                           | μA   |
|  |   | Wakeup time       | -                                 | 132                              | -                                | -                                 | μs   |
| Standby                                    | LSI and IWDG enabled  | Operating current | 1.834                             | 2.254                            | 6.004                            | 10.898                            | μA   |
|  |   | Wakeup time       | -                                 | 152                              | -                                | -                                 | μs   |
|  | LSI enabled, IWDG disabled  | Operating current | 1.829                             | 2.253                            | 5.993                            | 10.883                            | μA   |
|  |   | Wakeup time       | -                                 | 152                              | -                                | -                                 | μs   |
|  | All oscillators disabled.   | Operating current | 1.154                             | 1.642                            | 5.393                            | 10.285                            | μA   |
|  |   | Wakeup time       | -                                 | 152                              | -                                | -                                 | μs   |
| Shutdown                                   | LSE enabled and RTC running<br>(BKPPDS = 0)   | Operating current | 1.465                             | 2.002                            | 165.692                          | 10.606                            | μA   |
|  |   | Wakeup time       | -                                 | 96                               | -                                | -                                 | μs   |
|  | LSE disabled and RTC stopped<br>(BKPPDS = 0)  | Operating current | 1.152                             | 1.633                            | 5.306                            | 10.112                            | μA   |
|  |   | Wakeup time       | -                                 | 96                               | -                                | -                                 | μs   |
|  | LSE and RTC disabled (BKPPDS = 1)   | Operating current | 0.319                             | 0.406                            | 1.027                            | 2.446                             | μA   |

| Mode | Condition | Parameter   | -40°C,<br>V <sub>DD</sub> = 3.3 V | 25°C,<br>V <sub>DD</sub> = 3.3 V | 85°C,<br>V <sub>DD</sub> = 3.3 V | 105°C,<br>V <sub>DD</sub> = 3.3 V | Unit |
|------|-----------|-------------|-----------------------------------|----------------------------------|----------------------------------|-----------------------------------|------|
|      |           | Wakeup time | -                                 | 364                              | -                                | -                                 | μs   |

## 4.2.6 HSE clock characteristics

Table 4-9 HSE clock characteristics

| Symbol                | Parameter   | Condition   | Min | Typ  | Max | Unit |
|-----------------------|---|---|-----|------|-----|------|
| f <sub>OSC_IN</sub>   | Oscillator frequency  | -   | 4   | 8    | 32  | MHz  |
| R <sub>F</sub>        | Feedback resistor   | -   | -   | 2    | -   | MΩ   |
| T <sub>SU (HSE)</sub> | Oscillator startup time   | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>                       | 3   | -    | 4   | μs   |
| C                     | Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (R <sub>S</sub> ) | -   | -   | 12.5 | -   | PF   |
| I <sub>DD (HSE)</sub> | HSE oscillator power consumption  | Normal operation: V <sub>DD</sub> = 3.3 V, C <sub>L</sub> = 12.5 pF@8 MHz | 60  | 100  | 300 | μA   |

HK32ASAFE010xB integrates an HSE negative feedback circuit supplied with a resonator. The following crystal oscillator circuit outside the chip is recommended:

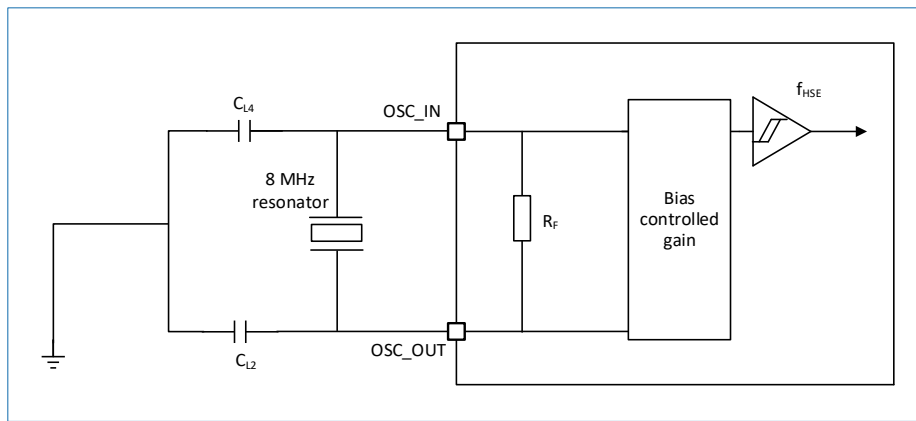


Figure 4-1 HSE negative feedback circuit

Alternatively, HK32ASAFE010xB can be clocked from the OSC\_IN pin. The following table lists the requirements for this clock signal:

Table 4-10 Characteristics of the input HSE clock

| Symbol                                   | Parameter                                  | Condition | Min                | Typ | Max                | Unit |
|--|--|-----------|--------------------|-----|--------------------|------|
| f <sub>HSE_ext</sub>                     | External clock source frequency            | -         | 1                  | 8   | 25                 | MHz  |
| V <sub>HSEH</sub>                        | High level voltage on the OSC_IN input pin | -         | 0.7V <sub>DD</sub> | -   | V <sub>DD</sub>    | V    |
| V <sub>HSEL</sub>                        | Low level voltage on the OSC_IN input pin  | -         | V <sub>SS</sub>    | -   | 0.3V <sub>DD</sub> | V    |
| t <sub>H(HSE)</sub> /t <sub>L(HSE)</sub> | High or low time of OSC_IN                 | -         | 5                  | -   | -                  | ns   |
| t <sub>r(HSE)</sub> /t <sub>f(HSE)</sub> | Rise or fall time of OSC_IN                | -         | -                  | -   | 20                 | ns   |
| C <sub>in(HSE)</sub>                     | OSC_IN input capacitance                   | -         | -                  | 5   | -                  | pF   |
| DuCy <sub>(HSE)</sub>                    | Duty cycle                                 | -         | 45                 | -   | 55                 | %    |

## 4.2.7 LSE clock characteristics

 Table 4-11 LSE clock characteristics (f<sub>LSE</sub> = 32.768 kHz)

| Symbol                | Parameter  | Condition   | Min | Typ  | Max  | Unit |
|-----------------------|--|---|-----|------|------|------|
| R <sub>F</sub>        | Feedback resistor  | -   | -   | 2    | -    | MΩ   |
| T <sub>SU (LSE)</sub> | Oscillator startup time  | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> | -   | -    | 2000 | ms   |
| C                     | Recommended load capacitance minus equivalent serial resistance of the crystal | -   | -   | 12.5 | -    | pF   |

| Symbol        | Parameter                        | Condition   | Min | Typ | Max | Unit          |
|---------------|----------------------------------|---|-----|-----|-----|---------------|
|               | oscillator                       |   |     |     |     |               |
| $I_2$         | LSE driving current              | -   | -   | 400 | -   | nA            |
| $I_{DD(LSE)}$ | LSE oscillator power consumption | Normal operation:<br>$V_{DD} = 3.3\text{ V}$ , $CL = 12.5\text{ pF}@8\text{ MHz}$ | -   | 80  | 100 | $\mu\text{A}$ |

HK32ASAFE010xB integrates an LSE negative feedback circuit supplied with a resonator. The following crystal oscillator circuit outside the chip is recommended:

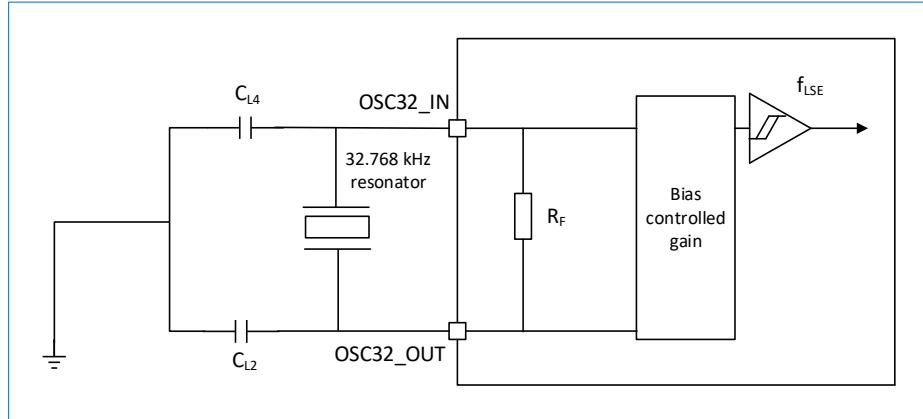


Figure 4-2 LSE negative feedback circuit

Alternatively, HK32ASAFE010xB can be clocked from the OSC32\_IN pin. The following table lists the requirements for this clock signal.

Table 4-12 Characteristics of the input LSE clock

| Symbol                  | Parameter                                  | Condition | Min         | Typ    | Max         | Unit |
|-------------------------|--|-----------|-------------|--------|-------------|------|
| $f_{LSE\_ext}$          | External clock source frequency            | -         | -           | 32.768 | 1000        | kHz  |
| $V_{LSEH}$              | High level voltage on the OSC_IN input pin | -         | $0.7V_{DD}$ | -      | $V_{DD}$    | V    |
| $V_{LSEL}$              | Low level voltage on the OSC_IN input pin  | -         | $V_{SS}$    | -      | $0.3V_{DD}$ | V    |
| $t_{H(LSE)}/t_{L(LSE)}$ | High or low time of OSC_IN                 | -         | 450         | -      | -           | ns   |
| $t_{r(LSE)}/t_{f(LSE)}$ | Rise or fall time of OSC_IN                | -         | -           | -      | 50          | ns   |
| $C_{in(LSE)}$           | OSC_IN input capacitance                   | -         | -           | 5      | -           | pF   |
| $DuCy_{(LSE)}$          | Duty cycle                                 | -         | 30          | -      | 70          | %    |

## 4.2.8 HSI clock characteristics

Table 4-13 HSI clock characteristics

| Symbol         | Parameter                    | Condition   | Min   | Typ  | Max | Unit          |     |
|----------------|------------------------------|---|---|------|-----|---------------|-----|
| $f_{HSI}$      | Frequency                    | -   | -   | 8    | -   | MHz           |     |
| $DuCy_{(HSI)}$ | Duty cycle                   | -   | 45  | -    | 55  | %             |     |
| $ACC_{(HSI)}$  | Oscillator accuracy          | RCC_CR register calibration completed by the user | -   | -    | 1   | %             |     |
|                |                              | Factory calibrated                                | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ | -1.5 | -   |               | 1.5 |
|                |                              |   | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$  | -1.0 | -   |               | 1.0 |
|                |                              | $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$    | -1.0  | -    | 1.0 |               |     |
| $T_{su(HSI)}$  | Oscillator startup time      | $V_{SS} \leq V_{IN} \leq V_{DD}$                  | 3   | -    | 4   | $\mu\text{s}$ |     |
| $I_{DD(HSI)}$  | Oscillator power consumption | -   | -   | 80   | 100 | $\mu\text{A}$ |     |

## 4.2.9 LSI clock characteristics

Table 4-14 LSI clock characteristics

| Symbol        | Parameter               | Condition                        | Min | Typ | Max | Unit          |
|---------------|-------------------------|----------------------------------|-----|-----|-----|---------------|
| $f_{LSI}$     | Frequency               | -                                | 34  | 40  | 46  | kHz           |
| $T_{su(LSI)}$ | Oscillator startup time | $V_{SS} \leq V_{IN} \leq V_{DD}$ | -   | 150 | -   | $\mu\text{s}$ |



| Symbol               | Parameter                    | Condition | Min | Typ | Max | Unit |
|----------------------|------------------------------|-----------|-----|-----|-----|------|
| I <sub>DD(LSI)</sub> | Oscillator power consumption | -         | -   | 0.5 | -   | μA   |

#### 4.2.10 PLL characteristics

Table 4-15 PLL characteristics

| Symbol               | Parameter              | Min | Typ | Max | Unit |
|----------------------|------------------------|-----|-----|-----|------|
| f <sub>PLL_IN</sub>  | Input clock frequency  | 2   | 8.0 | 80  | MHz  |
|                      | Input clock duty cycle | 40  | -   | 60  | %    |
| f <sub>PLL_OUT</sub> | Output clock frequency | 16  | -   | 120 | MHz  |
| t <sub>LOCK</sub>    | PLL lock time          | -   | 80  | 120 | μs   |
| Jitter               | Cycle-to-cycle jitter  | -   | 5   | 13  | ps   |

#### 4.2.11 Flash memory characteristics

Table 4-16 Flash memory characteristics

| Symbol               | Parameter                         | Min     | Typ <sup>(1)</sup> | Max | Unit   |
|----------------------|-----------------------------------|---------|--------------------|-----|--------|
| T <sub>PROG</sub>    | Half word programming time        | -       | 42                 | -   | μs     |
|                      | One-word programming time         | -       | 42                 | -   | μs     |
| T <sub>ERASE</sub>   | Half page erase time              | -       | 3.7                | -   | ms     |
|                      | Page erase time                   | -       | 7.45               | -   | ms     |
|                      | Mass erase time                   | -       | 190                | -   | ms     |
| I <sub>DDPROG</sub>  | Programming current               | -       | 1.5                | 5   | mA     |
| I <sub>DDERASE</sub> | Page/Mass erase current           | -       | 0.9                | 2   | mA     |
| I <sub>DDREAD</sub>  | Supply current@24 MHz (read mode) | -       | 2.5                | -   | mA     |
| N <sub>END</sub>     | Erase endurance                   | 100,000 | -                  | -   | Cycles |
| t <sub>RET</sub>     | Data retention                    | 10      | -                  | -   | Years  |

(1). The typical values are obtained in the following conditions: 1.5 V, TT process corner, 25°C.

#### 4.2.12 I/O pin input characteristics

Table 4-17 I/O pin input direct current characteristics

| Symbol             | Parameter                          | Condition  | Min  | Typ | Max  | Unit |
|--------------------|------------------------------------|--|------|-----|------|------|
| V <sub>IH</sub>    | Input high level voltage           | V <sub>DD</sub> = 3.3 V                              | 1.82 | -   | -    | V    |
| V <sub>IL</sub>    | Input low level voltage            | V <sub>DD</sub> = 3.3 V                              | -    | -   | 1.3  | V    |
| V <sub>IHhys</sub> | Input high level voltage           | V <sub>DD</sub> = 3.3 V                              | 1.64 | -   | -    | V    |
| V <sub>ILhys</sub> | Input low level voltage            | V <sub>DD</sub> = 3.3 V                              | -    | -   | 1.44 | V    |
| V <sub>hys</sub>   | Schmitt trigger voltage hysteresis | V <sub>DD</sub> = 3.3 V                              | -    | 160 | -    | mV   |
| I <sub>lkg</sub>   | Input leakage current              | V <sub>DD</sub> = 3.3 V; 0 < V <sub>IN</sub> < 3.3 V | -    | -   | 0.01 | μA   |
|                    |                                    | V <sub>DD</sub> = 3.3 V; V <sub>IN</sub> = 5 V       | -    | -   | 1.65 | μA   |
| R <sub>PU</sub>    | Pull-up resistor                   | V <sub>IN</sub> = V <sub>SS</sub>                    | -    | 33  | -    | kΩ   |
| R <sub>PD</sub>    | Pull-down resistor                 | V <sub>IN</sub> = V <sub>DD</sub>                    | -    | 34  | -    | kΩ   |
| C <sub>IO</sub>    | I/O pin capacitance                | -  | -    | 5   | -    | pF   |

#### 4.2.13 I/O pin output characteristics

Table 4-18 I/O pin output alternating current characteristics

| Mode OSPEEDy[1:0] | Symbol               | Parameter                          | Condition                           | Min | Typ  | Max | Unit |
|-------------------|----------------------|------------------------------------|-------------------------------------|-----|------|-----|------|
| x0                | t <sub>f(I)out</sub> | Output high to low level fall time | CL = 50 pF, V <sub>DD</sub> = 3.3 V | -   | 9.50 | -   | ns   |
|                   | t <sub>r(I)out</sub> | Output low to high level rise time |                                     | -   | 22.7 | -   | ns   |
| 01                | t <sub>f(I)out</sub> | Output high to low level fall time | CL = 50 pF, V <sub>DD</sub> = 3.3 V | -   | 5.0  | -   | ns   |
|                   | t <sub>r(I)out</sub> | Output low to high level rise time |                                     | -   | 6.70 | -   | ns   |
| 11                | t <sub>f(I)out</sub> | Output high to low level fall time | CL = 50 pF, V <sub>DD</sub> = 3.3 V | -   | 4.25 | -   | ns   |

| Mode                           | Symbol          | Parameter                          | Condition                           | Min | Typ  | Max | Unit |
|--------------------------------|-----------------|------------------------------------|-------------------------------------|-----|------|-----|------|
| OSPEEDy[1:0]                   |                 |                                    |                                     |     |      |     |      |
|                                | $t_{r(I/O)out}$ | Output low to high level rise time |                                     | -   | 5.00 | -   | ns   |
| OSPEEDy[1:0] = 11 and UHDy = 1 | $t_{f(I/O)out}$ | Output high to low level fall time | CL = 50 pF, V <sub>DD</sub> = 3.3 V | -   | 3.35 | -   | ns   |
|                                | $t_{r(I/O)out}$ | Output low to high level rise time |                                     | -   | 3.85 | -   | ns   |

#### 4.2.14 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-19 NRST pin input characteristics

| Symbol             | Parameter                  | Min | Max | Unit |
|--------------------|----------------------------|-----|-----|------|
| T <sub>Noise</sub> | Low level ignored duration | -   | 50  | ns   |

#### 4.2.15 TIM timer characteristics

Table 4-20 TIM pin input characteristics

| Symbol           | Condition                                    | Min | Max                                    | Unit |
|------------------|--|-----|--|------|
| F <sub>EXT</sub> | Timer external clock frequency on CH1 to CH4 | 0   | F <sub>TIMxCLK</sub> /2 <sup>(1)</sup> | MHz  |

(1). f<sub>TIMxCLK</sub> = 96 MHz

#### 4.2.16 ADC characteristics

Table 4-21 ADC characteristics

| Item                             | Description  | Condition  | Min   | Typ | Max              | Unit                 |
|----------------------------------|--|--|-------|-----|------------------|----------------------|
| V <sub>DDA</sub>                 | Analog power supply voltage when ADC is enabled  | -  | 2.4   | -   | 3.6              | V                    |
| INL                              | Integral non linearity (maximum difference between the actual conversion point and the end point correlation line) | f <sub>ADC</sub> = 14 MHz<br>R <sub>AIN</sub> < 10 kΩ<br>Test after calibration<br>V <sub>DDA</sub> = 2.4 V to 3.6 V | -     | ±1  | -2 to 3          | LSB                  |
| DNL                              | Differential non linearity (maximum difference between the actual step and the ideal step)                         | f <sub>ADC</sub> = 14 MHz<br>R <sub>AIN</sub> < 10 kΩ<br>Test after calibration<br>V <sub>DDA</sub> = 2.4 V to 3.6 V | -     | ±1  | -2 to 3          | LSB                  |
| f <sub>ADC</sub>                 | ADC clock frequency  | -  | 0.6   | -   | 14               | MHz                  |
| f <sub>S</sub> <sup>(1)</sup>    | Sampling frequency   | -  | 0.05  | -   | 1                | MHz                  |
| f <sub>TRIG</sub> <sup>(1)</sup> | External trigger frequency   | f <sub>ADC</sub> = 14 MHz  | -     | -   | 823              | kHz                  |
|                                  |  | -  | -     | -   | 17               | 1/f <sub>ADC</sub>   |
| V <sub>AIN</sub>                 | Conversion voltage range   | -  | 0     | -   | V <sub>DDA</sub> | V                    |
| R <sub>AIN</sub> <sup>(1)</sup>  | External input impedance   | For details, see <a href="#">Table 4-22</a> .  | -     | -   | 60               | kΩ                   |
| R <sub>ADC</sub> <sup>(1)</sup>  | Sampling switch resistance   | -  | -     | -   | 1                | kΩ                   |
| C <sub>ADC</sub> <sup>(1)</sup>  | Sampling and hold capacitor  | -  | -     | -   | 5                | pF                   |
| t <sub>CAL</sub> <sup>(2)</sup>  | ADC calibration time   | f <sub>ADC</sub> = 14 MHz  | 5.9   | -   | -                | μs                   |
|                                  |  | -  | 8.3   | -   | -                | 1/f <sub>ADC</sub>   |
| t <sub>iatr</sub>                | Trigger conversion latency   | f <sub>ADC</sub> = f <sub>PCLK</sub> /2 = 14 MHz   | 0.196 | -   | -                | μs                   |
|                                  |  | f <sub>ADC</sub> = f <sub>PCLK</sub> /2  | 5.5   | -   | -                | 1/f <sub>PCLK</sub>  |
|                                  |  | f <sub>ADC</sub> = f <sub>PCLK</sub> /4 = 12 MHz   | 0.219 | -   | -                | μs                   |
|                                  |  | f <sub>ADC</sub> = f <sub>PCLK</sub> /4  | 10.5  | -   | -                | 1/f <sub>PCLK</sub>  |
|                                  |  | f <sub>ADC</sub> = f <sub>HSI14</sub> = 14 MHz   | 0.188 | -   | 0.259            | μs                   |
| Jitter <sub>ADC</sub>            | Jitters triggered by ADC conversions   | f <sub>ADC</sub> = f <sub>HSI14</sub>  | -     | 1   | -                | 1/f <sub>HSI14</sub> |
| t <sub>S</sub> <sup>(1)</sup>    | Sampling time  | f <sub>ADC</sub> = 14 MHz  | 0.107 | -   | 17.1             | μs                   |

| Item                             | Description                                     | Condition                                      | Min   | Typ | Max   | Unit               |
|----------------------------------|---|--|---|-----|-------|--------------------|
|                                  |   | -  | 1.5   | -   | 239.5 | 1/f <sub>ADC</sub> |
| t <sub>STAB</sub> <sup>(1)</sup> | Sampling stable time                            | -  | 14  |     |       | μs                 |
| t <sub>CONV</sub> <sup>(1)</sup> | Total conversion time (including sampling time) | f <sub>ADC</sub> = 14 MHz<br>12-bit resolution | 1   | -   | 18    | μs                 |
|                                  |   | 12-bit resolution                              | 14 to 252 (t <sub>CONV</sub> = sampling time t <sub>s</sub> + conversion time 12.5) |     |       | 1/f <sub>ADC</sub> |

- (1). The value is guaranteed in design but not tested in production.  
 (2). The value is measured based on the ADC clock. The register access latency is not taken into account.

The calculation formula of the maximum input impedance R<sub>AIN</sub>:

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-22 Maximum input impedance values (f<sub>ADC</sub> = 14 MHz)

| Sampling Cycles (Cycles) | Sampling Time t <sub>S</sub> (μs) | Maximum Input Impedance (kΩ) |
|--------------------------|-----------------------------------|------------------------------|
| 1.5                      | 0.11                              | 1.21                         |
| 7.5                      | 0.54                              | 10.05                        |
| 13.5                     | 0.96                              | 18.88                        |
| 28.5                     | 2.04                              | 40.97                        |
| 41.5                     | 2.96                              | 60.12                        |
| 55.5                     | 3.96                              | 80.74                        |
| 71.5                     | 5.11                              | N/A                          |
| 239.5                    | 17.1                              | N/A                          |

Table 4-23 ADC accuracy

| Symbol | Parameter                                   | Test Condition   | Typ     | Max     | Unit |
|--------|---|--|---------|---------|------|
| ET     | Total unadjusted error <sup>(1)</sup>       | SystemCLK = 56 MHz<br>ADCCLK = 14 MHz<br>Input impedance < 10 kΩ<br>V <sub>DD</sub> = V <sub>DDA</sub> = 3.305 V<br>Test after ADC calibration | -1 to 1 | -2 to 3 | LSB  |
| EO     | Offset error <sup>(2)</sup>                 |  | 1       | 0 to 2  |      |
| EG     | Gain error <sup>(3)</sup>                   |  | 3       | 1 to 3  |      |
| ED     | Differential linearity error <sup>(4)</sup> |  | -1 to 1 | -2 to 3 |      |
| EL     | Integral linearity error <sup>(5)</sup>     |  | -1 to 1 | -2 to 3 |      |

- (1). Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.  
 (2). Offset error: The deviation between the first actual conversion and the first ideal conversion.  
 (3). Gain error: The deviation between the last ideal conversion and the last actual conversion.  
 (4). Differential linearity error: The maximum deviation between the actual step and the ideal step.  
 (5). Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With restricted V<sub>DDA</sub>, frequency, and temperature ranges, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

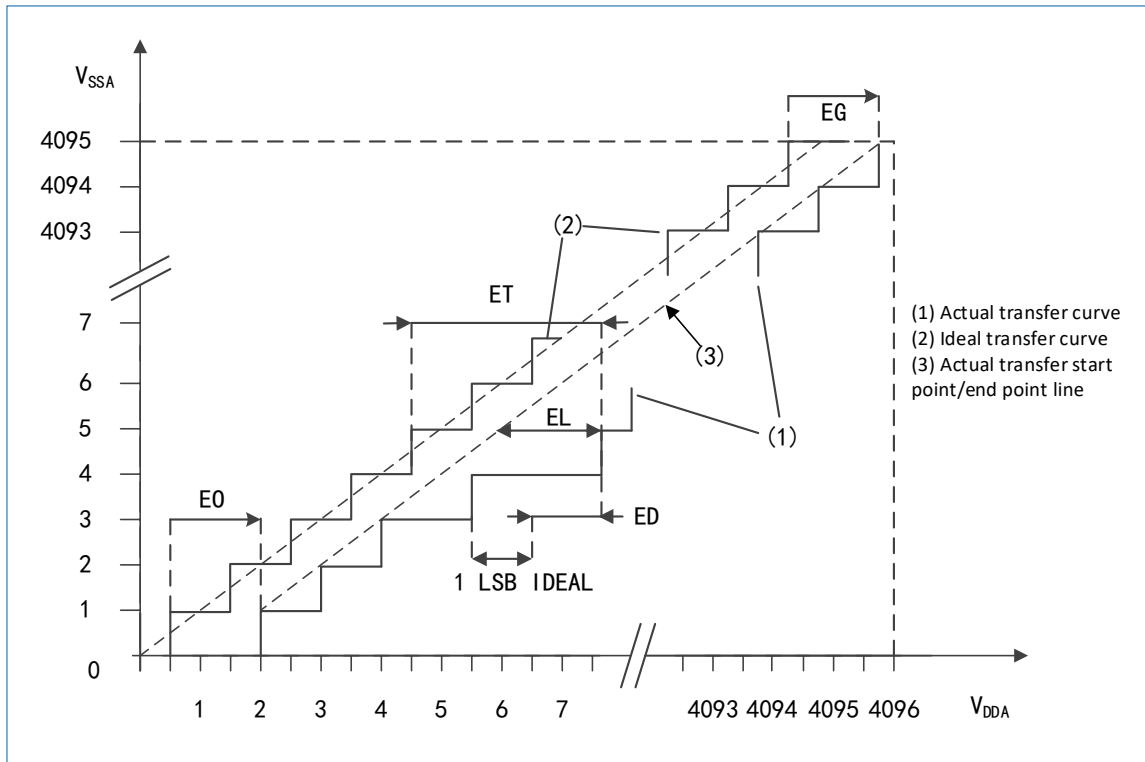


Figure 4-3 ADC accuracy characteristics

Note: For the explanations of EO, ET, EG, EL, and ED, see [Table 4-23](#).

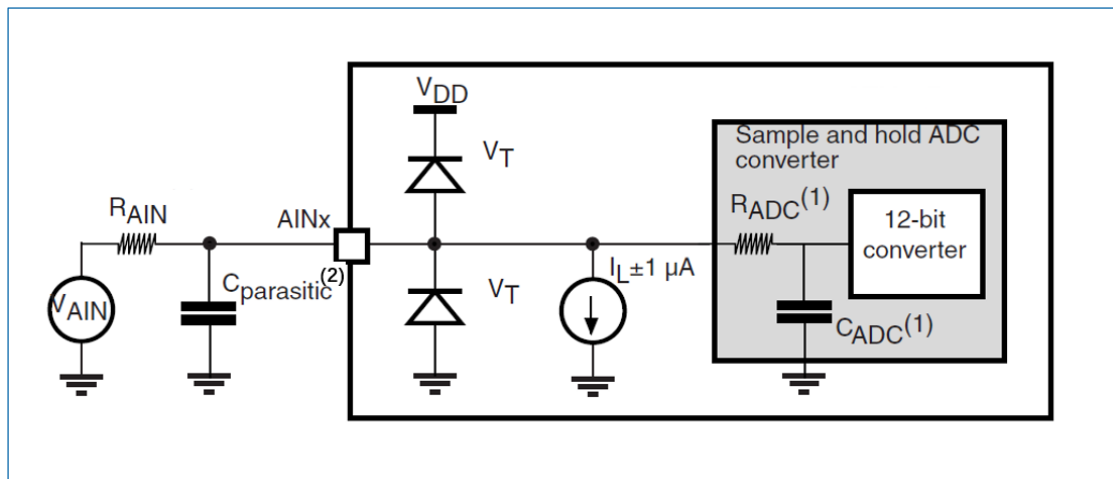


Figure 4-4 Typical connection diagram of ADC

- (1). For the ADC characteristics of  $R_{ADC}$  and  $C_{ADC}$ , see [Table 4-21](#).
- (2).  $C_{parasitic}$  equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high  $C_{parasitic}$  value would reduce conversion accuracy, so  $f_{ADC}$  should be reduced.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following section "5 Typical circuitry". To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

## 4.2.17 Temperature sensor characteristics

Table 4-24 Temperature sensor characteristics

| Symbol    | Parameter                          | Condition            | Min  | Typ     | Max     | Unit                   |
|-----------|------------------------------------|----------------------|------|---------|---------|------------------------|
| $T_L$     | Temperature sensor linearity error | -                    | -    | $\pm 1$ | $\pm 3$ | $^{\circ}\text{C}$     |
| $V_{25}$  | Output voltage                     | $25^{\circ}\text{C}$ | 0.85 | 0.89    | 0.93    | V                      |
| Avg_Slope | Temperature sensor slope           | -                    | -    | 3       | -       | mV/ $^{\circ}\text{C}$ |

### 5 Typical circuitry

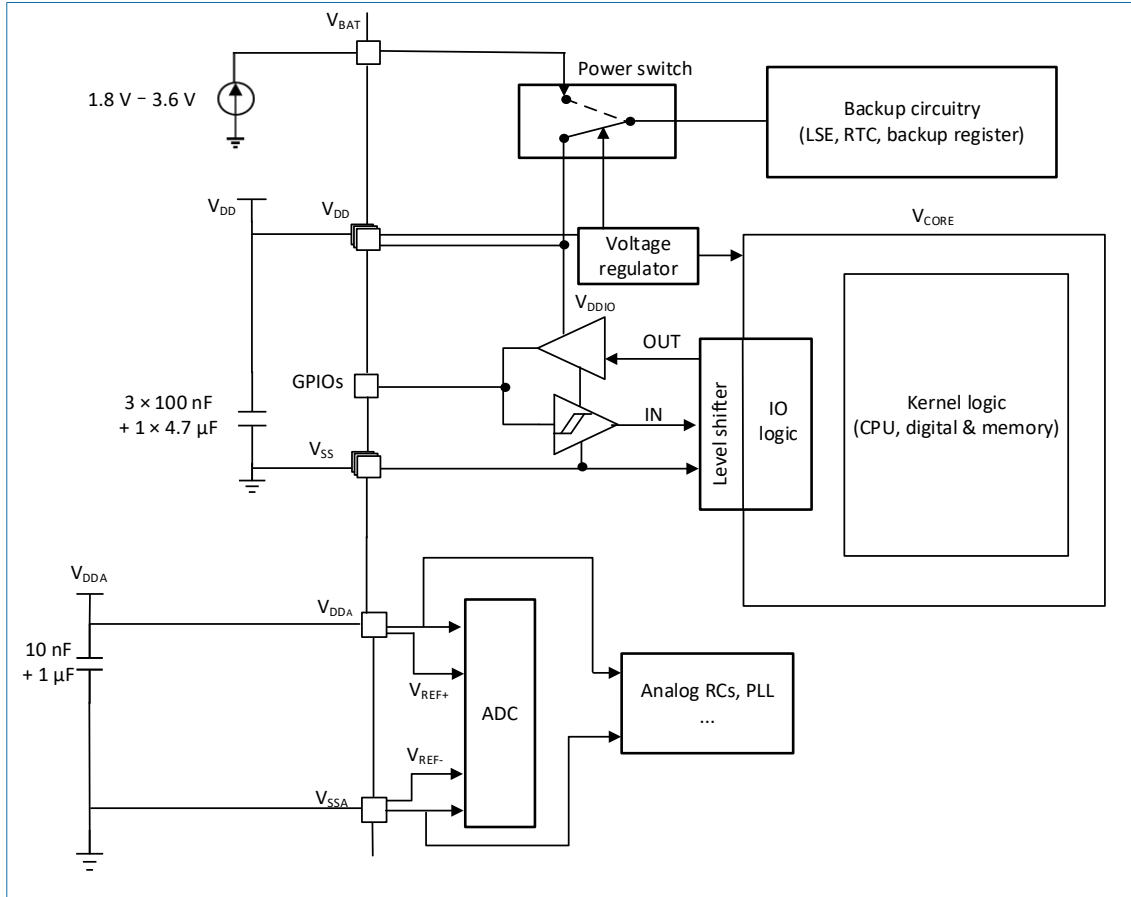


Figure 5-1 Power supply reference circuitry

## 6 Pinouts and pin descriptions

HK32ASAFE010xB MCUs are delivered in TSSOP20, QFN28, QFN32, LQFP32, LQFP48, and LQFP64 packages. The pinouts of the packages are as follows:

### 6.1 TSSOP20

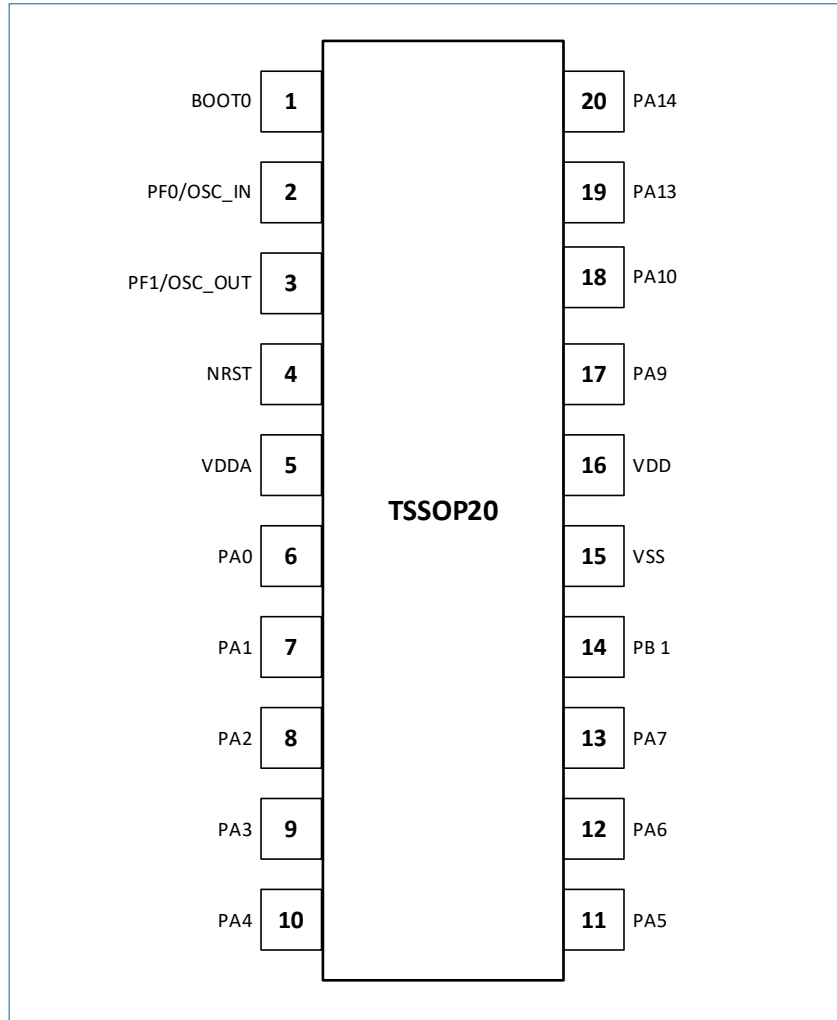


Figure 6-1 TSSOP20 pinout

## 6.2 QFN28

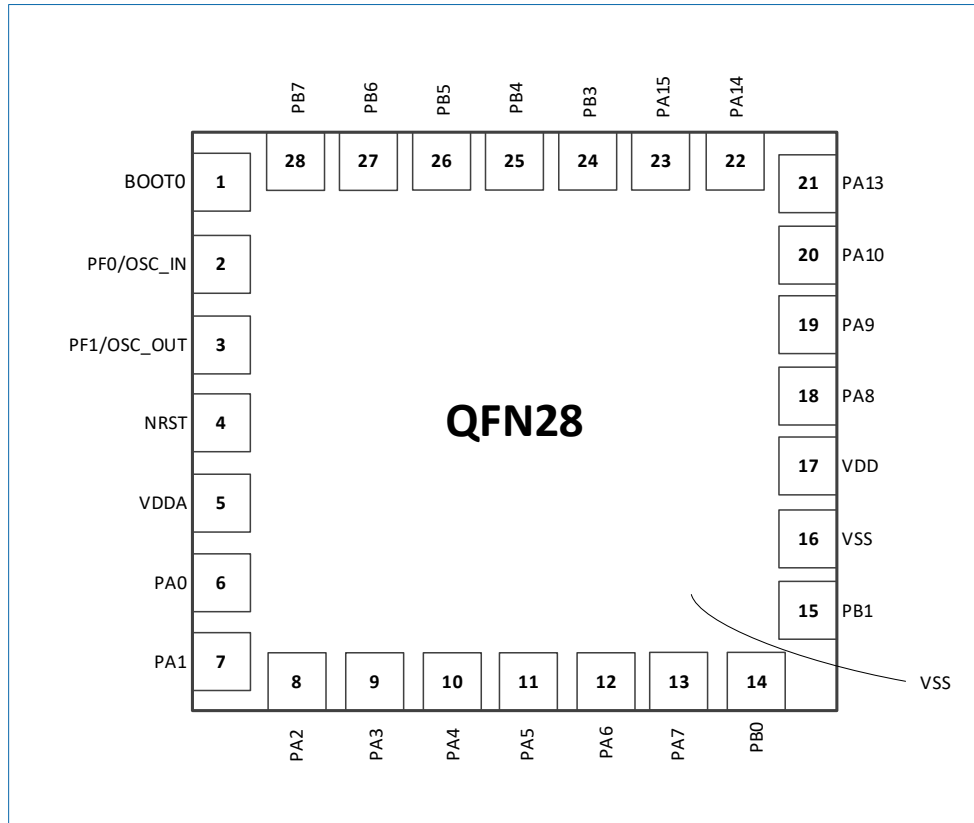


Figure 6-2 QFN28 pinout

## 6.3 QFN32

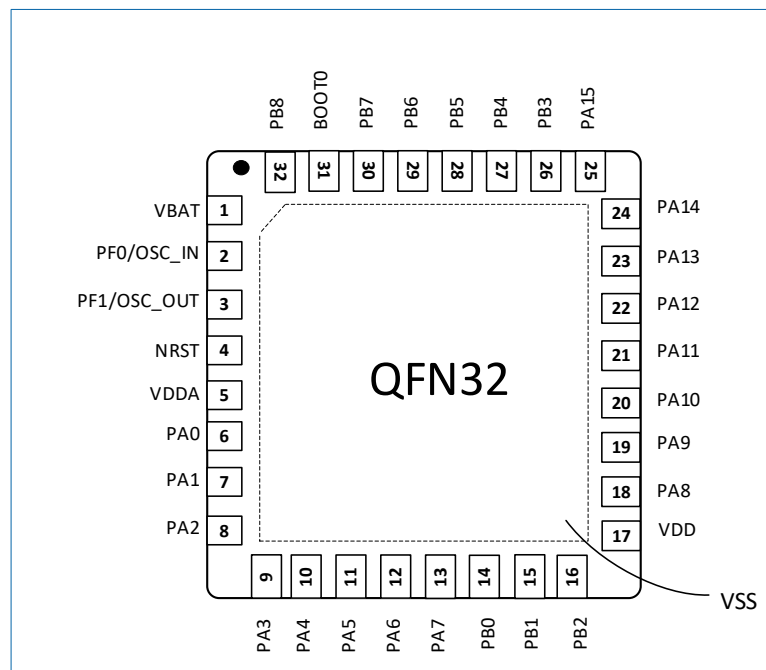


Figure 6-3 QFN32 pinout

## 6.4 LQFP32

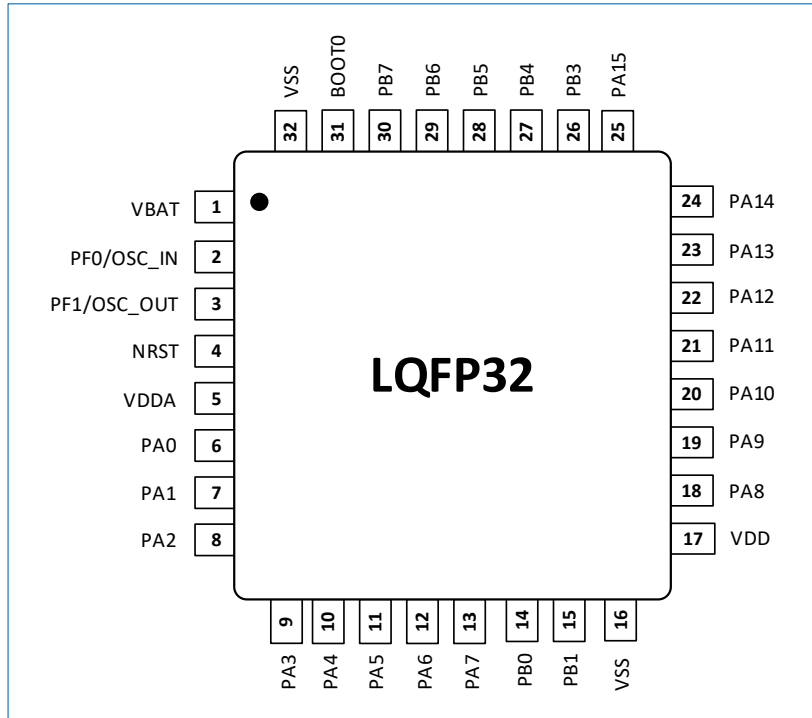


Figure 6-4 LQFP32 pinout

## 6.5 LQFP48

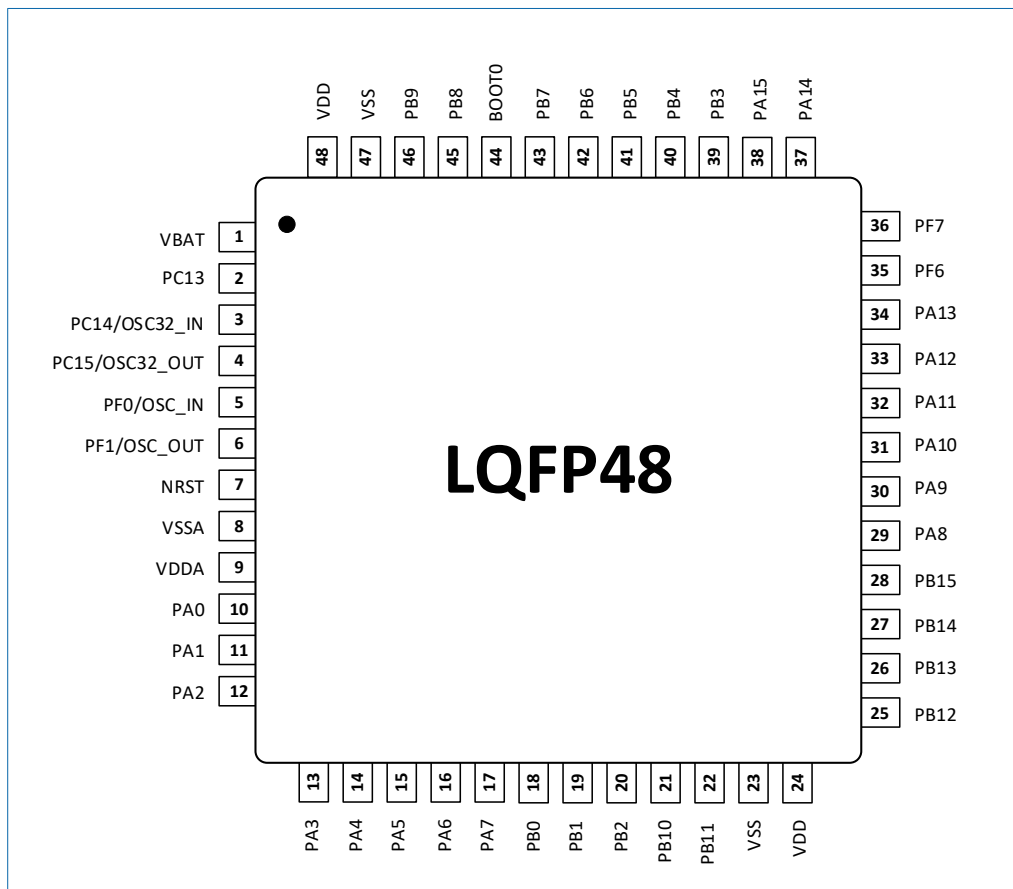


Figure 6-5 LQFP48 pinout



## 6.6 LQFP64

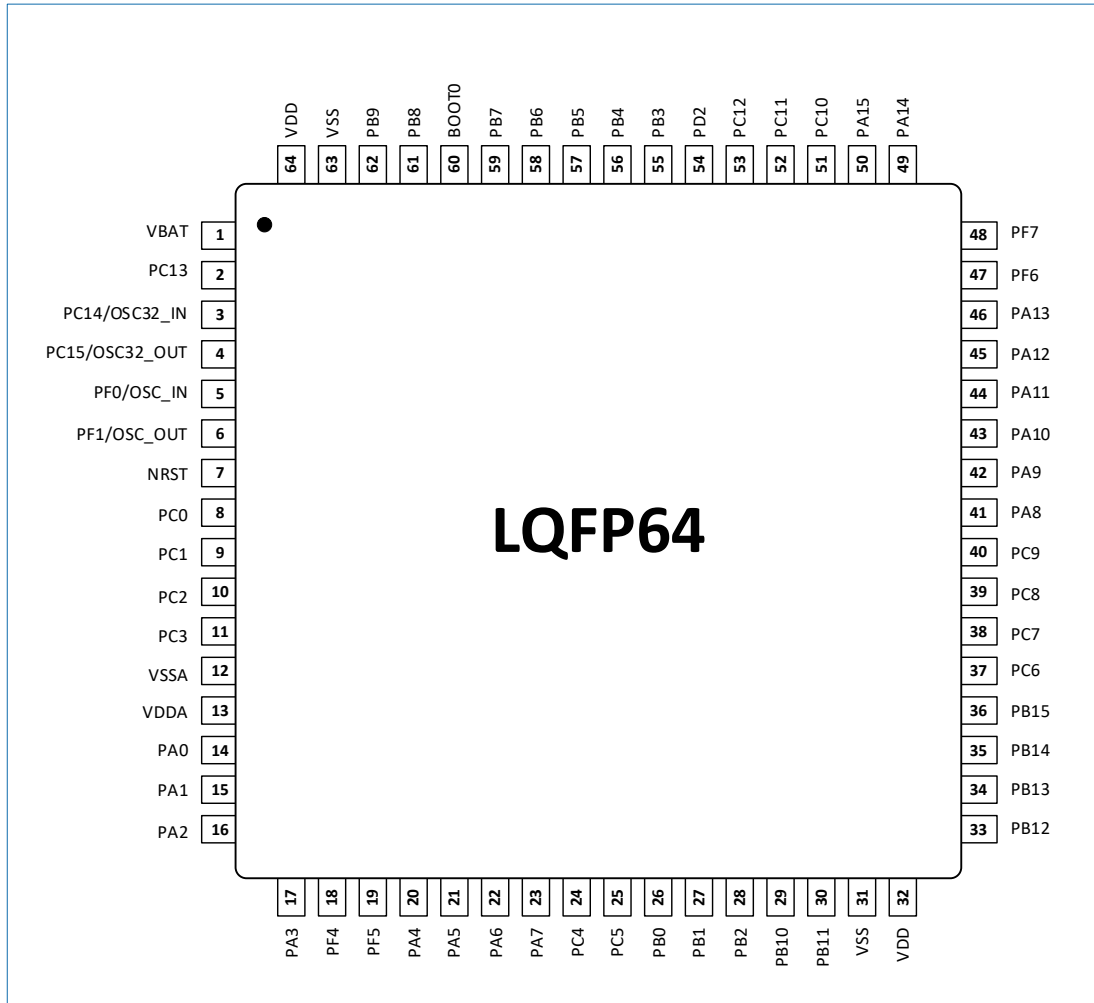


Figure 6-6 LQFP64 pinout

## 6.7 Pin descriptions

Table 6-1 Pin description of each package

| TSSOP20 | QFN28 | QFN32 | LQFP32 | LQFP48 | LQFP64 | Pin Name | Pin Type <sup>(1)</sup> | 5 V-tolerant | Alternate Function                            | Additional Function                               |
|---------|-------|-------|--------|--------|--------|----------|-------------------------|--------------|---|---|
| -       | -     | -     | -      | 1      | 1      | VBAT     | S                       |              | Battery power supply input                    |   |
| -       | -     | -     | -      | 2      | 2      | PC13     | I/O                     | FT           | -   | RTC_TAMP1<br>RTC_TS<br>RTC_OUT<br>WKUP2<br>EXTI13 |
| -       | -     | -     | -      | 3      | 3      | PC14     | I/O                     | FT           | -   | OSC32_IN<br>EXTI14                                |
| -       | -     | -     | -      | 4      | 4      | PC15     | I/O                     | FT           | -   | OSC32_OUT<br>EXTI15                               |
| 2       | 2     | 2     | 2      | 5      | 5      | PF0      | I/O                     | FT           | I2C1_SDA                                      | OSC_IN  |
| 3       | 3     | 3     | 3      | 6      | 6      | PF1      | I/O                     | FT           | I2C1_SCL                                      | OSC_OUT   |
| 4       | 4     | 4     | 4      | 7      | 7      | NRST     | I/O                     | -            | Reset input/internal reset output, active low |   |
| -       | -     | -     | -      | -      | 8      | PC0      | I/O                     | -            | LPTIM_IN1                                     | ADC_IN10<br>EXTI0                                 |
| -       | -     | -     | -      | -      | 9      | PC1      | I/O                     | -            | LPTIM_OUT                                     | ADC_IN11<br>EXTI1                                 |
| -       | -     | -     | -      | -      | 10     | PC2      | I/O                     | -            | SPI2_MISO<br>I2S2_MCK<br>LPTIM_IN2            | ADC_IN12<br>EXTI2                                 |

| TSSOP20 | QFN28 | QFN32 | LQFP32 | LQFP48 | LQFP64 | Pin Name | Pin Type <sup>(1)</sup> | 5 V-tolerant | Alternate Function   | Additional Function                               |
|---------|-------|-------|--------|--------|--------|----------|-------------------------|--------------|--|---|
| -       | -     | -     | -      | -      | 11     | PC3      | I/O                     | -            | SPI2_MOSI<br>I2S2_SD<br>LPTIM_ETR  | ADC_IN13<br>EXTI3                                 |
| -       | -     | -     | -      | 8      | 12     | VSSA     | S                       | -            | Analog ground  |   |
| 5       | 5     | 5     | 5      | 9      | 13     | VDDA     | S                       | -            | Analog power supply  |   |
| 6       | 6     | 6     | 6      | 10     | 14     | PA0      | I/O                     | -            | USART1_CTS<br>USART2_CTS<br>TIM2_CH1<br>TIM2_ETR<br>CMP1_ININ1/CMP1_OUT<br>LPUART_RX<br>LPTIM_IN1                | ADC_IN0<br>WKUP1<br>RTC_TAMP2<br>EXTCLK4<br>EXTI0 |
| 7       | 7     | 7     | 7      | 11     | 15     | PA1      | I/O                     | -            | USART1_RTS/USART1_DE<br>USART2_RTS/USART2_DE<br>TIM15_CH1N<br>TIM2_CH2<br>CMP1_INP1<br>LPTIM_IN2                 | ADC_IN1<br>EXTI1                                  |
| 8       | 8     | 8     | 8      | 12     | 16     | PA2      | I/O                     | -            | USART1_TX<br>USART2_TX<br>TIM15_CH1<br>TIM2_CH3<br>CMP2_INN1<br>CMP2_OUT<br>LPTIM_ETR                            | ADC_IN2<br>EXTI2                                  |
| 9       | 9     | 9     | 9      | 13     | 17     | PA3      | I/O                     | -            | USART1_RX<br>USART2_RX<br>TIM15_CH2<br>TIM2_CH4<br>CMP2_INP1<br>LPTIM_OUT  | ADC_IN3<br>EXTI3                                  |
| -       | -     | -     | -      | -      | 18     | PF4      | I/O                     | -            | -  | ADC_AIN17<br>EXTI4                                |
| -       | -     | -     | -      | -      | 19     | PF5      | I/O                     | FT           | -  | EXTI5   |
| 10      | 10    | 10    | 10     | 14     | 20     | PA4      | I/O                     | -            | SPI1_NSS<br>I2S1_WS<br>USART1_CK<br>USART2_CK<br>TIM14_CH1<br>CMP1_INN2<br>CMP2_INN2<br>CMP3_INN2<br>DAC1_AOOUT0 | ADC_IN4<br>EXTCLK1<br>EXTI4                       |
| 11      | 11    | 11    | 11     | 15     | 21     | PA5      | I/O                     | -            | SPI1_SCK<br>I2S1_CK<br>TIM2_CH1<br>TIM2_ETR<br>CMP1_INN3<br>CMP2_INN3<br>CMP3_INN1                               | ADC_IN5<br>EXTI5                                  |
| 12      | 12    | 12    | 12     | 16     | 22     | PA6      | I/O                     | -            | SPI1_MISO<br>I2S1_MCK<br>TIM3_CH1<br>TIM1_BKIN<br>TIM16_CH1<br>CMP1_OUT<br>LPUART_CTS<br>CAN_RX                  | ADC_IN6<br>EXTI6                                  |
| 13      | 13    | 13    | 13     | 17     | 23     | PA7      | I/O                     | -            | SPI1_MOSI<br>I2S1_SD<br>TIM3_CH2<br>TIM14_CH1  | ADC_IN7<br>EXTI7                                  |

| TSSOP20 | QFN28 | QFN32 | LQFP32 | LQFP48 | LQFP64 | Pin Name | Pin Type <sup>(1)</sup> | 5 V-tolerant | Alternate Function   | Additional Function |
|---------|-------|-------|--------|--------|--------|----------|-------------------------|--------------|--|---------------------|
|         |       |       |        |        |        |          |                         |              | TIM1_CH1N<br>TIM17_CH1<br>RCC_MCO<br>CMP2_OUT<br>CAN_TX  |                     |
| -       | -     | -     | -      | -      | 24     | PC4      | I/O                     | -            | LPUART_TX  | ADC_IN14<br>EXTI4   |
| -       | -     | -     | -      | -      | 25     | PC5      | I/O                     | -            | LPUART_RX  | ADC_IN15<br>EXTI5   |
| -       | 14    | 14    | 14     | 18     | 26     | PB0      | I/O                     | -            | TIM3_CH3<br>TIM1_CH2N<br>CMP3_INN3   | ADC_IN8<br>EXTI0    |
| 14      | 15    | 15    | 15     | 19     | 27     | PB1      | I/O                     | -            | TIM3_CH4<br>TIM14_CH1<br>TIM1_CH3N<br>CMP3_INN1/CMP3_OUT<br>LPUART_RTS/LPUART_DE                             | ADC_IN9<br>EXTI1    |
| -       | -     | 16    | -      | 20     | 28     | PB2      | I/O                     | FT           | I2C1_SMBA<br>I2C2_SMBA<br>LPTIM_OUT  | EXTI2               |
| -       | -     | -     | -      | 21     | 29     | PB10     | I/O                     | FT           | I2C1_SCL<br>I2C2_SCL<br>SPI2_SCK<br>I2S2_CK<br>TIM2_CH3<br>LPUART_TX   | EXTI10              |
| -       | -     | -     | -      | 22     | 30     | PB11     | I/O                     | FT           | I2C1_SDA<br>I2C2_SDA<br>TIM2_CH4<br>LPUART_RX  | EXTI11              |
| 15      | 16    | -     | 16     | 23     | 31     | VSS      | I/O                     | -            | Ground   |                     |
| 16      | 17    | 17    | 17     | 24     | 32     | VDD      | I/O                     | -            | Digital power supply   |                     |
| -       | -     | -     | -      | 25     | 33     | PB12     | I/O                     | FT           | SPI1_NSS<br>I2S1_WS<br>SPI2_NSS<br>I2S2_WS<br>TIM1_BKIN<br>TIM15_BKIN<br>I2C2_SMBA<br>LPUART_RTS/LPUART_DE   | EXTI12              |
| -       | -     | -     | -      | 26     | 34     | PB13     | I/O                     | FT           | SPI1_SCK<br>I2S1_CK<br>SPI2_SCK<br>I2S2_CK<br>TIM1_CH1N<br>I2C2_SCL<br>LPUART_CTS                            | EXTI13              |
| -       | -     | -     | -      | 27     | 35     | PB14     | I/O                     | FT           | SPI1_MISO<br>I2S1_MCK<br>SPI2_MISO<br>I2S2_MCK<br>TIM1_CH2N<br>TIM15_CH1<br>I2C2_SDA<br>LPUART_RTS/LPUART_DE | EXTI14              |
| -       | -     | -     | -      | 28     | 36     | PB15     | I/O                     | FT           | SPI1_MOSI<br>I2S1_SD<br>SPI2_MOSI<br>I2S2_SD<br>TIM1_CH3N<br>TIM15_CH1N<br>TIM15_CH2                         | EXTI15<br>RTC_REFIN |

| TSSOP20 | QFN28 | QFN32 | LQFP32 | LQFP48 | LQFP64 | Pin Name | Pin Type <sup>(1)</sup> | 5 V-tolerant | Alternate Function  | Additional Function |
|---------|-------|-------|--------|--------|--------|----------|-------------------------|--------------|---|---------------------|
| -       | -     | -     | -      | -      | 37     | PC6      | I/O                     | FT           | TIM3_CH1<br>LPTIM_IN1   | EXTI6               |
| -       | -     | -     | -      | -      | 38     | PC7      | I/O                     | FT           | TIM3_CH2<br>LPTIM_OUT   | EXTI7               |
| -       | -     | -     | -      | -      | 39     | PC8      | I/O                     | FT           | TIM3_CH3<br>LPTIM_IN2   | EXTI8               |
| -       | -     | -     | -      | -      | 40     | PC9      | I/O                     | FT           | TIM3_CH4<br>LPTIM_ETR   | EXTI9               |
| -       | 18    | 18    | 18     | 29     | 41     | PA8      | I/O                     | FT           | USART1_CK<br>TIM1_CH1<br>RCC_MCO<br>LPUART_RX                                     | WKUP3<br>EXTI8      |
| 17      | 19    | 19    | 19     | 30     | 42     | PA9      | I/O                     | FT           | USART1_TX<br>TIM1_CH2<br>TIM15_BKIN<br>I2C1_SCL<br>RCC_MCO<br>LPUART_TX<br>CAN_RX | EXTI9               |
| 18      | 20    | 20    | 20     | 31     | 43     | PA10     | I/O                     | FT           | USART1_RX<br>TIM1_CH3<br>TIM17_BKIN<br>I2C1_SDA<br>LPUART_RX<br>CAN_TX            | EXTI10              |
| -       | -     | 21    | 21     | 32     | 44     | PA11     | I/O                     | -            | USART1_CTS<br>TIM1_CH4<br>I2C2_SCL<br>CAN_RX<br>CMP1_OUT                          | EXTI11              |
| -       | -     | 22    | 22     | 33     | 45     | PA12     | I/O                     | -            | USART1_RTS/USART1_DE<br>TIM1_ETR<br>I2C2_SDA<br>CAN_TX<br>CMP2_OUT                | EXTI12              |
| 19      | 21    | 23    | 23     | 34     | 46     | PA13     | I/O                     | FT           | IRTIM_IROUT<br>SWDIO<br>CAN_RX<br>LPUART_RX<br>CMP3_OUT                           | EXTCLK2<br>EXTI13   |
| -       | -     | -     | -      | 35     | 47     | PF6      | I/O                     | FT           | I2C1_SCL<br>I2C2_SCL  | EXTI6               |
| -       | -     | -     | -      | 36     | 48     | PF7      | I/O                     | FT           | I2C1_SDA<br>I2C2_SDA  | EXTI7               |
| 20      | 22    | 24    | 24     | 37     | 49     | PA14     | I/O                     | FT           | USART1_TX<br>USART2_TX<br>SWCLK<br>CAN_TX<br>LPUART_TX                            | EXTCLK3<br>EXTI14   |
| -       | 23    | 25    | 25     | 38     | 50     | PA15     | I/O                     | FT           | SPI1_NSS<br>I2S1_WS<br>USART1_RX<br>USART2_RX<br>TIM2_CH1<br>TIM2_ETR             | EXTI15              |
| -       | -     | -     | -      | -      | 51     | PC10     | I/O                     | FT           | LPUART_TX<br>LPTIM_IN1  | EXTI10              |
| -       | -     | -     | -      | -      | 52     | PC11     | I/O                     | FT           | CAN_RX<br>LPUART_RX<br>LPTIM_OUT  | EXTI11              |
| -       | -     | -     | -      | -      | 53     | PC12     | I/O                     | FT           | CAN_TX<br>LPTIM_IN2   | EXTI12              |

| TSSOP20 | QFN28            | QFN32            | LQFP32 | LQFP48 | LQFP64 | Pin Name             | Pin Type <sup>(1)</sup> | 5 V-tolerant | Alternate Function   | Additional Function |
|---------|------------------|------------------|--------|--------|--------|----------------------|-------------------------|--------------|--|---------------------|
| -       | -                | -                | -      | -      | 54     | PD2                  | I/O                     | FT           | TIM3_ETR<br>LPUART_DE/LPUART_RTS<br>LPTIM_ETR                            | EXTI2               |
| -       | 24               | 26               | 26     | 39     | 55     | PB3                  | I/O                     | FT           | SPI1_SCK<br>I2S1_CK<br>TIM2_CH2<br>CMP3_OUT                              | EXTI3               |
| -       | 25               | 27               | 27     | 40     | 56     | PB4                  | I/O                     | FT           | SPI1_MISO<br>I2S1_MCK<br>TIM3_CH1<br>TIM17_BKIN                          | EXTI4               |
| -       | 26               | 28               | 28     | 41     | 57     | PB5                  | I/O                     | FT           | SPI1_MOSI<br>I2S1_SD<br>I2C1_SMBA<br>TIM16_BKIN<br>TIM3_CH2<br>LPTIM_IN1 | EXTI5               |
| -       | 27               | 29               | 29     | 42     | 58     | PB6                  | I/O                     | FT           | I2C1_SCL<br>USART1_TX<br>TIM16_CH1N<br>LPUART_TX<br>LPTIM_ETR            | EXTI6               |
| -       | 28               | 30               | 30     | 43     | 59     | PB7                  | I/O                     | FT           | I2C1_SDA<br>USART1_RX<br>TIM17_CH1N<br>LPUART_RX<br>LPTIM_IN2            | EXTI7               |
| 1       | 1                | 31               | 31     | 44     | 60     | Boot0 <sup>(2)</sup> | I                       |              | Boot mode configuration  |                     |
| -       | -                | 32               | -      | 45     | 61     | PB8                  | I/O                     | FT           | I2C1_SCL<br>TIM16_CH1<br>CAN_RX  | EXTI8               |
| -       | -                | -                | -      | 46     | 62     | PB9                  | I/O                     | FT           | I2C1_SDA<br>IRTIM_IROUT<br>TIM17_CH1<br>SPI2_NSS<br>I2S2_WS<br>CAN_TX    | EXTI9               |
| -       | 0 <sup>(3)</sup> | 0 <sup>(3)</sup> | 32     | 47     | 63     | VSS                  | S                       |              | Ground   |                     |
| -       | -                | 1                | 1      | 48     | 64     | VDD                  | S                       |              | Digital power supply   |                     |

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). By default, the Boot0 pin has a 50 kΩ pull-down resistor.

(3). In the QFN package, pin 0 is the thermal pad on the package bottom.

#### Note:

- Unless otherwise specified, all I/Os are configured in input floating mode during and after resets.
- For details about alternate functions, see section "[6.8 Alternate function table](#)".

## 6.8 Alternate function table

Table 6-2 Alternate function table

| Pin      | AF0                    | AF1                      | AF2                     | AF3                      | AF4       | AF5                     | AF6       | AF7       | AF8 | AF9 to AF13 | AF14   | AF15      |
|----------|------------------------|--------------------------|-------------------------|--------------------------|-----------|-------------------------|-----------|-----------|-----|-------------|--------|-----------|
| PA0/AIN0 | -                      | USART1_CTS               | TIM2_CH1/<br>TIM2_ETRIN | USART2_CTS               | -         | LPUART_RX/<br>LPUART_TX | LPTIM_IN1 | COMP1_OUT | -   |             | -      | -         |
| PA1/AIN1 | -                      | USART1_RTS/<br>USART1_DE | TIM2_CH2                | USART2_RTS/<br>USART2_DE | -         | TIM15_CH1N              | LPTIM_IN2 | -         | -   |             | -      | -         |
| PA2/AIN2 | TIM15_CH1              | USART1_TX/<br>USART1_RX  | TIM2_CH3                | USART2_TX/<br>USART2_RX  | -         | -                       | LPTIM_ETR | COMP2_OUT | -   |             | -      | -         |
| PA3/AIN3 | TIM15_CH2              | USART1_RX/<br>USART1_TX  | TIM2_CH4                | USART2_RX/<br>USART2_TX  | -         | -                       | LPTIM_OUT | -         | -   |             | -      | -         |
| PA4/AIN4 | SPI1_NSS/<br>I2S1_WS   | USART1_CK                | -                       | USART2_CK                | TIM14_CH1 | -                       | -         | -         | -   |             | -      | -         |
| PA5/AIN5 | SPI1_SCK/<br>I2S1_CK   | -                        | TIM2_CH1/<br>TIM2_ETRIN | -                        | -         | -                       | -         | -         | -   |             | -      | -         |
| PA6/AIN6 | SPI1_MISO/<br>I2S1_MCK | TIM3_CH1                 | TIM1_BKIN               | LPUART_CTS               | -         | TIM16_CH1               | -         | COMP1_OUT | -   |             | CAN_RX | -         |
| PA7/AIN7 | SPI1_MOSI/<br>I2S1_SD  | TIM3_CH2                 | TIM1_CH1N               | -                        | TIM14_CH1 | TIM17_CH1               | -         | COMP2_OUT | -   |             | CAN_TX | RCC_MCO   |
| PA8      | RCC_MCO                | USART1_CK                | TIM1_CH1                | -                        | -         | LPUART_RX/<br>LPUART_TX | -         | -         | -   |             | -      | -         |
| PA9      | TIM15_BKIN             | USART1_TX/<br>USART1_RX  | TIM1_CH2                | LPUART_TX/<br>LPUART_RX  | I2C1_SCL  | RCC_MCO                 | -         | -         | -   |             | CAN_RX | -         |
| PA10     | TIM17_BKIN             | USART1_RX/<br>USART1_TX  | TIM1_CH3                | LPUART_RX/<br>LPUART_TX  | I2C1_SDA  | -                       | -         | -         | -   |             | CAN_TX | -         |
| PA11     | -                      | USART1_CTS               | TIM1_CH4                | -                        | -         | I2C2_SCL                | -         | COMP1_OUT | -   |             | CAN_RX | -         |
| PA12     | -                      | USART1_RTS/<br>USART1_DE | TIM1_ETR                | -                        | -         | I2C2_SDA                | -         | COMP2_OUT | -   |             | CAN_TX | -         |
| PA13     | CM0_SWD                | IRTIM_IROUT              | -                       | LPUART_RX/<br>LPUART_TX  | -         | -                       | -         | COMP3_OUT | -   |             | CAN_RX | -         |
| PA14     | CM0_SWCLK              | USART1_TX/<br>USART1_RX  | -                       | LPUART_TX/<br>LPUART_RX  | -         | USART2_TX/<br>USART2_RX | -         | -         | -   |             | CAN_TX | -         |
| PA15     | SPI1_NSS/<br>I2S1_WS   | USART1_RX/<br>USART1_TX  | TIM2_CH1/<br>TIM2_ETRIN | -                        | -         | USART2_RX/<br>USART2_TX | -         | -         | -   |             | -      | -         |
| PB0/AIN8 | -                      | TIM3_CH3                 | TIM1_CH2N               | -                        | -         | -                       | -         | -         | -   |             | -      | -         |
| PB1/AIN9 | TIM14_CH1              | TIM3_CH4                 | TIM1_CH3N               | LPUART_RTS/<br>LPUART_DE | -         | -                       | -         | COMP3_OUT | -   |             | -      | -         |
| PB2      | -                      | -                        | -                       | -                        | I2C2_SMBA | -                       | LPTIM_OUT | -         | -   |             | -      | I2C1_SMBA |
| PB3      | SPI1_SCK/<br>I2S1_CK   | -                        | TIM2_CH2                | -                        | -         | -                       | -         | COMP3_OUT | -   |             | -      | -         |
| PB4      | SPI1_MISO/<br>I2S1_MCK | TIM3_CH1                 | -                       | -                        | -         | TIM17_BKIN              | -         | -         | -   |             | -      | -         |
| PB5      | SPI1_MOSI/<br>I2S1_SD  | TIM3_CH2                 | TIM16_BKIN              | I2C1_SMBA                | -         | -                       | LPTIM_IN1 | -         | -   |             | -      | -         |

| Pin       | AF0                     | AF1                   | AF2        | AF3                      | AF4 | AF5                  | AF6       | AF7 | AF8                    | AF9 to AF13 | AF14   | AF15      |
|-----------|-------------------------|-----------------------|------------|--------------------------|-----|----------------------|-----------|-----|------------------------|-------------|--------|-----------|
| PB6       | USART1_TX/<br>USART1_RX | I2C1_SCL              | TIM16_CH1N | LPUART_TX/<br>LPUART_RX  | -   | -                    | LPTIM_ETR | -   | -                      | -           | -      | -         |
| PB7       | USART1_RX/<br>USART1_TX | I2C1_SDA              | TIM17_CH1N | LPUART_RX/<br>LPUART_TX  | -   | -                    | LPTIM_IN2 | -   | -                      | -           | -      | -         |
| PB8       | -                       | I2C1_SCL              | TIM16_CH1  | -                        | -   | -                    | -         | -   | -                      | -           | CAN_RX | -         |
| PB9       | IRTIM_IROUT             | I2C1_SDA              | TIM17_CH1  | -                        | -   | SPI2_NSS/<br>I2S2_WS | -         | -   | -                      | -           | CAN_TX | -         |
| PB10      | -                       | I2C1_SCL              | TIM2_CH3   | LPUART_TX/<br>LPUART_RX  | -   | SPI2_SCK/<br>I2S2_CK | I2C2_SCL  | -   | -                      | -           | -      | -         |
| PB11      | -                       | I2C1_SDA              | TIM2_CH4   | LPUART_RX/<br>LPUART_TX  | -   | -                    | I2C2_SDA  | -   | -                      | -           | -      | -         |
| PB12      | SPI1_NSS/<br>I2S1_WS    | -                     | TIM1_BKIN  | LPUART_RTS/<br>LPUART_DE | -   | TIM15_BKIN           | -         | -   | SPI2_NSS/<br>I2S2_WS   | -           | -      | I2C2_SMBA |
| PB13      | SPI1_SCK/<br>I2S1_CK    | -                     | TIM1_CH1N  | LPUART_CTS               | -   | I2C2_SCL             | -         | -   | SPI2_SCK/<br>I2S2_CK   | -           | -      | -         |
| PB14      | SPI1_MISO/<br>I2C1_MCK  | TIM15_CH1             | TIM1_CH2N  | LPUART_RTS/<br>LPUART_DE | -   | I2C2_SDA             | -         | -   | SPI2_MISO/<br>I2S2_MCK | -           | -      | -         |
| PB15      | SPI1_MOSI/<br>I2S1_SD   | TIM15_CH2             | TIM1_CH3N  | TIM15_CH1N               | -   | -                    | -         | -   | SPI2_MOSI/<br>I2S2_SD  | -           | -      | -         |
| PC0/AIN10 | -                       | -                     | -          | -                        | -   | -                    | LPTIM_IN1 | -   | -                      | -           | -      | -         |
| PC1/AIN11 | -                       | -                     | -          | -                        | -   | -                    | LPTIM_OUT | -   | -                      | -           | -      | -         |
| PC2/AIN12 | -                       | SPI2_MISO/<br>I2S_MCK | -          | -                        | -   | -                    | LPTIM_IN2 | -   | -                      | -           | -      | -         |
| PC3/AIN13 | -                       | SPI2_MOSI/<br>I2S2_SD | -          | -                        | -   | -                    | LPTIM_ETR | -   | -                      | -           | -      | -         |
| PC4/AIN14 | -                       | -                     | -          | LPUART_T/<br>LPUART_RX   | -   | -                    | -         | -   | -                      | -           | -      | -         |
| PC5/AIN15 | -                       | -                     | -          | LPUART_RX/<br>LPUART_TX  | -   | -                    | -         | -   | -                      | -           | -      | -         |
| PC6       | TIM3_CH1                | -                     | -          | -                        | -   | -                    | LPTIM_IN1 | -   | -                      | -           | -      | -         |
| PC7       | TIM3_CH2                | -                     | -          | -                        | -   | -                    | LPTIM_OUT | -   | -                      | -           | -      | -         |
| PC8       | TIM3_CH3                | -                     | -          | -                        | -   | -                    | LPTIM_IN2 | -   | -                      | -           | -      | -         |
| PC9       | TIM3_CH4                | -                     | -          | -                        | -   | -                    | LPTIM_ETR | -   | -                      | -           | -      | -         |
| PC10      | -                       | -                     | -          | LPUART_TX/<br>LPUART_RX  | -   | -                    | LPTIM_IN1 | -   | -                      | -           | -      | -         |
| PC11      | -                       | -                     | -          | LPUART_RX/<br>LPUART_TX  | -   | -                    | LPTIM_OUT | -   | -                      | -           | CAN_RX | -         |
| PC12      | -                       | -                     | -          | -                        | -   | -                    | LPTIM_IN2 | -   | -                      | -           | CAN_TX | -         |
| PD2       | TIM3_ETR                | -                     | -          | LPUART_RTS/<br>LPUART_DE | -   | -                    | LPTIM_ETR | -   | -                      | -           | -      | -         |
| PF0       | -                       | I2C1_SDA              | -          | -                        | -   | -                    | -         | -   | -                      | -           | -      | -         |
| PF1       | -                       | I2C1_SCL              | -          | -                        | -   | -                    | -         | -   | -                      | -           | -      | -         |
| PF4       | -                       | -                     | -          | -                        | -   | -                    | -         | -   | -                      | -           | -      | -         |
| PF5       | -                       | -                     | -          | -                        | -   | -                    | -         | -   | -                      | -           | -      | -         |
| PF6       | -                       | I2C1_SCL              | -          | -                        | -   | -                    | I2C2_SCL  | -   | -                      | -           | -      | -         |
| PF7       | -                       | I2C1_SDA              | -          | -                        | -   | -                    | I2C2_SDA  | -   | -                      | -           | -      | -         |

## 7 Package characteristics

### 7.1 TSSOP20

TSSOP20 is a 6.5 mm × 6.5 mm, 0.65 mm pitch package.

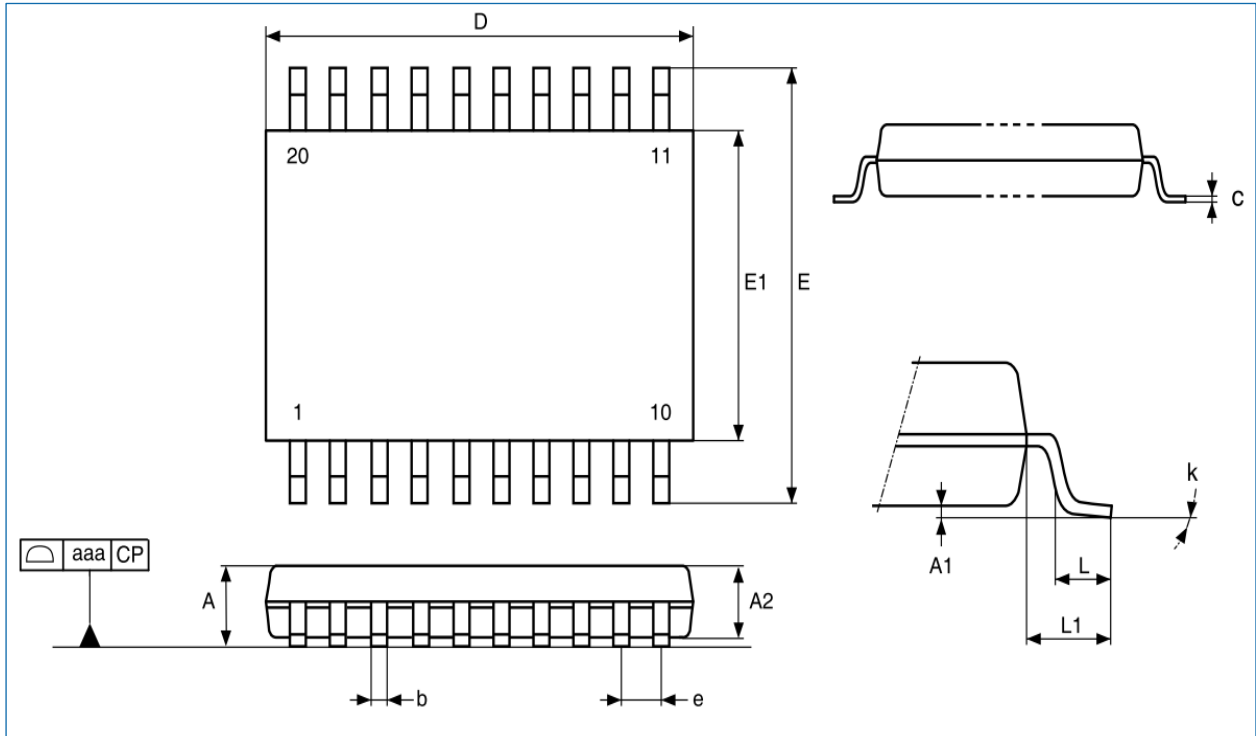


Figure 7-1 TSSOP20 package outline

Table 7-1 TSSOP20 package parameters

| Symbol | Min (mm) | Typ (mm) | Max (mm) | Min (inches) <sup>(1)</sup> | Typ (inches) <sup>(1)</sup> | Max (inches) <sup>(1)</sup> |
|--------|----------|----------|----------|-----------------------------|-----------------------------|-----------------------------|
| A      | -        | -        | 1.200    | -                           | -                           | 0.0472                      |
| A1     | 0.050    | -        | 0.150    | 0.0020                      | -                           | 0.0059                      |
| A2     | 0.800    | 1.000    | 1.050    | 0.0315                      | 0.0394                      | 0.0413                      |
| b      | 0.190    | -        | 0.300    | 0.0075                      | -                           | 0.0118                      |
| c      | 0.090    | -        | 0.200    | 0.0035                      | -                           | 0.0079                      |
| D      | 6.400    | 6.500    | 6.600    | 0.2520                      | 0.2559                      | 0.2598                      |
| E      | 6.200    | 6.400    | 6.600    | 0.2441                      | 0.2520                      | 0.2598                      |
| E1     | 4.300    | 4.400    | 4.500    | 0.1693                      | 0.1732                      | 0.1772                      |
| e      | -        | 0.650    | -        | -                           | 0.0256                      | -                           |
| L      | 0.450    | 0.600    | 0.750    | 0.0177                      | 0.0236                      | 0.0295                      |
| L1     | -        | 1.000    | -        | -                           | 0.0394                      | -                           |
| k      | 0°       | -        | 8.0°     | 0°                          | -                           | 8.0°                        |
| aaa    | -        | -        | 0.1000   | -                           | -                           | 0.0039                      |

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.



## 7.2 QNF28

QNF28 is a 4 mm × 4 mm, 0.4 mm pitch package.

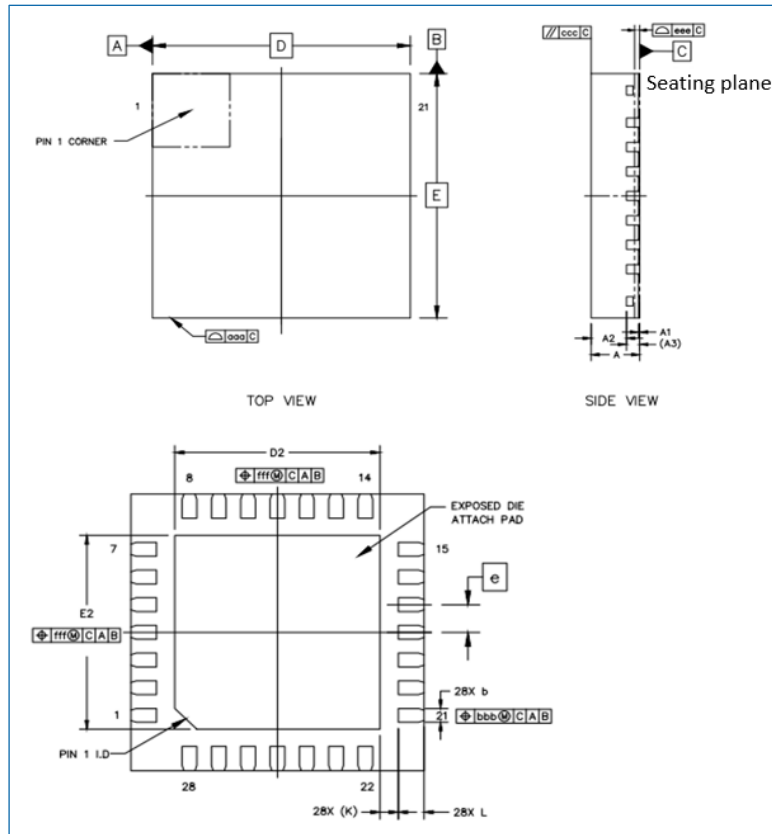


Figure 7-2 QNF28 package outline

Table 7-2 QNF28 package parameters

| Symbol | Min (mm)                 | Typ (mm) | Max (mm) |
|--------|--------------------------|----------|----------|
| A      | 0.7                      | 0.75     | 0.8      |
| A1     | 0                        | 0.02     | 0.05     |
| A2     | -                        | 0.55     | -        |
| A3     | 0.203 REF <sup>(1)</sup> |          |          |
| b      | 0.15                     | 0.20     | 0.25     |
| D      | 4 BSC <sup>(2)</sup>     |          |          |
| E      | 4 BSC                    |          |          |
| e      | 0.4 BSC                  |          |          |
| D2     | 2.7                      | 2.9      | 2.9      |
| E2     | 2.7                      | 2.9      | 2.9      |
| L      | 0.3                      | 0.35     | 0.4      |
| K      | 0.25 REF                 |          |          |
| aaa    | 0.1                      |          |          |
| ccc    | 0.1                      |          |          |
| eee    | 0.08                     |          |          |
| bbb    | 0.1                      |          |          |
| fff    | 0.1                      |          |          |

(1). REF indicates a reference value.

(2). BSC: basic spacing between centers.

### 7.3 QFN32

QFN32 is a 5 mm × 5 mm, 0.5 mm pitch package.

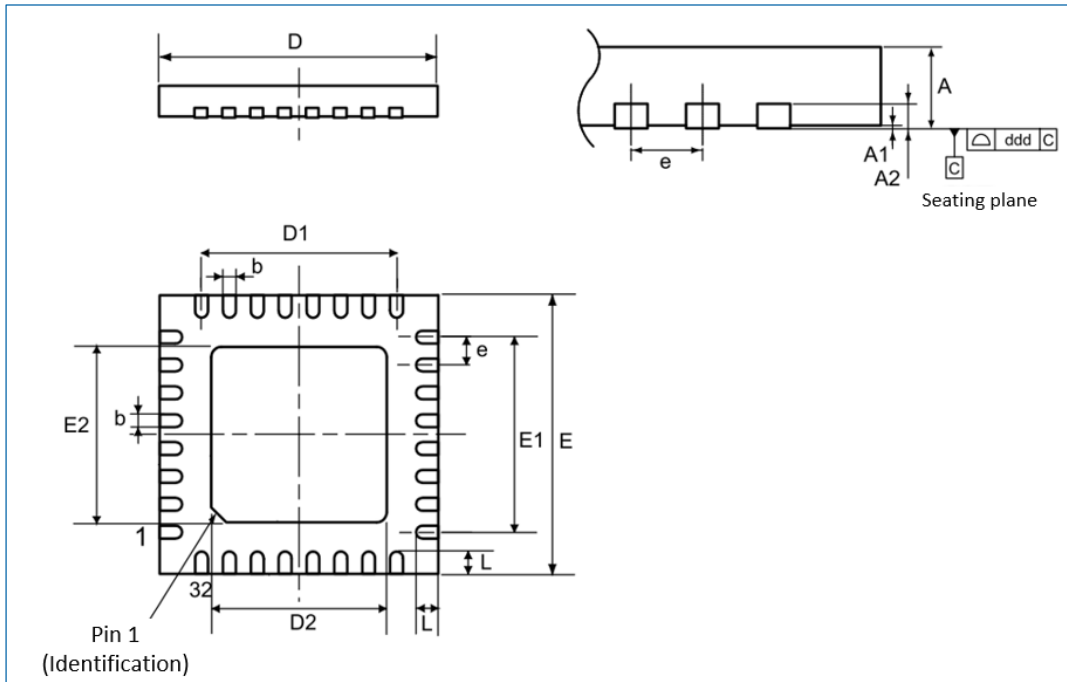


Figure 7-3 QFN32 package outline

Table 7-3 QFN32 package parameters

| Symbol | Min (mm) | Typ (mm) | Max (mm) | Min (inches) <sup>(1)</sup> | Typ (inches) <sup>(1)</sup> | Max (inches) <sup>(1)</sup> |
|--------|----------|----------|----------|-----------------------------|-----------------------------|-----------------------------|
| A      | 0.500    | 0.550    | 0.600    | 0.0197                      | 0.0217                      | 0.0236                      |
| A1     | 0.500    | 0.550    | 0.600    | 0.0197                      | 0.0217                      | 0.0236                      |
| A2     | 0.000    | 0.020    | 0.050    | 0.0000                      | 0.0008                      | 0.0020                      |
| A3     | -        | 0.152    | -        | -                           | 0.0060                      | -                           |
| b      | 0.180    | 0.230    | 0.280    | 0.0071                      | 0.0091                      | 0.0110                      |
| D      | 4.900    | 5.000    | 5.100    | 0.1929                      | 0.1969                      | 0.2008                      |
| D1     | 3.400    | 3.500    | 3.600    | 0.1339                      | 0.1378                      | 0.1417                      |
| D2     | 3.400    | 3.500    | 3.600    | 0.1339                      | 0.1378                      | 0.1417                      |
| E      | 4.900    | 5.000    | 5.100    | 0.1929                      | 0.1969                      | 0.2008                      |
| E1     | 3.400    | 3.500    | 3.600    | 0.1339                      | 0.1378                      | 0.1417                      |
| E2     | 3.400    | 3.500    | 3.600    | 0.1339                      | 0.1378                      | 0.1417                      |
| e      | -        | 0.500    | -        | -                           | 0.0197                      | -                           |
| L      | 0.300    | 0.400    | 0.500    | 0.0118                      | 0.0157                      | 0.0197                      |
| ddd    | -        | -        | 0.080    | -                           | -                           | 0.0031                      |

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

## 7.4 LQFP32

LQFP32 is a 7 mm × 7 mm, 0.8 mm pitch package.

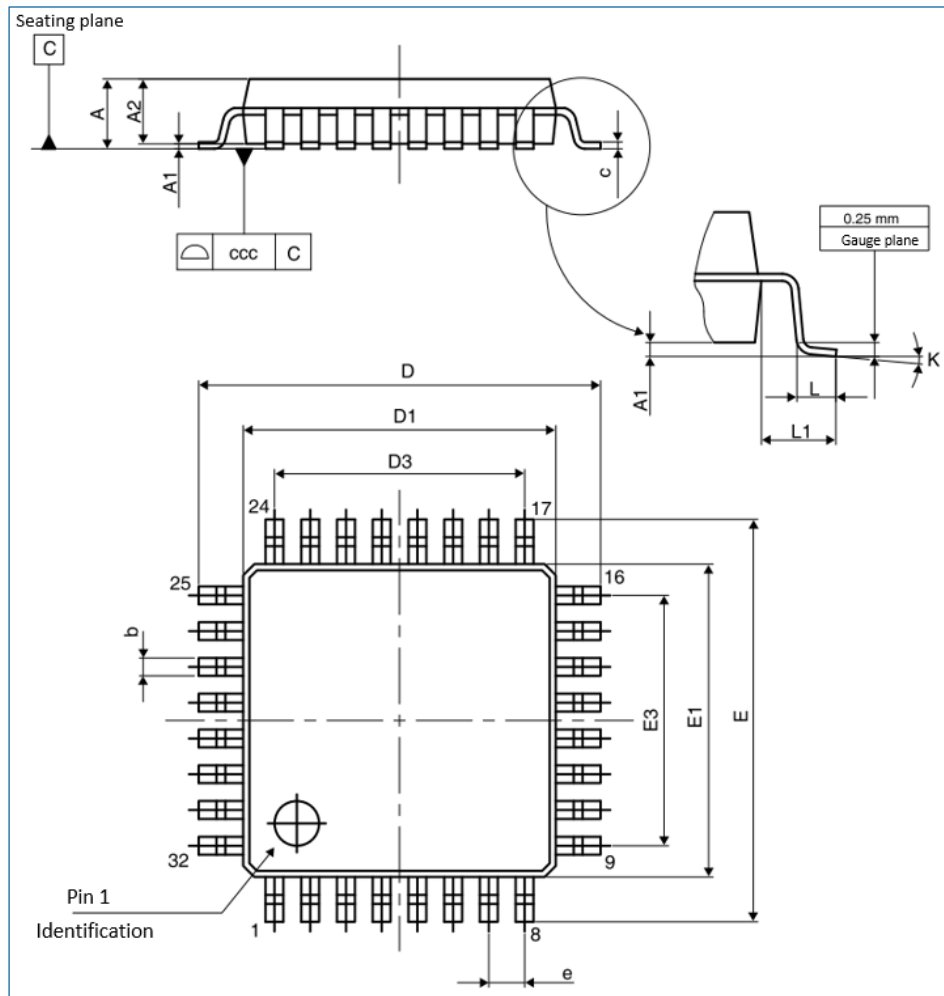


Figure 7-4 LQFP32 package outline

Table 7-4 LQFP32 package parameters

| Symbol | Min (mm) | Typ (mm) | Max (mm) | Min (inches) <sup>(1)</sup> | Typ (inches) <sup>(1)</sup> | Max (inches) <sup>(1)</sup> |
|--------|----------|----------|----------|-----------------------------|-----------------------------|-----------------------------|
| A      | -        | -        | 1.600    | -                           | -                           | 0.0630                      |
| A1     | 0.050    | -        | 0.150    | 0.0020                      | -                           | 0.0059                      |
| A2     | 1.350    | 1.400    | 1.450    | 0.0531                      | 0.0551                      | 0.0571                      |
| b      | 0.300    | 0.370    | 0.450    | 0.0118                      | 0.0146                      | 0.0177                      |
| c      | 0.090    | -        | 0.200    | 0.0035                      | -                           | 0.0079                      |
| D      | 8.800    | 9.000    | 9.200    | 0.3465                      | 0.3543                      | 0.3622                      |
| D1     | 6.800    | 7.000    | 7.200    | 0.2677                      | 0.2756                      | 0.2835                      |
| D3     | -        | 5.600    | -        | -                           | 0.2205                      | -                           |
| E      | 8.800    | 9.000    | 9.200    | 0.3465                      | 0.3543                      | 0.3622                      |
| E1     | 6.800    | 7.000    | 7.200    | 0.2677                      | 0.2756                      | 0.2835                      |
| E3     | -        | 5.600    | -        | -                           | 0.2205                      | -                           |
| e      | -        | 0.800    | -        | -                           | 0.0315                      | -                           |
| K      | 0°       | 3.5°     | 7°       | 0°                          | 3.5°                        | 7°                          |
| L      | 0.450    | 0.600    | 0.750    | 0.0177                      | 0.0236                      | 0.0295                      |
| L1     | -        | 1.000    | -        | -                           | 0.0394                      | -                           |
| ccc    | -        | -        | 0.100    | -                           | -                           | 0.0039                      |

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

## 7.5 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

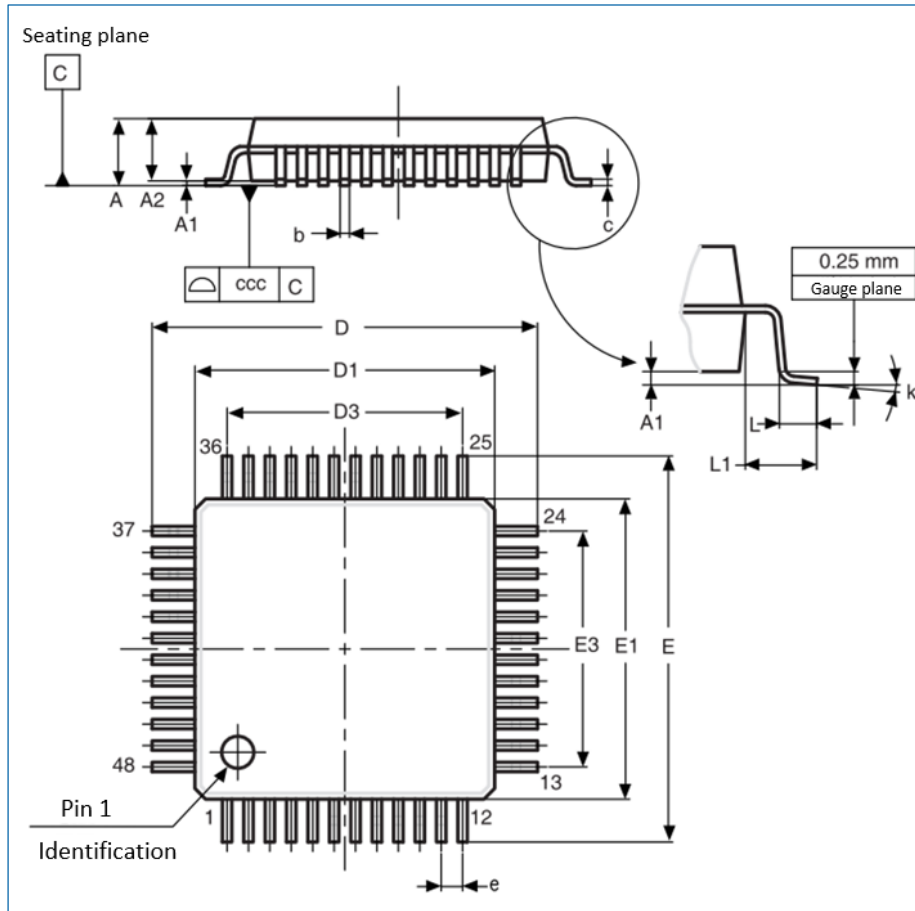


Figure 7-5 LQFP48 package outline

Table 7-5 LQFP48 package parameters

| Symbol | Min (mm) | Typ (mm) | Max (mm) | Min (inches) <sup>(1)</sup> | Typ (inches) <sup>(1)</sup> | Max (inches) <sup>(1)</sup> |
|--------|----------|----------|----------|-----------------------------|-----------------------------|-----------------------------|
| A      | -        | -        | 1.600    | -                           | -                           | 0.0630                      |
| A1     | 0.050    | -        | 0.150    | 0.0020                      | -                           | 0.0059                      |
| A2     | 1.350    | 1.400    | 1.450    | 0.0531                      | 0.0551                      | 0.0571                      |
| b      | 0.170    | 0.220    | 0.270    | 0.0067                      | 0.0087                      | 0.0106                      |
| c      | 0.090    | -        | 0.200    | 0.0035                      | -                           | 0.0079                      |
| D      | 8.800    | 9.000    | 9.200    | 0.3465                      | 0.3543                      | 0.3622                      |
| D1     | 6.800    | 7.000    | 7.200    | 0.2677                      | 0.2756                      | 0.2835                      |
| D3     | -        | 5.500    | -        | -                           | 0.2165                      | -                           |
| E      | 8.800    | 9.000    | 9.200    | 0.3465                      | 0.3543                      | 0.3622                      |
| E1     | 6.800    | 7.000    | 7.200    | 0.2677                      | 0.2756                      | 0.2835                      |
| E3     | -        | 5.500    | -        | -                           | 0.2165                      | -                           |
| e      | -        | 0.500    | -        | -                           | 0.0197                      | -                           |
| L      | 0.450    | 0.600    | 0.750    | 0.0177                      | 0.0236                      | 0.0295                      |
| L1     | -        | 1.000    | -        | -                           | 0.0394                      | -                           |
| k      | 0°       | 3.5°     | 7°       | 0°                          | 3.5°                        | 7°                          |
| ccc    | 0.080    |          |          | 0.0031                      |                             |                             |

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

## 7.6 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch package.

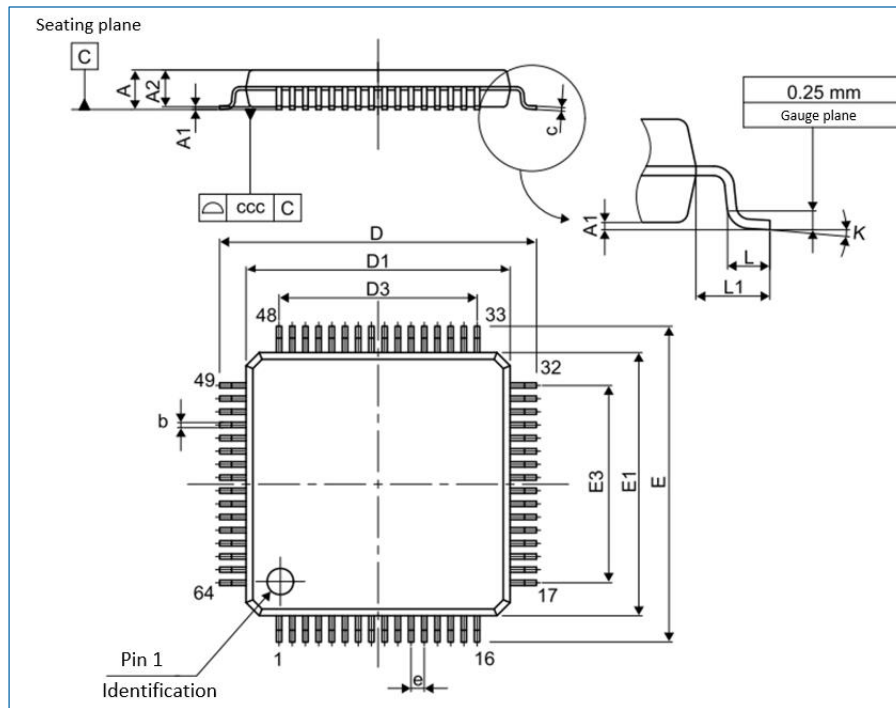


Figure 7-6 LQFP64 package outline

Table 7-6 LQFP64 package parameters

| Symbol | Min (mm) | Typ (mm) | Max (mm) | Min (inches) <sup>(1)</sup> | Typ (inches) <sup>(1)</sup> | Max (inches) <sup>(1)</sup> |
|--------|----------|----------|----------|-----------------------------|-----------------------------|-----------------------------|
| A      | -        | -        | 1.600    | -                           | -                           | 0.0630                      |
| A1     | 0.050    | -        | 0.150    | 0.0020                      | -                           | 0.0059                      |
| A2     | 1.350    | 1.400    | 1.450    | 0.0531                      | 0.0551                      | 0.0571                      |
| b      | 0.170    | 0.220    | 0.270    | 0.0067                      | 0.0087                      | 0.0106                      |
| c      | 0.090    | -        | 0.200    | 0.0035                      | -                           | 0.0079                      |
| D      | -        | 12.000   | -        | -                           | 0.4724                      | -                           |
| D1     | -        | 10.000   | -        | -                           | 0.3937                      | -                           |
| D3     | -        | 7.500    | -        | -                           | 0.2953                      | -                           |
| E      | -        | 12.000   | -        | -                           | 0.4724                      | -                           |
| E1     | -        | 10.000   | -        | -                           | 0.3937                      | -                           |
| E3     | -        | 7.500    | -        | -                           | 0.2953                      | -                           |
| e      | -        | 0.500    | -        | -                           | 0.0197                      | -                           |
| K      | 0°       | 3.5°     | 7°       | 0°                          | 3.5°                        | 7°                          |
| L      | 0.450    | 0.600    | 0.750    | 0.0177                      | 0.0236                      | 0.0295                      |
| L1     | -        | 1.000    | -        | -                           | 0.0394                      | -                           |
| ccc    | -        | -        | 0.080    | -                           | -                           | 0.0031                      |

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

## 8 Ordering information

Table 8-1 HK32ASAFE010xB ordering information

| Package Type | Part Number      | Shipping Option    | Remarks |
|--------------|------------------|--------------------|---------|
| TSSOP20      | HK32ASAFE010FBP6 | Tape and reel/Tube |         |
| QFN28        | HK32ASAFE010GBU6 | Tape and reel/Tray |         |
| QFN32        | HK32ASAFE010KBU6 | Tape and reel/Tray |         |
| LQFP32       | HK32ASAFE010KBT6 | Tape and reel/Tray |         |
| LQFP48       | HK32ASAFE010CBT6 | Tape and reel/Tray | -       |
| LQFP64       | HK32ASAFE010RBT6 | Tape and reel/Tray | -       |

## 9 Acronyms

| Term  | Full Name   |
|-------|---|
| ADC   | Analog-to-Digital Converter                             |
| AHB   | Advanced High-performance Bus                           |
| APB   | Advanced Peripheral Bus                                 |
| AWU   | Auto-wakeup Unit  |
| CRC   | Cyclic Redundancy Check                                 |
| CSS   | Clock Security System                                   |
| CTS   | Clear to Send   |
| DMA   | Direct Memory Access                                    |
| EXTI  | Extended Interrupt/Event Controller                     |
| GPIO  | General-purpose Input/Output                            |
| HSE   | High Speed External (Clock Signal)                      |
| I2C   | Inter-Integrated Circuit                                |
| I2S   | Inter-IC Sound  |
| IWDG  | Independent Watchdog                                    |
| LSI   | Low Speed Internal (clock signal)                       |
| MCU   | Microcontroller Unit                                    |
| MSPS  | Million Samples Per Second                              |
| NVIC  | Nested Vectored Interrupt Controller                    |
| PDR   | Power-down Reset  |
| PLL   | Phase-locked Loop                                       |
| POR   | Power-on Reset  |
| PPM   | Parts per Million                                       |
| PWM   | Pulse Width Modulation                                  |
| RCC   | Reset and Clock Control                                 |
| RISC  | Reduced Instruction Set Computer                        |
| RTS   | Request to Send   |
| SPI   | Serial Peripheral Interface                             |
| SRAM  | Static Random Access Memory                             |
| SWD   | Serial Wire Debug                                       |
| USART | Universal Synchronous/Asynchronous Receiver/Transmitter |
| WWDG  | Window Watchdog   |

## 10 Legal and contact information



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