HK32A040 Datasheet

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Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32A040 series microcontrollers (MCUs). This document helps you quickly understand the characteristics and functions of HK32A040.

Audience

This document is intended for:

- HK32A040 developers
- HK32A040 testers
- HK32A040 users

Release Notes

This document is applicable to HK32A040 series MCUs.

Revision History

Version	Date	Description
1.0	2023/10/20	The initial release.

Contents

1 Introduction

This document is the datasheet for HK32A040 series MCUs. HK32A040 is a family of automotive MCUs developed by Shenzhen Hangshun Chip Technology R&D Co., Ltd. (hereinafter referred to as Hangshun). This MCU family includes:

- HK32A040RBT3 (LQFP64 package)
- HK32A040CBT3 (LQFP48 package)
- HK32A040KBU3 (QFN32 package)
- HK32A040GBU3 (QFN28 package)

For more details of HK32A040, see *HK32A040 User Manual*.

2 Product overview

HK32A040 adopts the ARM® Cortex®-M0 core operating at a maximum frequency of 96 MHz and has up to 124 Kbytes of flash and 10 Kbytes of SRAM. You can configure the Flash controller register to remap interrupt vectors in the main Flash.

HK32A040 supports conventional Flash readout protection (RDP) Level 0, Level 1, and Level 2 and provides the patented Flash code encryption function of Hangshun.

To meet the security requirements of various applications, HK32A040 provides the hardware cyclic redundancy check (CRC), Advanced Encryption Standard (AES), hash, and True Random Number Generator (TRNG) hardware units. These hardware units can be used to verify data accuracy and data integrity during data transmission and storage and to encrypt and decrypt Flash data.

HK32A040 incorporates a wide selection of communication interfaces:

- 2 × USARTs and 1 × LPUART (up to 12 Mbit/s)

  The USARTs support the synchronous and asynchronous full-duplex or half-duplex communication, multiprocessor communication, LIN protocol, Smart Card protocol, and IrDA SIR ENDEC. The RX and TX pins can be exchanged by using the software. The USARTs and LPUART can wake up the MCU from Stop mode when receiving data.

- Up to 2 × high-speed SPIs/I2Ss (up to 18 Mbit/s)

  The SPIs/I2Ss support the 4-bit to 16-bit full-duplex or half-duplex communication, master/slave mode, TI mode, NSS pulse mode, automatic CRC, and I2S protocol.

- Up to 2 × high-speed I2Cs (up to 1 Mbit/s)

  The I2Cs support the 1 MHz, 400 kHz, and 100 kHz transmission modes, master/slave mode, multimaster mode, 7-bit/10-bit addressing, and SMBus protocol. The I2Cs can wake up the MCU from Stop mode when receiving data.

HK32A040 embeds a 16-bit advanced PWM timer (four PWM output channels in total, three of which have complementary PWM outputs with programmable inserted dead-times), a 32-bit and five 16-bit general-purpose PWM timers, and a basic timer.

HK32A040 also incorporates the analog circuitry: a 12-bit ADC (16 analog signal input channels in total, differential pair input supported; sampling rate of up to 1 MSPS), the power-on reset (POR)/power-down reset (PDR) circuitry, an internal reference voltage obtained from internal ADC sampling, and a 1/2 V_{BAT} voltage divider circuit.

HK32A040 integrates the division and square root (DVSQ) hardware unit which provides higher performance than software and faster responses to external events.

A hardware unit of motor algorithms is embedded in HK32A040, speeding up the processing of motor drive operations.

HK32A040 has four configurable logic units (CLUs) for configurable synchronous and asynchronous Boolean logic operations.

Except for the power pins, ground pins, and NRST pins, all the other pins of HK32A040 can be used as GPIOs, peripheral I/Os, or external interrupt inputs. This way, more pin functions can be provided.

HK32A040 operates in the –40°C to +125°C temperature range, from a 1.8 V to 3.6 V power supply. It meets the environmental requirements of most applications.

HK32A040 is suitable for automotive electronics applications.

2.1 Features

- CPU core

- ARM® Cortex®-M0
- Maximum frequency: 96 MHz
- 24-bit SysTick timer
- Supports the remapping of interrupt vectors (configured by using the Flash controller register)

- Operating voltage range
  - Single power domain (main power supply V_{DD}): 1.8 V to 3.6 V
  - Backup power supply V_{BAT}: 1.8 V to 3.6 V
- Operating temperature range: –40°C to +125°C
- Typical operating current
  - Run mode: 6.1 mA@96 MHz; 1.6 mA@8 MHz
  - Sleep mode: 4.7 mA@96 MHz
  - Stop mode:
    - LDO full-speed: 0.7 mA@3.3 V
    - LDO low-power: 60 µA@3.3 V
  - Standby mode: 1.6 µA@3.3 V
  - Shutdown mode: 0.4 µA@3.3 V
- Memory
  - Up to 124 Kbytes of Flash
    - No wait state for Flash access when the CPU frequency is 24 MHz or lower
    - Separate read and write protection for Flash data
    - Encryption for instructions and data stored in the Flash, preventing the damage caused by physical attacks
  - 10-Kbyte SRAM
- Data security
  - CRC hardware implementation unit
  - Multiple encryption modules including AES, hash, and TRNG
- Clock
  - High-speed external clock (HSE): 4 MHz to 32 MHz, typical value: 8 MHz
  - Low-speed external clock (LSE): 32.768 kHz
  - High-speed internal clock (HSI): configurable to 8 MHz/14 MHz/56 MHz
  - Low-speed internal clock (LSI): 40 kHz
  - PLL clock: 96 MHz (maximum value)
  - Chip pin input clock (EXTCLK)
- Reset
  - External pin reset
  - POR/PDR
  - Software reset
  - IWDG and WWDG reset
  - Low-power management reset
  - Option byte loading (OBL) reset

- Programmable voltage detector (PVD)
  - Adjustable eight-level thresholds for detecting voltage
  - Rising edge and falling edge detection configurable
- GPIO
  - Up to 55 GPIO pins
  - Each GPIO pin can be used as an external interrupt input
- Data communication interface
  - 2 × USARTs: support synchronous transmission corresponding to SPI master mode and the modem hardware flow control. Provide the ISO7816 interface, LIN, IrDA capability, automatic baud rate detection, and the feature of wakeup from Stop mode.
  - Up to 2 × high-speed SPIs: support 4-bit to 16-bit programmable data frames, I2S multiplexed.
  - Up to 2 × I2Cs: can operate in fast mode plus (1 MHz) and support SMBus and PMBus. Can wake up the MCU from Stop mode when receiving data.
  - 1 × LPUART: supports asynchronous serial communication, single-wire half-duplex communication, modem hardware flow control (CTS/RTS), and multiprocessor communication in the lowest power mode.
  - 1 × CAN: compliant with Specification 2.0A and 2.0B (active).
- Timer and PWM generator
  - 1 × 16-bit advanced timer: with the break function and four PWM outputs in total, three of which have complementary PWM outputs with programmable inserted dead-times
  - 5 × 16-bit and 1 × 32-bit general-purpose timers: TIM2/TIM3/TIM14/TIM15/TIM16/TIM17
  - 1 × 16-bit basic timer: TIM6
- On-chip analog circuitry
  - 1 × 12-bit SAR ADC (up to 16 analog input channels)
  - Maximum frequency: 1 MSPS
  - Supports automatic continuous conversion and scan conversion
  - 3 × voltage comparators
- DMA controller (7-channel)
  - Can be triggered by peripherals such as the timer, ADC, SPI, I2C, USART, AES, and hash
- Temperature sensor
  - The analog output is connected to an independent ADC channel.
- CPU trace and debug
  - SWD debug port
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (for low-power mode simulation control, debugged peripheral clock control, and debug and trace interfaces allocation)
- Division and square root calculation unit
  - Supports 32-bit fixed point division, with the quotient and remainder calculated
  - Supports 32-bit fixed point high-precision root calculation
- Four configurable logic units (CLUs) for handling simple logic operations
- Electric motor acceleration (EMACC) hardware unit for faster motor algorithm processing
- RTC

- With the alarm function
- Periodically wakes up the MCU from Stop or Standby mode

- 96-bit unique ID (UID) of each MCU
- Reliability
  - Passed HBM6000V/CDM2000V/MM200V/LU200mA level tests.

2.2 Device overview

Table 2-1 HK32A040 series features

Feature		HK32A040RBT3	HK32A040CBT3	HK32A040KBU3	HK32A040GBU3
Package		LQFP64	LQFP48	QFN32	QFN28
GPIOs		55	39	27	23
Operating voltage	Main power supply	1.8 V – 3.6 V			
	Backup power supply	1.8 V – 3.6 V			
Operating temperature		–40°C to +125°C			
Memory	Flash (Kbyte)	124			
	SRAM (Kbyte)	10			
CPU	Core	Cortex®-M0			
	Frequency	96 MHz			
DMA		7-channel (handles the ADC/SPI/I2C/USART/Timer/AES/hash requests)			
Division and square root (DVSQ) calculation unit		Supported			
Clock	LSI	40 kHz			
	HSI	Configurable to 8 MHz/14 MHz/56 MHz (default: 56 MHz)			
	PLL clock	Up to 96 MHz			
	HSE	4 – 32 MHz			
	LSE	32.768 kHz			
Timer	Advanced timer	TIM1 (16-bit)			
	General-purpose timer	32-bit: TIM2 16-bit: TIM3/TIM14/TIM15/TIM16/TIM17			
	Basic timer	TIM6 (16-bit)			
	SysTick timer	Supported			
	RTC	Supported			
	IWDG	Supported			
	WWDG	Supported			
Peripheral comm. interface	USART	2			
	LPUART	1			
	I2C	2	2	2	1
	SPI/I2S	2/2	2/2	1/1	1/1
	CAN (2.0A/2.0B)	1			
ADC	External channels	16	10	10	10
	Reference selection	External reference voltage input			
	Sampling rate	1 MSPS			
	Accuracy	12-bit			
Electric motor acceleration (EMACC)		1			
Programmable voltage detector (PVD)		Supported			
Voltage comparator (COMP)		3			

Feature		HK32A040RBT3	HK32A040CBT3	HK32A040KBU3	HK32A040GBU3
Configurable logic unit (CLU)		4			
Info. security	CRC	Supported			
	96-bit UID	Supported			
	AES	Supported			
	Hash	Supported			
	TRNG	Supported			

3 Function description

3.1 Block diagram

ARM® Cortex®-M0 is a 32-bit RISC processor that provides an MCU platform featuring low cost and low power consumption. It delivers outstanding computational performance and advanced system responses to interrupts. With an embedded ARM® Cortex®-M0 core, the HK32A040 family is compatible with ARM tools and software.

The block diagram of HK32A040RBT3 is as follows:

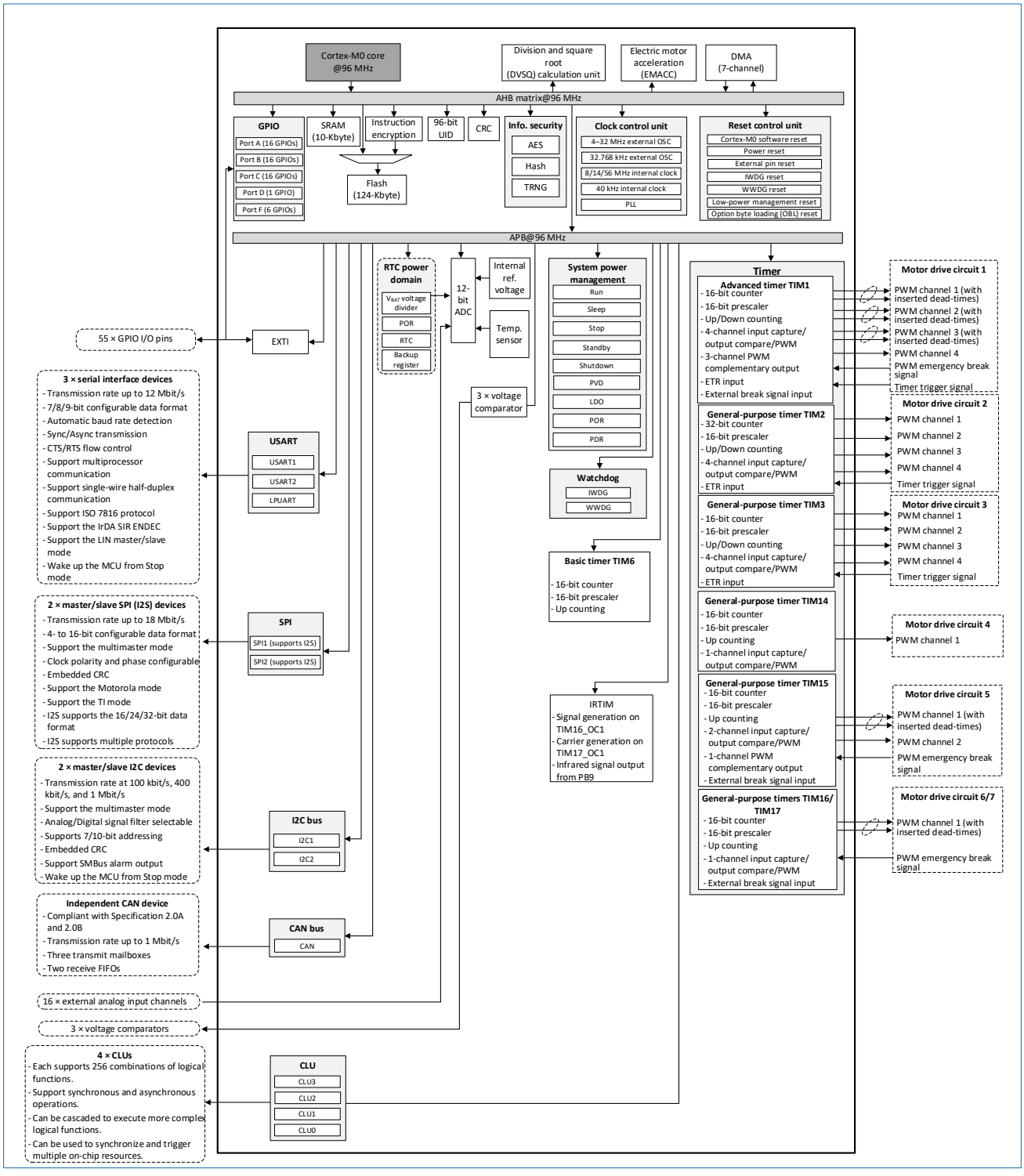

Figure 3-1 HK32A040RBT3 block diagram

3.2 Memory mapping

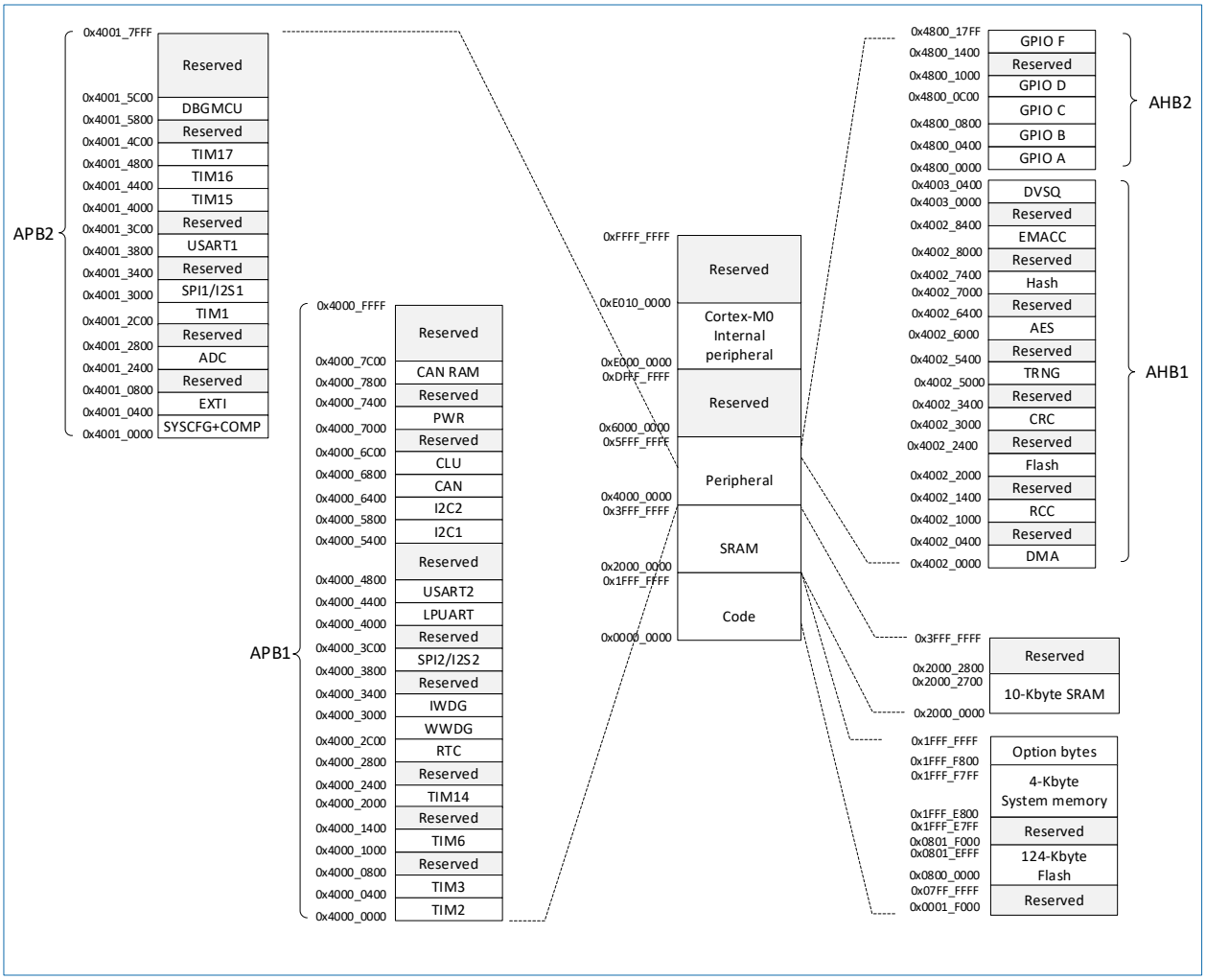

Figure 3-2 HK32A040 memory mapping

3.3 Flash

HK32A040 integrates a Flash memory of up to 124 Kbytes to store programs and data.

3.4 SRAM

HK32A040 integrates a 10-Kbyte SRAM which can be accessed in words, half words, or bytes. The CPU can access the SRAM with no wait state, meeting the requirements of most applications.

3.5 Resets

3.5.1 System reset

The system reset resets all registers, except for the reset flags in the control/status register RCC_CSR and the registers in the backup domain. You can identify the reset source by checking reset status flags in the RCC_CSR register.

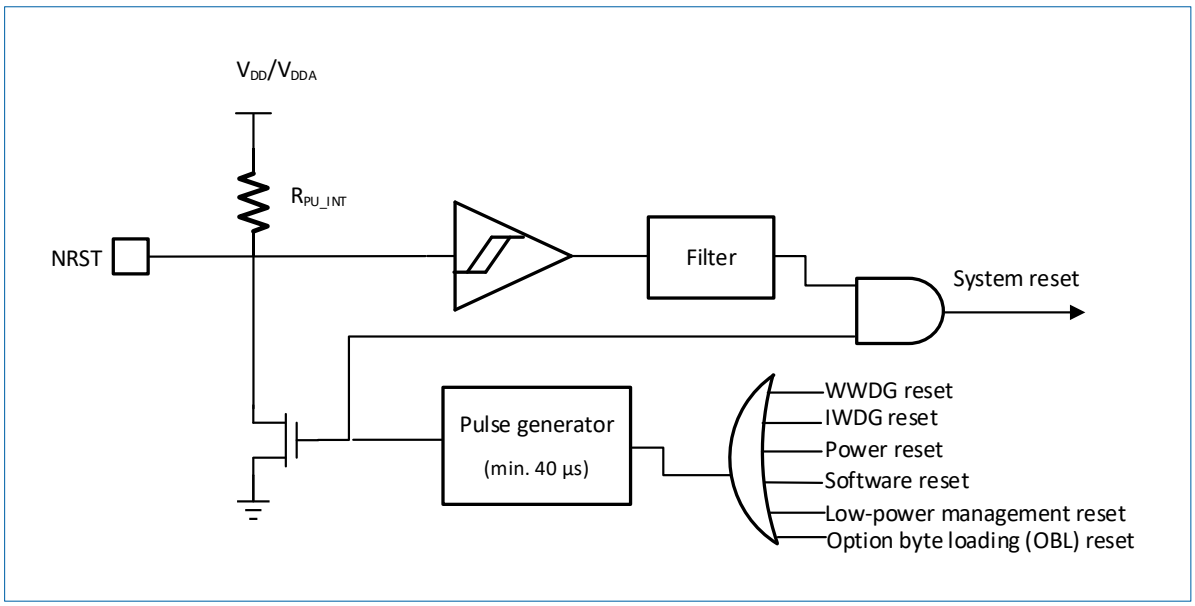

Figure 3-3 Reset signal

A system reset is generated when any of the following events occurs:

- Low level on the NRST pin (external reset)
- Window watchdog counting terminates (WWDG reset)
- Independent watchdog counting terminates (IWDG reset)
- Software reset (SW reset): The SYSRESETREQ bit in Cortex®-M0 Application Interrupt and Reset Control Register must be set to 1 to force a software reset on the device.
- Low-power management reset
- Option byte loading (OBL) reset

The reset sources act on the NRST pin and the NRST pin keeps the low level during resets. The reset routine vector is fixed at address 0x0000 0004.

The internal reset signals are output on the NRST pin. The pulse generator guarantees a reset pulse duration of at least 40 µs for each internal reset source. When the NRST pin is pulled low and an external reset is generated, the reset pulse is generated.

3.5.2 Power reset

A power reset is generated when any of the following events occurs:

- POR/PDR
- Exit from Standby mode

The power reset resets all registers, except for the registers in the backup domain.

HK32A040 MCUs contain the power-on reset (POR)/power-down reset (PDR) circuitry. The circuitry keeps operating to ensure that the system runs properly when the power supply exceeds the 1.8 V threshold. When V_{DD} is less than the POR/PDR threshold, the MCU will be reset without using any external reset circuit.

3.5.3 Backup domain reset

The backup domain has two resets that only affect the backup domain.

A backup domain reset is generated when any of the following events occurs:

- Software reset triggered by the BDRST bit in the RCC_BDCR register
- V_{DD} and/or V_{BAT} power-on after being powered down

3.6 Clocks and clock tree

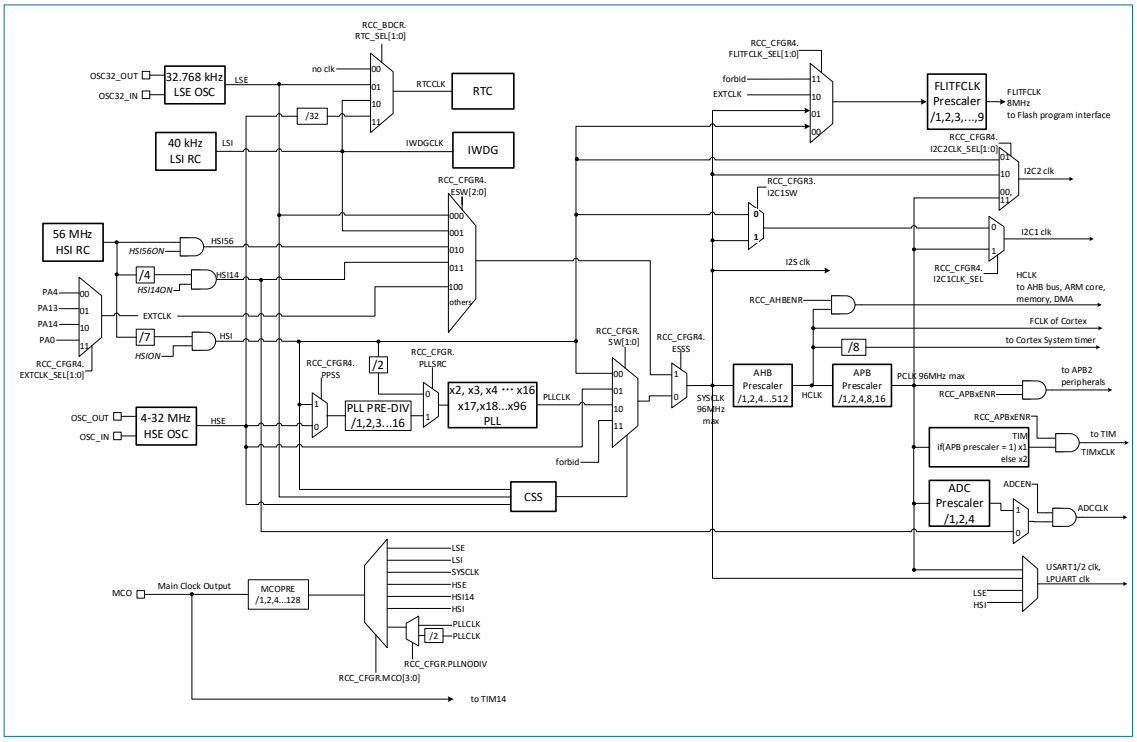

Figure 3-4 Clock tree of HK32A040

As Figure 3-4 shows, HSI and HSI14 are generated by the same internal oscillator operating at 56 MHz. Therefore, when HSI or HSI14 is used, disabling the other clock cannot reduce power consumption. HSI/HSE can be used as the input of the phase-locked loop (PLL) prescaler. You can use HSI together with PLL to configure different system clock frequencies.

HK32A040 MCUs use SYSCLK as the CPU clock when they start. The 56 MHz clock output by the internal oscillator, or the prescaled HSI or HSI14 can be used as the SYSCLK.

HK32A040 provides more clock sources for the system clock and offers convenient, flexible, and diverse operating modes to products. The following clocks can act as the system clock:

- 56 MHz HSI
- HSE
- PLL clock
- 14 MHz HSI14
- 8 MHz HSI
- 40 kHz LSI, which can drive the IWDG or be used as the RTC to automatically wake up the MCU from Stop/Standby mode
- 32.768 kHz LSE, which can drive the RTCCLK

In addition, PCLK can act as the I2C clock source.

3.7 Power supply scheme

- V_{DD} = 1.8 V to 3.6 V. The V_{DD} pin supplies power to I/O pins and the internal low dropout regulators (LDOs).
- V_{DDA} = 1.8 V to 3.6 V. The V_{DDA} pin supplies power to the analog circuitry, such as the ADC and temperature sensor.
- V_{BAT} = 1.8 V to 3.6 V. When V_{DD} is powered off, V_{BAT} supplies power to the RTC, external 32.768 kHz oscillator, and backup registers.

3.8 Boot modes

The Boot0 pin and its configuration bit are used to select the system boot mode:

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The bootloader program is stored in the system memory. The bootloader program can reprogram the Flash via the USART1 PA9/PA10 pin or USART2 PA14/PA15 pin.

3.9 PVD

HK32A040 integrates a programmable voltage detector (PVD). The PVD monitors V_{DD} and compares it with the V_{PVD} threshold. When V_{DD} is below or over the V_{PVD} threshold, an interrupt is generated, and the interrupt program may send a warning message or set the MCU in the safe state. The PVD is enabled by setting the software.

3.10 Low-power modes

HK32A040 supports multiple power consumption modes.

- Run mode

  In Run mode, the CPU runs at full speed.

- Sleep mode

  In Sleep mode, only the CPU stops. All peripherals keep operating. The CPU can be woken up when an interrupt or event occurs.

- Stop mode

  In Stop mode, MCUs achieve the lowest power consumption while retaining the content in SRAM and registers. In Stop mode, all clocks in the core domain, the HSI RC oscillator, and the HSE crystal oscillator are disabled. MCUs can be woken up from Stop mode by any EXTI line, such as a PVD output or an RTC alarm.

- Standby mode

  In Standby mode, the MCU achieves the very power consumption. The internal LDO is off, so the entire 1.2 V domain is powered off. The PLL, HSI RC oscillator, and HSE crystal oscillator are disabled. The SRAM and register content is lost, except for registers in the backup domain. The Standby circuitry works as normal.

  MCUs exit from Standby mode when an external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

- Shutdown mode

  In Shutdown mode, the MCU achieves extremely low power consumption as in Standby mode. All internal LDO power supplies (including the power supply of the backup domain) and all clock sources are off, except for the shutdown wakeup circuitry. MCUs exit from Shutdown mode when an external reset on the NRST pin, an IWDG reset, or a rising edge on the WKUP pin occurs. The backup domain is off, so the MCU cannot be woken up by an RTC alarm.

Table 3-1 Operating modes and power consumption

Operating Mode	Test Condition	Power Consumption(1)	Wakeup Time
Run mode	HCLK = 8 MHz, APB clock disabled	Power consumption 1.6 mA/8 MHz@3.3 V	-
Sleep mode	HCLK = 8 MHz, APB clock disabled	Power consumption 1.3 mA/8 MHz@3.3 V	4.7 µs
Stop mode	LDO in the low-power state, HSE/HSI/LSE disabled, IWDG disabled	Static power consumption 60 µA@3.3 V	132 µs (fastest speed)
Standby mode	All oscillators disabled	Static power consumption 1.6 µA@3.3 V	152 µs
Shutdown mode	LSE and RTC disabled	Lowest static power consumption 0.4 µA@3.3 V	364 µs

(1). For details about the test condition of each power consumption indicator, see Table 4-8.

The conditions for entering and exiting low-power modes are listed in the following table:

Table 3-2 Conditions of entering and exiting low-power modes

Operating Mode	Entry	Exit
Sleep	1. Set PWR_CR:LPDS = 0. 2. The software executes WFI/WFE instructions.	Any IRQ interrupt/event, including the SysTick timer.
Stop	1. Set PWR_CR:LPDS = 0. 2. Set the SLEEPDEEP bit in the Cortex-M0 system control register. The software executes WFI/WFE instructions.	Any EXTI line.
Standby	1. Set PWR_CR:LPDS = 0. 2. Set PWR_CR:PDDS = 1. 3. Set the SLEEPDEEP bit in the Cortex-M0 system control register. The software executes WFI/WFE instructions.	An external reset on the NRST pin, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm
Shutdown	1. Set PWR_CR:LPDS = 0. 2. Set PWR_CR:PDDS = 1. 3. Set PWR_CSR2:SHDS = 1. 4. Set the SLEEPDEEP bit in the Cortex-M0 system control register. The software executes WFI/WFE instructions.	Three polarity-configurable external pins.

3.11 NVIC

HK32A040 incorporates the nested vectored interrupt controller (NVIC). NVIC can flexibly manage up to 32 maskable interrupt channels (excluding 16 Cortex®-M0 interrupt lines) and four interrupt priorities with the lowest interrupt latency.

- The closely coupled NVIC ensures low latency during interrupt processing.
- The interrupt vector entry address is directly passed to the core.
- Allows the early processing of interrupts.
- Processes higher-priority interrupts even if they arrive late.
- Supports tail-chaining.
- Saves the processor state automatically.
- The previous state is resumed upon interrupt exit with no extra instruction needed.

Table 3-3 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000_0000
-	-3	Fixed	Reset	Reset	0x0000_0004
-	-2	Fixed	NMI	Non-maskable interrupt. The RCC clock security system (CSS) is connected to the NMI vector.	0x0000_0008
-	-1	Fixed	HardFault	All classes of faults	0x0000_000C
-	3	Configurable	SVCall	System service call via SWI instruction	0x0000_002C
-	5	Configurable	PendSV	Pendable request for system service	0x0000_0038
-	6	Configurable	SysTick	SysTick timer	0x0000_003C
0	7	Configurable	WWDG	Window watchdog interrupt	0x0000_0040
1	8	Configurable	PVD	PVD interrupt (through EXTI line 16)	0x0000_0044
2	9	Configurable	RTC	RTC interrupt (through EXTI line 17, 19, and 20)	0x0000_0048
3	10	Configurable	Flash	Flash global interrupt	0x0000_004C
4	11	Configurable	RCC	RCC global interrupt	0x0000_0050

Position	Priority		Name	Description	Address
5	12	Configurable	EXTI0_1	EXTI Line[1:0] interrupts	0x0000_0054
6	13	Configurable	EXTI2_3	EXTI Line[3:2] interrupts	0x0000_0058
7	14	Configurable	EXTI4_15	EXTI Line[15:4] interrupts	0x0000_005C
8	15	Configurable	LPUART_IRQ	LPUART interrupt (through EXTI line 28)	0x0000_0060
9	16	Configurable	DMA_CH1	DMA channel 1 global interrupt	0x0000_0064
10	17	Configurable	DMA_CH2_3	DMA channel 2/3 interrupt	0x0000_0068
11	18	Configurable	DMA_CH4_7	DMA channel 4/5/6/7 interrupt	0x0000_006C
12	19	Configurable	ADC	ADC interrupt (through EXTI line 21, 22, 30, and 31)	0x0000_0070
13	20	Configurable	TIM1_BRK_UP_TRG_COM	TIM1 break, update, trigger, and commutation interrupt	0x0000_0074
14	21	Configurable	TIM1_CC	TIM1 capture/compare interrupt	0x0000_0078
15	22	Configurable	TIM2	TIM2 global interrupt	0x0000_007C
16	23	Configurable	TIM3	TIM3 global interrupt	0x0000_0080
17	24	Configurable	TIM6	TIM6 global interrupt	0x0000_0084
18	25	Configurable	-	Reserved	0x0000_0088
19	26	Configurable	TIM14	TIM14 global interrupt (through EXTI line 32 connected to CLU0)	0x0000_008C
20	27	Configurable	TIM15	TIM15 global interrupt	0x0000_0090
21	28	Configurable	TIM16	TIM16 global interrupt (through EXTI line 33 connected to CLU1)	0x0000_0094
22	29	Configurable	TIM17	TIM17 global interrupt	0x0000_0098
23	30	Configurable	I2C1	I2C1 global interrupt (through EXTI line 23)	0x0000_009C
24	31	Configurable	I2C2	I2C2 global interrupt (through EXTI line 24)	0x0000_00A0
25	32	Configurable	SPI1	SPI1 global interrupt (through EXTI line 34 connected to CLU2)	0x0000_00A4
26	33	Configurable	SPI2	SPI2 global interrupt (through EXTI line 35 connected to CLU3)	0x0000_00A8
27	34	Configurable	USART1	USART1 global interrupt (through EXTI line 25)	0x0000_00AC
28	35	Configurable	USART2	USART2 global interrupt (through EXTI line 26)	0x0000_00B0
29	36	Configurable	AES_TRNG_HASH_EMACC	AES, TRNG, HASH, and EMACC global interrupt	0x0000_00B4
30	37	Configurable	CAN	CAN global interrupt	0x0000_00B8
31	38	Configurable	DVSQ	DVSQ global interrupt	0x0000_00BC

3.12 EXTI

The external interrupt/event controller (EXTI) manages 34 interrupt lines that are used to generate interrupt/event requests and wake up the system through edge detection. The trigger event of each EXTI line can be configured and masked independently. The trigger event can be a rising edge, a falling edge, or both. The pending register stores the status of each interrupt request. EXTI can detect external interrupt line signals whose pulse width is shorter than the internal clock period. Up to 55 GPIOs can be connected to up to 16 external interrupt lines.

The EXTI lines from EXTI 0 to EXTI 15 are connected to I/O pins. The connections of the other EXTI lines are as follows:

- EXTI 16 connected to the PVD output
- EXTI 17 connected to the RTC alarm event
- EXTI 19 connected to the RTC tamper detection and timestamp event

- EXTI 20 connected to the RTC wakeup event
- EXTI 21 connected to the Comp1 output
- EXTI 22 connected to the Comp2 output
- EXTI 23 connected to the I2C1 wakeup event
- EXTI 24 connected to the I2C2 wakeup event
- EXTI 25 connected to the USART1 wakeup event
- EXTI 26 connected to the USART2 wakeup event
- EXTI 28 connected to the LPUART wakeup event
- EXTI 30 connected to the Comp3 output
- EXTI 31 connected to the ADC AWD event
- EXTI 32 connected to the CLU0 output
- EXTI 33 connected to the CLU1 output
- EXTI 34 connected to the CLU2 output
- EXTI 35 connected to the CLU3 output

EXTI lines from EXTI 23 to EXTI 26, EXTI 28, and EXTI 31 are connected to internal events and do not have the rising trigger selection register (RTSR), falling trigger selection register (FTSR), software interrupt event register (SWIER), and pending register (PR). These EXTI lines detect the rising edge of events in only Stop mode and generate the event request (ERQ) and interrupt request (IRQ) to wake up the system. The corresponding interrupt control bit and status bit are stored in the peripheral from which events are generated.

3.13 IWDG

The independent watchdog (IWDG) is based on a 12-bit downcounter and a 3-bit prescaler. The IWDG is clocked by an internal independent 40 kHz RC oscillator. The RC oscillator is independent of the main clock, so it can operate in Stop mode and Standby mode. The IWDG can reset the system when a problem occurs or work as a free-running timer that provides timeout management for applications. The IWDG can be started by hardware or software through the configuration of the option bytes. In debug mode, the counter can be frozen.

You can set the IWDG_WINR register to use IWDG in window mode.

3.14 WWDG

The window watchdog (WWDG) is based on an internal 7-bit downcounter. The counter can be set to the free running mode or used as a watchdog to reset the system when the system crashes. The WWDG is clocked by the main clock and has the early warning interrupt function. In debug mode, the counter can be frozen.

3.15 SysTick timer

The SysTick timer is a dedicated standard downcounter for the operating system. Its features include:

- 24-bit downcounter
- Auto-reload capability
- Generates a maskable interrupt when the counter reaches 0
- Programmable clock source

3.16 Timers

Each HK32A040 MCU has an advanced timer, six general-purpose timers, and a basic timer. The features of the timers are listed in the following table.

Table 3-4 Features of the timers

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	0 – 0xFFFF	Yes	Yes	4	3
General-purpose timer	TIM2	32-bit	Up, down, up/down	0 – 0xFFFF	Yes	No	4	No
	TIM3	16-bit	Up, down, up/down	0 – 0xFFFF	Yes	No	4	No
	TIM14	16-bit	Up	0 – 0xFFFF	No	No	1	No
	TIM15	16-bit	Up	0 – 0xFFFF	Yes	Yes	2	1
	TIM16	16-bit	Up	0 – 0xFFFF	Yes	Yes	1	1
	TIM17	16-bit	Up	0 – 0xFFFF	Yes	Yes	1	1
Basic timer	TIM6	16-bit	Up	0 – 0xFFFF	Yes	No	No	No

3.16.1 Advanced timer

HK32A040 integrates an advanced timer TIM1.

TIM1 can be deemed as a three-phase PWM generator with six channels or used as a complete general-purpose timer. The four independent channels of TIM1 can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned mode)
- One-pulse mode output

Three of the four channels have complementary PWM outputs with programmable inserted dead-times.

If TIM1 is configured as a 16-bit basic timer, it has the same functions as a basic timer. If the advanced timer is configured as a 16-bit PWM generator, it has full modulation capability (0 – 100%). Many functions of TIM1 are the same as those of general-purpose timers. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

In debug mode, the counter can be frozen.

3.16.2 General-purpose timer

HK32A040 integrates six general-purpose timers.

- TIM2 and TIM3

  TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have four independent channels respectively. The channels can be used for input capture, output compare, PWM output, and one-pulse mode output. In the LQFP64 package, up to 12 channels are available for input capture, output compare, and PWM output.

  TIM2 and TIM3 can work with advanced timer TIM1 through the Timer Link feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 can process quadrature (incremental) encoder signals and the digital outputs from one to three hall-effect sensors. In debug mode, the counter can be frozen.

- TIM14 and TIM15

  TIM14 and TIM15 are based on a 16-bit auto-reload upcounter and a 16-bit prescaler respectively. TIM14 has a channel for input capture, output compare, PWM output, and one-pulse mode output. TIM15 has two channels, one of which is for complementary output. In debug mode, the counter can be frozen. TIM15 can generate DMA requests but TIM14 cannot.

- TIM16 and TIM17

  TIM16 and TIM17 are based on a 16-bit auto-reload upcounter and a 16-bit prescaler respectively. TIM16 and TIM17 have a channel respectively for input capture, output compare, PWM output, and one-pulse mode output. TIM16 and TIM17 all have complementary outputs with programmable inserted dead-times and can generate independent DMA requests. In debug mode, the counter can be frozen.

3.16.3 Basic timer

HK32A040 integrates a basic timer TIM6.

TIM6 embeds a 16-bit upcounter and a 16-bit prescaler.

3.17 IRTIM

An infrared interface (IRTIM) is embedded in each HK32A040 MCU. The IRTIM works with infrared LEDs to provide the remote control function. To generate infrared remote control signals, you must enable the IRTIM (PB9) and configure TIM16 channel 1 (TIM16_OC1) and TIM17 channel 1 (TIM17_OC1).

The infrared receiver function can be implemented by setting TIM16 channel 1 and TIM17 channel 1 to the basic input capture mode.

3.18 I2C

Up to two I2C bus interfaces are embedded in HK32A040 MCUs. The I2C bus interfaces can operate in master or slave mode and support the following modes:

- Standard mode (up to 100 kHz)
- Fast mode (up to 400 kHz)
- Fast mode plus (up to 1 MHz)

The I2C bus interfaces support the 7-bit or 10-bit addressing mode and 7-bit dual addressing mode (as slave). The I2C interfaces embed hardware CRC generation/verification.

The I2C interfaces are compatible with SMBus 2.0 and PMBus 1.1. The address resolution protocol (ARP) capability, host notify protocol, hardware CRC (packet error checking, PEC) generation/verification, timeout verification, and alert protocol management are supported.

The I2C interfaces also have a clock independent of the CPU clock domain, so they can wake up the MCU from Stop mode when the address is matched.

The I2C interfaces have an analog filter and a digital filter. The following table lists the features of the filters:

Table 3-5 Programmable analog noise filter and digital noise filter

	Analog Filter	Digital Filter
Suppressed pulse width	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clock periods
Advantage	Available in Stop mode	• Extra filtering capability, standard requirements • Stable programmable length
Disadvantage	Performance changes along with the temperature, voltage, and process	When the digital filter is enabled, I2C cannot wake up the MCU from Stop mode even if the address is matched.

3.19 USART

Two universal synchronous/asynchronous receivers/transmitters (USART1 and USART2) are embedded in each

HK32A040 MCU. They can communicate at up to 12 Mbit/s.

The USARTs provide hardware management for the CTS, RTS, and RS485 DE signals. The USARTs support the multiprocessor communication mode, host synchronous communication mode, and single-wire half-duplex communication mode. The USARTs also support Smart Card communication (ISO 7816), IrDA SIR ENDEC, LIN master/slave capability, and automatic baud rate detection. The USARTs can be served by the DMA controller.

The USARTs have a clock independent of the CPU clock domain, so they can wake up the MCU from Stop mode.

Table 3-6 USART1/USART2 features

Feature	USART1/USART2
Modem hardware flow control	Supported
DMA continuous transmission	Supported
Multiprocessor communication	Supported
Synchronous mode	Supported
Smart Card mode	Supported
Single-wire half-duplex communication	Supported
IrDA SIR ENDEC	Supported
LIN mode	Supported
Dual clock domains and wakeup from Stop mode	Supported
Receiver timeout interrupt	Supported
Modbus communication	Supported
Automatic baud rate detection	Supported
Driver enable	Supported

3.20 LPUART

HK32A040 incorporates a low-power universal asynchronous receiver/transmitter (LPUART) which can communicate at up to 10 Mbit/s. The LPUART supports asynchronous serial communication, single-wire half-duplex communication, and modem hardware flow control (CTS/RTS) in low-power mode. It also supports multiprocessor communication.

The LPUART has a clock independent of the CPU clock domain. It can wake up the MCU from Stop mode at a baud rate of up to 4.8 kbit/s. The LPUART can wake up the MCU from Stop mode when any of the following events occurs:

- Start bit detection event
- Interrupt of receiving any data frame
- Receiving specific programming data frame

When using the 32.768 kHz LSE, the LPUART can communicate at up to 9600 baud. In Stop mode, the LPUART waits for incoming frames at extremely low power consumption. If the LPUART uses a faster clock, it can communicate at a higher baud rate.

The LPUART can be served by the DMA controller.

3.21 SPI/I2S

Up to two SPI interfaces operating at up to 18 Mbit/s are embedded in HK32A040 MCUs. The SPI interfaces support master and slave modes and full-duplex or half-duplex communication. The 3-bit prescaler generates eight frequencies of master mode. Each frame can be configured to 4- to 16-bit.

Table 3-7 SPI1/SPI2 features

SPI Feature	SPI1/SPI2
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
I2S mode	Supported
TI mode	Supported

The standard I2S interfaces (with SPI multiplexed) provide four types of audio standards and can operate in

master/slave half-duplex communication mode. The I2S interfaces have dedicated signals for data synchronization. The data format can be 16-bit, 24-bit, or 32-bit and the I2S interfaces can operate with 16- or 32-bit resolution. The I2S interfaces can be set to an audio sampling frequency from 8 kHz to 192 kHz by the 8-bit programmable linear prescaler. When working in master mode, the I2S interface can output a clock of 256 times the sampling frequency to external audio components.

Table 3-8 I2S features

I2S Feature	I2S1/I2S2
Half-duplex mode	Supported
Master/Slave mode configurable	Supported
8-bit programmable linear prescaler	Supported
Data format programmable	Supported
Clock polarity programmable	Supported
I2S protocol	Supported
DMA transmission	Supported
Driving external audio components	Supported

3.22 GPIO

Each GPIO pin can be configured by software as an output pin (push-pull or open-drain), an input pin (floating, pull-up, or pull-down), or a peripheral alternate function pin. Most of the GPIO pins are shared by digital and analog peripherals. All GPIOs are high current capable. I/O alternate functions can be locked as needed to avoid unexpected writes to the I/O registers.

3.23 DMA

The 7-channel general-purpose DMA controller manages the data transfer from memories to memories, from devices to memories, and from memories to devices. The DMA controller supports circular buffer management, preventing the interrupt that occurs when the DMA controller reaches the end of the buffer.

Each channel is connected to a dedicated hardware DMA request and can be triggered by using software. The length, source, and destination of data to be transferred can be independently set by using the software. DMA can be used with the main peripherals, such as SPI, I2C, USART, TIMx, and ADC.

3.24 ADC

The 12-bit analog-to-digital converter (ADC) has the following functions:

- Up to 16 external channels and three internal channels (temperature sensor, reference voltage, and V_{BAT})
- Performs A/D conversion in single-channel or multi-channel scan mode. In scan mode, the conversion is automatically performed on a selected group of analog inputs.
- Can be served by the DMA controller
- Supports the sampling of 1/2 V_{BAT}
- Can be triggered by external trigger sources

The analog watchdog function can realize precise monitoring of one, some, or all selected channels. If the converted voltage exceeds the threshold set by the program, an interrupt is generated.

3.25 CAN

The CAN interface is compliant with Specification 2.0A and 2.0B (active). The highest bit rate is 1 Mbit/s. The CAN interface can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. The CAN interface has three transmit mailboxes and two 3-stage receive FIFOs. Each FIFO has 14 scalable filters.

3.26 RTC clock

In all operating modes of HK32A040 (including the Standby mode), a real-time clock (RTC) and five backup

registers are provided. The backup registers are 32-bit registers. They are used to store 20 bytes of user application data. The system reset and wakeup from the Standby mode do not reset backup registers.

The RTC has programmable periodic wakeup flags with the interrupt function.

The digital calibration feature compensates for deviation in the crystal oscillator accuracy.

After the RTC domain is reset, unexpected writes to all RTC registers are prevented.

As long as the power supply voltage of the MCU is within the operating range, the RTC keeps working in all modes of the MCU.

The RTC is an independent binary-coded decimal (BCD) timer/counter. It has the following features:

- Calendar with sub-seconds, seconds, minutes, hours (12- or 24-hour format), day of the week, day of the month, month, and year in BCD
- Automatic adjustment to the days of different months: 28 days, 29 days (leap year), 30 days, and 31 days. Adjustment of daylight saving time supported.
- Two programmable alarms that can wake up the MCU from Stop or Standby mode
- Programmable resolution and periodic wakeup from Stop or Standby mode
- Correction of 1 to 32,767 RTC clock pulses during runtime for synchronization between RTC and the main clock
- Reference clock detection: a more accurate secondary clock source (50 Hz or 60 Hz) that can improve calendar accuracy
- Digital calibration circuit with 0.95 ppm resolution for compensation of deviation in the crystal oscillator accuracy
- Two tamper detection pins with programmable filters. Wakeup from Stop or Standby mode when any tamper event is detected
- Timestamp feature used for storage of calendar content. The timestamp feature can be triggered by the event on the timestamp pin or by the tamper event. MCUs can be woken up from Stop or Standby mode when any timestamp event is detected.

The RTC clock source can be:

- 32.768 kHz external crystal oscillator LSE
- Low-power internal RC oscillator (typical frequency: 40 kHz) LSI
- HSE divided by 32

3.27 Information security

3.27.1 AES

HK32A040 integrates an Advanced Encryption Standard (AES) unit compliant with Federal Information Processing Standards 197 (FIPS 197).

- Supports the Electronic Code Book (ECB) mode
  - Supports the 128-bit, 192-bit, and 256-bit keys for encryption
  - Encryption computation time:
    - 128-bit key: 57 clock periods
    - 192-bit key: 67 clock periods
    - 256-bit key: 77 clock periods
  - Decryption computation time:

- 128-bit key: 57 clock periods
- 192-bit key: 67 clock periods
- 256-bit key: 77 clock periods

◦ After calling a single decryption operation, enter the decryption key in the AES_KEYRx register again.

- Supports the randomization of the AES clock by using TRNG.
- More convenient protection of the register content and easier resumption of the context when interrupts occur.
- Supports data transmission by using DMA (two DMA channels required)

3.27.2 Hash

The hash module is applicable to data authentication applications. It is compliant with the following protocols:

- Federal Information Processing Standards Publications 180-2 (FIPS PUB 180-2)
- Secure Hash Algorithm 256 (SHA-256)

The SHA-256 fast computation processing module is a slave peripheral attached to the AHB. It receives 32-bit data in words, half-words, bytes, and bits. The SHA-256 module only supports data stored in little-endian mode.

The input data in little-endian mode is automatically converted to the big-endian mode adopted by SHA-256. The last input data in little-endian mode is automatically padded to fit the digest minimum block size of 512 bits (16 × 32 bits). The digest of the whole message is obtained by adding the 32-bit words of the digests of consecutive message blocks. The data flow can be automatically controlled by using DMA.

3.27.3 TRNG

The true random number generator (TRNG) provides a 32-bit random number based on continuous analog noise when the CPU reads data. TRNG has the following features:

- Provides 32-bit random numbers generated by the analog generator.
- The interval at which two random numbers are generated is 40 TRNG_CLK periods.
- The entropy of TRNG is monitored for the identification of exceptional behaviors (generation of stable values or stable value sequences).
- TRNG can be disabled to reduce system power consumption.

3.28 CRC calculation unit

The cyclic redundancy check (CRC) is used to verify the integrity of data during transmission and storage. HK32A040 integrates a CRC hardware calculation unit. It is used to get a CRC code from an 8-, 16- or 32-bit data word by using a generator polynomial.

The CRC calculation unit computes a signature of the software during runtime. This signature is to be compared with a reference signature generated at link time and stored at a specified memory location.

3.29 EMACC

The Electric Motor Acceleration (EMACC) unit can be used on brushless direct current (BLDC) motors controlled by the field-oriented control (FOC) algorithm. EMACC accelerates the mathematical operations of motor drives. Mathematical operations can be completed at a speed higher than that of software-based mathematical operations while occupying less CPU resources. The EMACC-embedded MCUs support higher motor rotation speeds under the same CPU frequency.

The Coordinate Rotation Digital Computer (CORDIC) algorithm, Clarke, Park, and Inverse Park transformations, and proportional-integral-derivative (PID) control of the FOC algorithm are implemented by hardware, which reduces CPU usage and speeds up computing. Users input three-phase currents Ia, Ib, and Ic. After the processing

by EMACC, the input U_α and U_β of space vector pulse width modulation (SVPWM) can be obtained. EMACC decreases the time consumed by the FOC algorithm.

EMACC can significantly increase algorithm efficiency.

3.30 DVSQ calculation unit

The division and square root (DVSQ) calculation unit has the following features:

- Supports the 32-bit signed integer division (SDIV), unsigned integer division (UDIV), and root calculation.
  - The DVSQ calculation unit supports either the division or root calculation at one time.
  - The quotient and remainder of 32-bit SDIV and UDIV are updated to the corresponding register.
  - The MOD operation is supported in the division.
- High-precision root calculation can be selected for unsigned integer root calculation by using the software.
- In the streamlined design, a 2-bit calculation is completed in each clock period.
- The calculation time varies based on the calculation data.
- Supports divide-by-zero interrupt and overflow interrupt.

3.31 CLU

HK32A040 embeds a configurable logic module (CLM). The CLM offers several programmable digital logic blocks which can operate without using the CPU resource. The CLM consists of four dedicated configurable logic units (CLUs) for configurable synchronous and asynchronous Boolean logic operations. The input of each CLU can be an internal or external signal, and the output of each CLU can be connected to an I/O pin or the input of a specified peripheral.

The CLU has the following features:

- Each CLU supports 65,536 combinations of logical functions, such as AND, OR, XOR, or multiplexing, and has a clock trigger used for synchronization.
- Synchronous and asynchronous operations are supported.
- CLUs can be cascaded to realize more complex logical functions.
- CLUs can be used in conjunction with timers or serial peripherals such as UART and SPI.
- CLUs can be used to synchronize and trigger multiple on-chip resources (such as ADC and timers).
- The output of asynchronous operations can be used to wake up the MCU from low-power modes.

3.32 Voltage comparator

HK32A040 has three built-in voltage comparators: COMP1, COMP2, and COMP3. The three comparators can be used as independent window comparators or used together.

3.33 Internal reference voltage

The internal reference voltage V_{REFINT} provides a stable voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The V_{REFINT} memory address can only be read.

Table 3-9 Internal voltage benchmark value

Value Name	Description	Memory Address
V_{REFINT_CAL}	The original data obtained under 25°C temperature. V_{DDA} = 3.3 V (±10 mV)	0x1FFF F7BA-0x1FFF F7BB

3.34 Temperature sensor

The temperature sensor generates a voltage that varies linearly based on the temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output

voltage into a digital value.

The temperature sensor is accurate, but it still needs to be calibrated to ensure the accuracy of overall temperature measurement. The temperature sensor offset of different MCUs varies based on the manufacturing processes of the MCUs. Therefore, uncalibrated temperature sensors are suited only for applications that measure temperature changes. All HK32A040 MCUs are factory-calibrated to ensure the measurement accuracy of the temperature sensors. The factory calibration data of temperature sensors is stored in the system memory and can only be read.

3.35 96-bit UID

The 96-bit unique identifier (UID) provides a reference number for each HK32A040 MCU. The UID is unique in any circumstances. You are not allowed to modify the UID. The 96-bit UID can be read in bytes (8 bits), half words (16 bits), or words (32 bits) for different applications. The 96-bit UID can be used:

- As a serial number. For example, as a USB string serial number or used for other terminal applications.
- As a security key. When programming the Flash, use the UID together with software encryption and decryption algorithms to enhance the security of code in the Flash.
- To activate the boot processes that have the security mechanism.

3.36 Debug port

Based on the ARM SWJ-DP embedded in HK32A040, SWDIO/SWCLK functions are available.

4 Electrical characteristics

4.1 Absolute maximum values

The absolute maximum values are stress test values within a short period.

Note:

- Do not use the device in conditions equal to or exceeding the absolute maximum values.
- Stresses beyond the absolute maximum values listed in Table 4-1 to Table 4-3 may cause permanent damage to the device.
- If the device works under the maximum values for extended periods, its reliability may deteriorate.

4.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
$V_{DD} – V_{SS}$	External main power supply voltage (including V_{DDA} and V_{DD})	–0.3	3.75	V
V_{IN}	Input voltage on pins	$V_{SS} – 0.3$	V_{DD}	
$\|\Delta V_{DDx}\|$	Variation between different power pins	-	50	mV
$\|V_{SSX} – V_{SS}\|$	Variation between different ground pins	-	50	

4.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} (source)(1)	100	mA
I_{VSS}	Total current from V_{SS} (sink)(1)	–100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	–40	
$I_{INJ(PIN)}$(2)	Injected current on pins(3)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	±25	

(1). All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must be connected to the external power supply within the permitted range all the time.

(2). Negative injected current causes the analog performance of the device to fluctuate.

(3). When V_{IN} is larger than V_{DD}, a positive injected current is induced; when V_{IN} is smaller than V_{SS}, a negative injected current is induced. The injected current must be within the permitted range.

(4). If multiple I/Os have current injection simultaneously, the maximum $\sum I_{INJ(PIN)}$ is the sum of the absolute instantaneous values of positive and negative injected currents.

4.1.3 Temperature characteristics

Table 4-3 Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	

4.2 Operating conditions

4.2.1 Recommended operating conditions

Table 4-4 Recommended operating conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	0	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	0	96	
f_{PCLK2}	Internal APB2 clock frequency	0	96	
V_{DD}	Standard operating voltage	1.8	3.6	V

Symbol	Description	Min	Max	Unit
V_{DDA}(1)	Analog operating voltage	1.8	3.6	V
T	Operating temperature	–40	125	°C

(1). V_{DDA} can be lower than V_{DD}. For example, V_{DD} = 3.3 V, V_{DDA} = 2.5 V.

4.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (V_{DD} rising edge)	PLS[2:0] = 000	2.10	2.23	2.36	V
		PLS[2:0] = 001	2.19	2.33	2.47	
		PLS[2:0] = 010	2.31	2.43	2.55	
		PLS[2:0] = 011	2.40	2.53	2.66	
		PLS[2:0] = 100	2.49	2.63	2.77	
		PLS[2:0] = 101	2.60	2.74	2.88	
		PLS[2:0] = 110	2.68	2.84	3.00	
		PLS[2:0] = 111	2.80	2.94	3.08	
	Programmable voltage detector level selection (V_{DD} falling edge)	PLS[2:0] = 000	2.11	2.21	2.31	
		PLS[2:0] = 001	2.21	2.31	2.41	
		PLS[2:0] = 010	2.31	2.41	2.51	
		PLS[2:0] = 011	2.40	2.51	2.62	
		PLS[2:0] = 100	2.50	2.61	2.72	
		PLS[2:0] = 101	2.59	2.71	2.83	
		PLS[2:0] = 110	2.69	2.81	2.93	
		PLS[2:0] = 111	2.78	2.91	3.04	

4.2.3 POR/PDR characteristics

Table 4-6 POR/PDR characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	POR/PDR threshold	Falling edge(2)	-	1.70	-	V
		Rising edge	-	1.64	-	V
$V_{PDRhyst}$	PDR hysteresis	-	-	60	-	mV
$t_{RSTTEMPO}$(3)	Reset duration	-	3.0	3.50	4.50	ms

(1). PDR is based on the monitoring of V_{DD} and V_{DDA}. POR is based on the monitoring of only V_{DD}.

(2). The actual performance value is guaranteed to be smaller than the minimum $V_{POR/PDR}$ value.

(3). The value is guaranteed in design.

4.2.4 Internal reference voltage

Table 4-7 Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40°C to 125°C	1.15	1.2	1.23	V

4.2.5 Operating current characteristics

Table 4-8 Operating current characteristics

Mode	Condition	Parameter	V_{DD} = 3.3 V				Unit
			–40°C	25°C	85°C	105°C	
Run	HCLK = 96 MHz, seven wait states for FLASH_LATENCY, APB clock enabled	Operating current	10.636	9.777	10.301	10.743	mA

Mode	Condition	Parameter	V_{DD} = 3.3 V				Unit
			–40°C	25°C	85°C	105°C	
	HCLK = 96 MHz, seven wait states for FLASH_LATENCY, APB clock disabled		6.933	6.062	6.578	7.008	mA
	HCLK = HSE (8 MHz), zero wait states for FLASH_LATENCY, APB clock enabled		2.857	1.950	2.433	2.844	mA
	HCLK = HSE (8 MHz), zero wait states for FLASH_LATENCY, APB clock disabled		2.543	1.641	2.122	2.533	mA
	HCLK = LSE (32.768 kHz), zero wait states for FLASH_LATENCY, APB clock enabled		0.995	1.080	1.567	1.912	mA
	HCLK = LSE (32.768 kHz), zero wait states for FLASH_LATENCY, APB clock disabled		0.994	1.078	1.565	1.908	mA
	HCLK = LSI (40 kHz), zero wait states for FLASH_LATENCY, APB clock enabled		0.996	1.080	1.517	1.914	mA
	HCLK = LSI (40 kHz), zero wait states for FLASH_LATENCY, APB clock disabled		0.994	1.079	1.514	1.909	mA
Sleep	HCLK = HSE (96 MHz), APB clock disabled	Operating current	5.676	4.786	5.286	5.710	mA
	HCLK = HSI (8 MHz), APB clock disabled	Operating current	1.275	1.363	1.796	2.191	mA
		Wakeup time	-	4.7	-	-	µs
	HCLK = LSE (32.768 kHz), APB clock disabled	Operating current	0.993	1.077	1.561	1.905	mA
	HCLK = LSI (40 kHz), APB clock disabled	Operating current	0.993	1.077	1.510	1.905	mA
Stop	LDO operating at full speed HSE/HSI/LSE disabled IWDG disabled	Operating current	0.628	0.688	1.099	1.487	mA
		Wakeup time	-	20	-	-	µs
	LDO in the low-power state HSE/HSI/LSE disabled IWDG disabled	Operating current	18.227	60.026	393.768	708.269	µA
		Wakeup time	-	132	-	-	µs
Standby	LSI and IWDG enabled	Operating current	1.834	2.254	6.004	10.898	µA
		Wakeup time	-	152	-	-	µs
	LSI enabled, IWDG disabled	Operating current	1.829	2.253	5.993	10.883	µA
		Wakeup time	-	152	-	-	µs
	All oscillators disabled	Operating current	1.154	1.642	5.393	10.285	µA
		Wakeup time	-	152	-	-	µs
Shutdown	LSE enabled and RTC running (BKPPDS = 0)	Operating current	1.465	2.002	165.692	10.606	µA
		Wakeup time	-	96	-	-	µs
	LSE disabled and RTC stopped (BKPPDS = 0)	Operating current	1.152	1.633	5.306	10.112	µA
		Wakeup time	-	96	-	-	µs

Mode	Condition	Parameter	V_{DD} = 3.3 V				Unit
			–40°C	25°C	85°C	105°C	
	LSE and RTC disabled (BKPPDS = 1)	Operating current	0.319	0.406	1.027	2.446	μA
		Wakeup time	-	364	-	-	μs

4.2.6 HSE clock characteristics

Table 4-9 HSE clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	2	-	MΩ
$T_{su\ (HSE)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	3	-	4	μs
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (R_S)	-	-	12.5	-	pF
$I_{DD\ (HSE)}$	HSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12.5 pF@8 MHz	60	100	300	μA

HK32A040 integrates an HSE negative feedback circuit supplied with a resonator. The following oscillator circuit outside the chip is recommended:

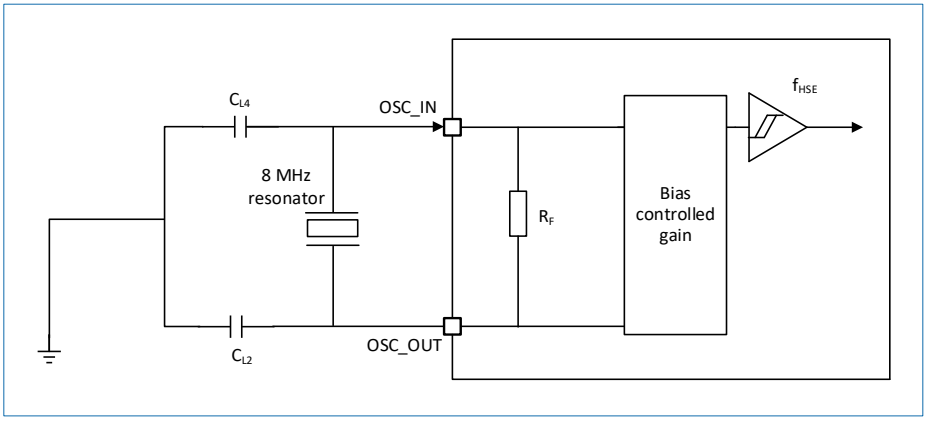

Figure 4-1 HSE crystal oscillator circuit with negative feedback

Alternatively, HK32A040 can be clocked from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 4-10 Characteristics of the input HSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	1	8	25	MHz
V_{HSEH}	High level voltage on the OSC_IN input pin	-	0.7 × V_{DD}	-	V_{DD}	V
V_{HSEL}	Low level voltage on the OSC_IN input pin	-	V_{SS}	-	0.3 × V_{DD}	V
$t_{H(HSE)}/t_{L(HSE)}$	High or low time of OSC_IN	-	5	-	-	ns
$t_{r(HSE)}/t_{f(HSE)}$	Rise or fall time of OSC_IN	-	-	-	20	ns
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

4.2.7 LSE clock characteristics

Table 4-11 LSE clock characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	2	-	MΩ
$T_{su\ (LSE)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	2000	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12.5	-	pF
I_2	LSE driving current	-	-	400	-	nA
$I_{DD(LSE)}$	LSE oscillator power consumption	Normal operation: V_{DD} = 3.3 V, CL = 12.5 pF@8 MHz	-	80	100	μA

HK32A040 integrates an LSE negative feedback circuit supplied with a resonator. The following oscillator circuit outside the chip is recommended:

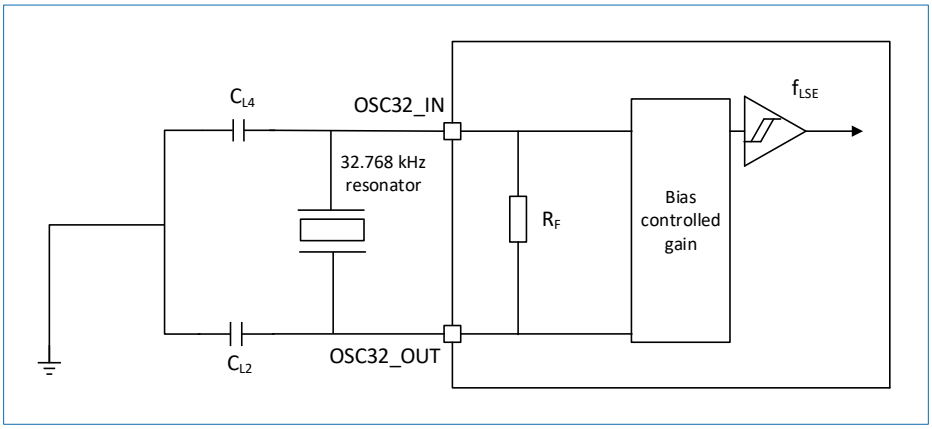

Figure 4-2 LSE crystal oscillator circuit with negative feedback

Alternatively, HK32A040 can be clocked from the OSC32_IN pin. The following table lists the requirements for this clock signal.

Table 4-12 Characteristics of the input LSE clock

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	High level voltage on the OSC_IN input pin	-	0.7 × V_{DD}	-	V_{DD}	V
V_{LSEL}	Low level voltage on the OSC_IN input pin	-	V_{SS}	-	0.3 × V_{DD}	V
$t_{H(LSE)}/t_{L(LSE)}$	High or low time of OSC_IN	-	450	-	-	ns
$t_{r(LSE)}/t_{f(LSE)}$	Rise or fall time of OSC_IN	-	-	-	50	ns
$C_{in(LSE)}$	OSC_IN input capacitance	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%

4.2.8 HSI clock characteristics

Table 4-13 HSI clock characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
$ACC_{(HSI)}$	HSI oscillator accuracy	RCC_CR register calibration completed by the user		-	-	1	
		Factory calibrated	T_A = –40°C to +125°C	–1.5	-	1.5	%
			T_A = –40°C to +85°C	–1.0	-	1.0	
			T_A = 0°C to +70°C	–1.0	-	1.0	
$T_{su\ (HSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$		3	-	4	μs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{DD(HSI)}$	Oscillator power consumption	-	-	80	100	μA

4.2.9 LSI clock characteristics

Table 4-14 LSI clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	34	40	46	kHz
$T_{su\ (LSI)}$	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	150	-	μs
$I_{DD(LSI)}$	Oscillator power consumption	-	-	0.5	-	μA

4.2.10 PLL characteristics

Table 4-15 PLL characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	Input clock frequency	2	8.0	80	MHz
	Input clock duty cycle	40	-	60	%
f_{PLL_OUT}	Output clock frequency	16	-	120	MHz
t_{LOCK}	PLL lock time	-	80	120	μs
Jitter	Cycle-to-cycle jitter	-	5	13	ps

4.2.11 Flash memory characteristics

Table 4-16 Flash memory characteristics

Symbol	Parameter	Min	Typ(1)	Max	Unit
T_{PROG}	Half word programming time	-	42	-	μs
	One-word programming time	-	42	-	μs
T_{ERASE}	Half page erase time	-	3.7	-	ms
	Page erase time	-	7.45	-	ms
	Mass erase time	-	190	-	ms
IDD_{PROG}	Programming current	-	1.5	5	mA
IDD_{ERASE}	Page/Mass erase current	-	0.9	2	mA
IDD_{READ}	Supply current@24 MHz (read mode)	-	2.5	-	mA
N_{END}	Endurance	100,000	-	-	Cycles
t_{RET}	Data retention	10	-	-	Years

(1). The typical values are obtained in the following conditions: 1.5 V, TT process corner, 25°C.

4.2.12 I/O pin input characteristics

Table 4-17 I/O pin input direct current characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD} = 3.3 V	1.82	-	-	V
V_{IL}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.3	V
V_{IHhys}	Input high level voltage	V_{DD} = 3.3 V	1.64	-	-	V
V_{ILhys}	Input low level voltage	V_{DD} = 3.3 V	-	-	1.44	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	-	160	-	mV
I_{lkg}	Input leakage current	V_{DD} = 3.3 V; 0 < V_{IN} < 3.3 V	-	-	0.01	μA
		V_{DD} = 3.3 V; V_{IN} = 5 V	-	-	1.65	μA
R_{PU}	Pull-up resistor	V_{IN} = V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down resistor	V_{IN} = V_{DD}	-	34	-	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

4.2.13 I/O pin output characteristics

Table 4-18 I/O pin output alternating current characteristics

Mode OSPEEDy[1:0]	Symbol	Parameter	Condition	Min	Typ	Max	Unit
x0	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	-	9.50	-	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	22.7	-	ns
01	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	-	5.0	-	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	6.70	-	ns
11	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	-	4.25	-	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	5.00	-	ns
OSPEEDy[1:0] = 11 and UHDy = 1	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	-	3.35	-	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	3.85	-	ns

4.2.14 NRST pin characteristics

The NRST pin is connected to a pull-up resistor. Its peripheral application circuit can connect to an external RC circuit or no circuit.

Table 4-19 NRST pin input characteristics

Symbol	Parameter	Min	Max	Unit
T_{Noise}	Low level ignored duration	-	50	ns

4.2.15 TIM timer characteristics

Table 4-20 TIM characteristics

Symbol	Condition	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}/2$(1)	MHz

(1). $f_{TIMxCLK}$ = 96 MHz

4.2.16 EMACC characteristics

Table 4-21 Motor drive frequency characteristics

System Clock	ADC Clock	Min	Typ	Max	Unit
48 MHz	$f_{PCLK} = f_{apb}$; $f_{ADC} = f_{PCLK}/4$	-	20	21±0.3	kHz
72 MHz	$f_{PCLK} = f_{apb;}$ $f_{ADC} = f_{PCLK}/4$	-	24	25±0.3	kHz
96 MHz	$f_{PCLK} = f_{apb}/2$; $f_{ADC} = f_{PCLK}/4$	-	28	29±0.3	kHz

Table 4-22 Comparison between the software and the FOC algorithm with EMACC

Test Condition	Electrical Angle	Coordinate System Conversion	Software-based SVPWM	Total Time Consumption	Unit
System clock: 48 MHz (software-based motor library)	12	13	7	32	µs
System clock: 48 MHz (EMACC-powered motor library)	12	2.8	7	21.8	µs

4.2.17 ADC characteristics

Table 4-23 ADC characteristics

Item	Description	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog power supply voltage when ADC is enabled	-	2.4	-	3.6	V
INL	Integral non linearity (maximum difference between the actual conversion point and the end point correlation line)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1	–2 to 3	LSB
DNL	Differential non linearity (maximum difference between the actual step and the ideal step)	f_{ADC} = 14 MHz R_{AIN} < 10 kΩ Test after calibration V_{DDA} = 2.4 V to 3.6 V	-	±1	–2 to 3	LSB
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S (1)	Sampling frequency	-	0.05		1	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-		17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (1)	External input impedance	For details, see Table 4-24.	-	-	60	kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (1)	Sampling and hold capacitor	-	-	-	5	pF
t_{CAL}(2)	ADC calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	8.3			$1/f_{ADC}$
t_{latr}	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.188	-	0.259	µs
$Jitter_{ADC}$	Jitters triggered by ADC conversions	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S(1)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
		-	1.5		239.5	$1/f_{ADC}$
t_{STAB} (1)	Sampling stable time	-	14			µs
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_{CONV} = sampling time ts + conversion time 12.5)			$1/f_{ADC}$

(1). The value is guaranteed in design but not tested in production.

(2). The values are measured based on the ADC clock. The register access latency is not taken into account.

The calculation formula of the maximum input impedance R_{AIN}:

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The value of N (resolution) is 12.

The allowable error can be lower than 1/4 least significant bit (LSB).

Table 4-24 Maximum input impedance values (f_{ADC} = 14 MHz)

Sampling Cycles (Cycles)	Sampling Time tS (µs)	Maximum Input Impedance (kΩ)
1.5	0.11	1.21
7.5	0.54	10.05
13.5	0.96	18.88
28.5	2.04	40.97
41.5	2.96	60.12
55.5	3.96	80.74
71.5	5.11	-
239.5	17.1	-

Table 4-25 ADC accuracy

Symbol	Parameter	Test Condition	Typ	Max	Unit
ET	Total unadjusted error(1)	SystemCLK = 56 MHz	–1 to 1	–2 to 3	LSB
EO	Offset error(2)	ADCCLK = 14 MHz	1	0 to 2	
EG	Gain error(3)	Input impedance < 10 kΩ	3	1 to 3	
ED	Differential linearity error(4)	V_{DD} = V_{DDA} = 3.305 V	–1 to 1	–2 to 3	
EL	Integral linearity error(5)	Test after ADC calibration	–1 to 1	–2 to 3	

(1). Total unadjusted error: The maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3). Gain error: The deviation between the last ideal conversion and the last actual conversion.

(4). Differential linearity error: The maximum deviation between the actual step and the ideal step.

(5). Integral linearity error: The maximum deviation between any actual transition and the endpoint correlation line.

Note:

- The ADC direct current accuracy values are measured after internal calibration.
- ADC accuracy and negative current injection: Avoid injecting negative currents on any standard (non-robust) analog input pin. Otherwise, the accuracy of the conversion being performed on another analog input pin is greatly reduced. It is recommended that you add a Schottky diode (pin to ground) to the standard analog pins on which negative currents may be injected.
- With restricted V_{DDA}, frequency, and temperature ranges, better ADC performance can be achieved.
- The data is based on characterization but not tested in production.

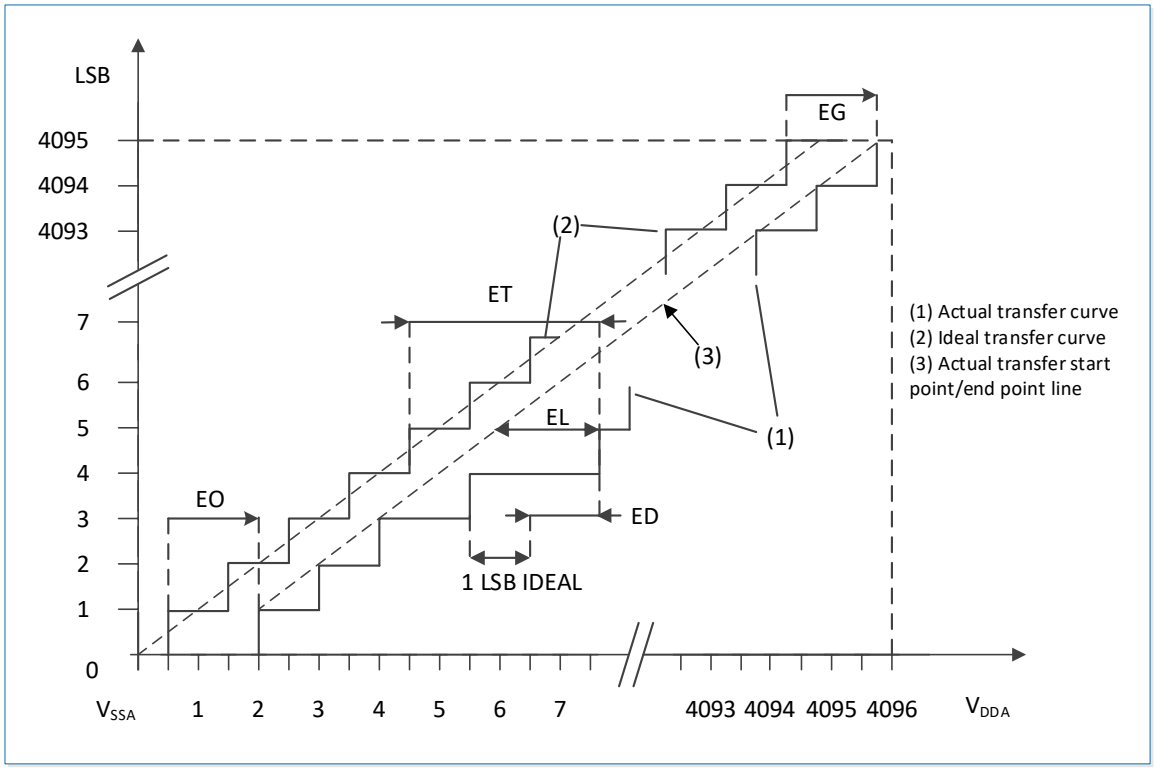

Figure 4-3 ADC accuracy characteristics

Note: For the explanations of EO, ET, EG, EL, and ED, see Table 4-25.

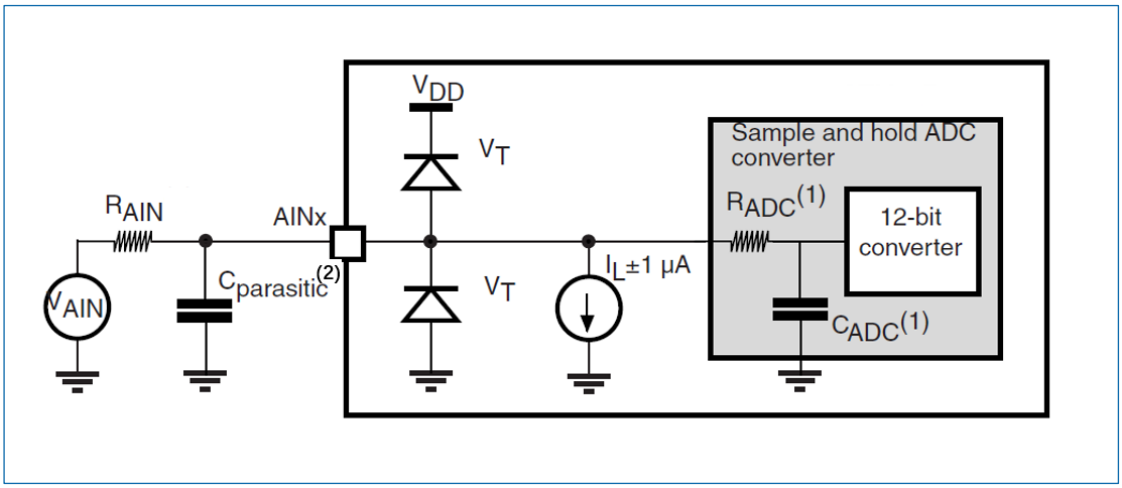

Figure 4-4 Typical connection diagram of ADC

(1). For the ADC characteristics of R_{ADC} and C_{ADC}, see Table 4-23.

(2). $C_{parasitic}$ equals the PCB capacitance (decided by soldering and the PCB layout quality) plus the pad capacitance (about 7 pF). A high $C_{parasitic}$ value would reduce conversion accuracy, so f_{ADC} should be reduced.

PCB design recommendation for ADC sampling: The power supply decoupling should be performed by following section "5 Typical circuitry". To ensure the ADC conversion accuracy, the 10 nF capacitors should be ceramic and placed close to the chip.

4.2.18 Temperature sensor characteristics

Table 4-26 Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L	Temperature sensor linearity error	-	-	±1	±3	°C
V_{25}	Output voltage	25°C	0.85	0.89	0.93	V
Avg_Slope	Temperature sensor slope	-	-	3	-	mV/°C

5 Typical circuitry

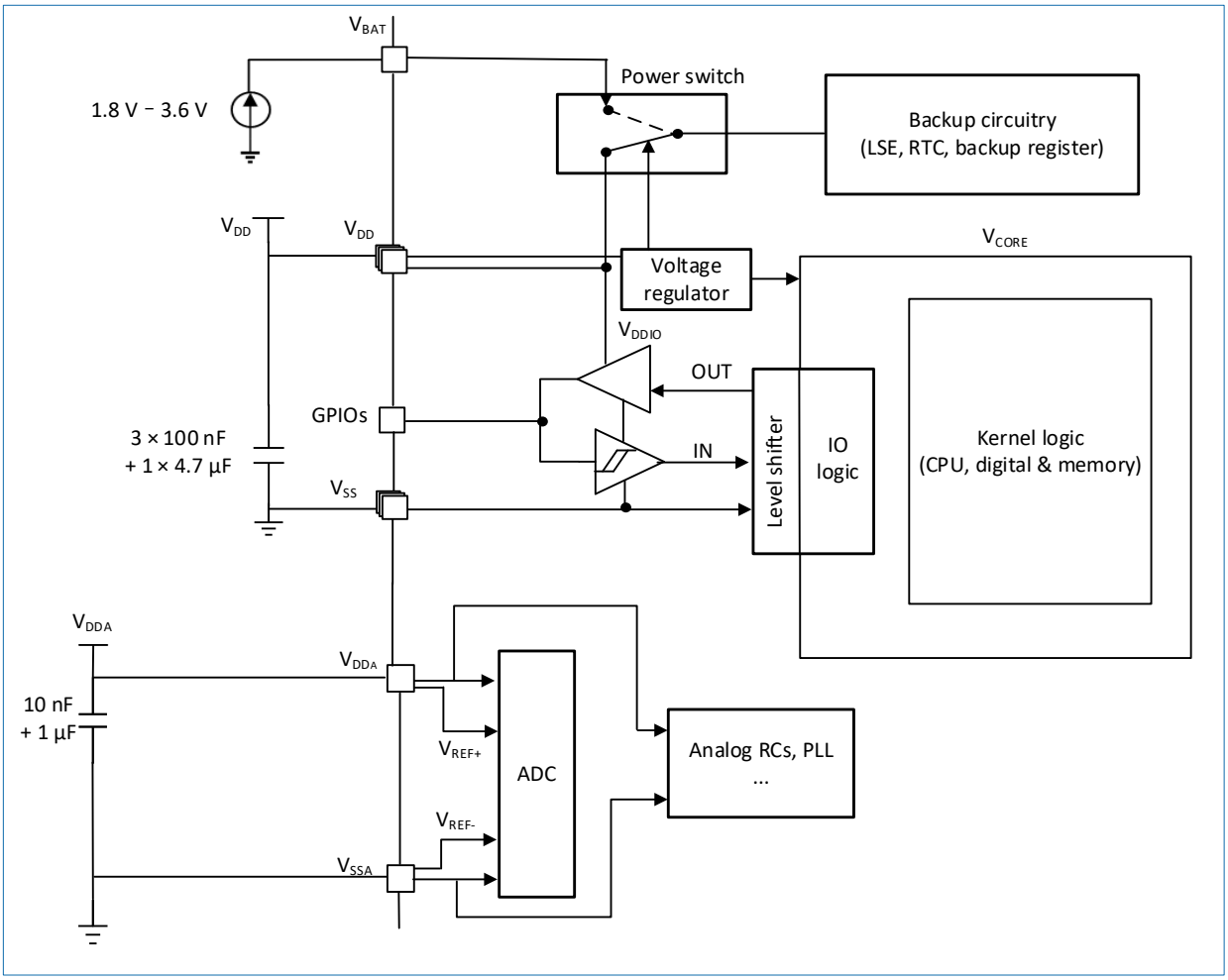

Figure 5-1 Power supply reference circuitry

6 Pinouts and pin descriptions

HK32A040 MCUs are delivered in LQFP64, LQFP48, QFN32, and QFN28 packages. The pinouts of the packages are as follows:

6.1 LQFP64

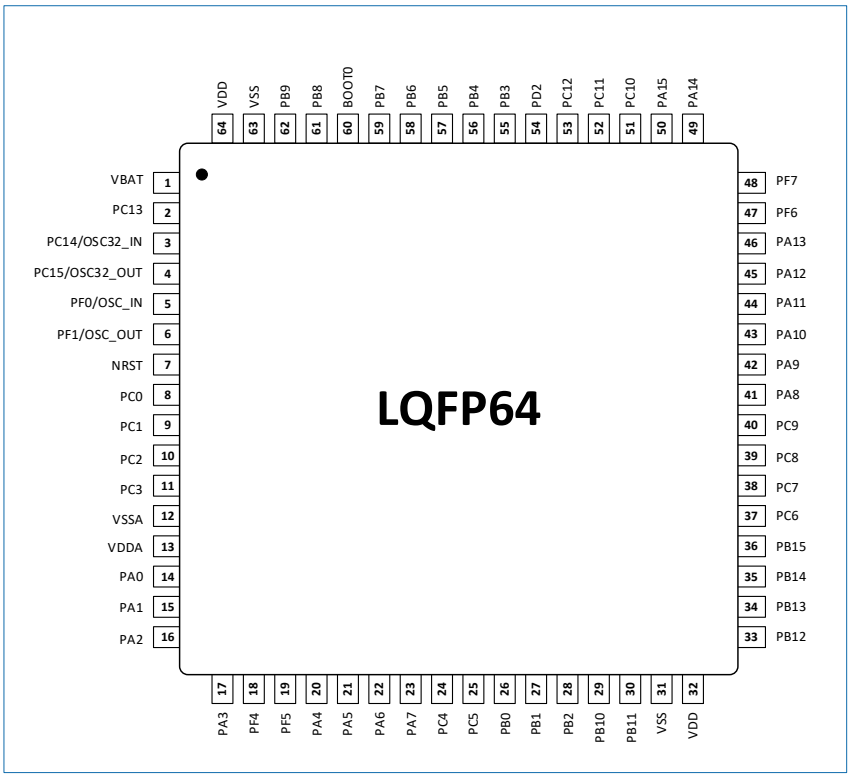

Figure 6-1 LQFP64 (HK32A040RBT3) pinout

6.2 LQFP48

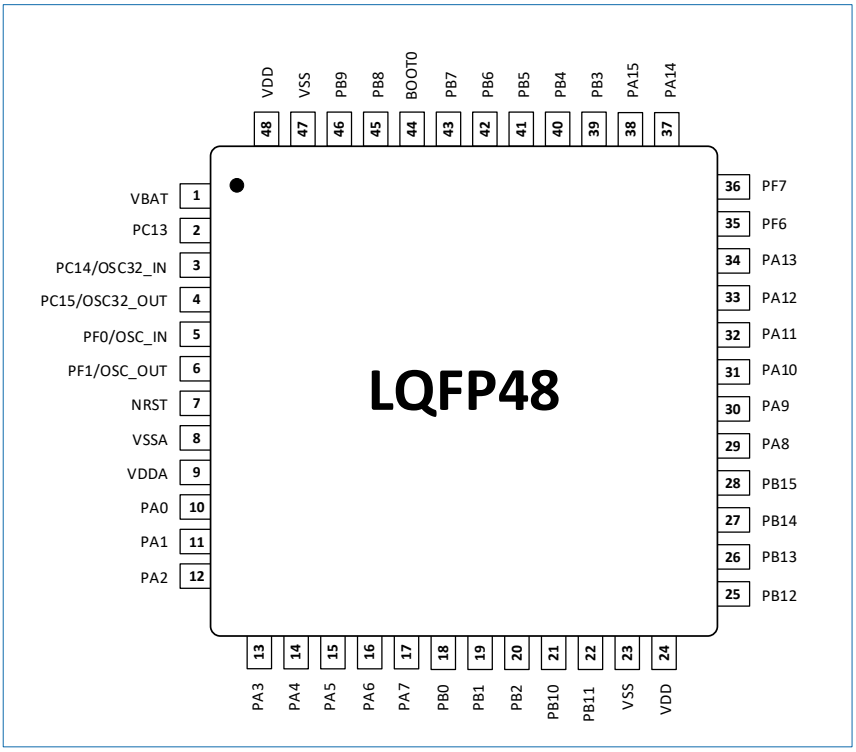

Figure 6-2 LQFP48 (HK32A040CBT3) pinout

6.3 QFN32

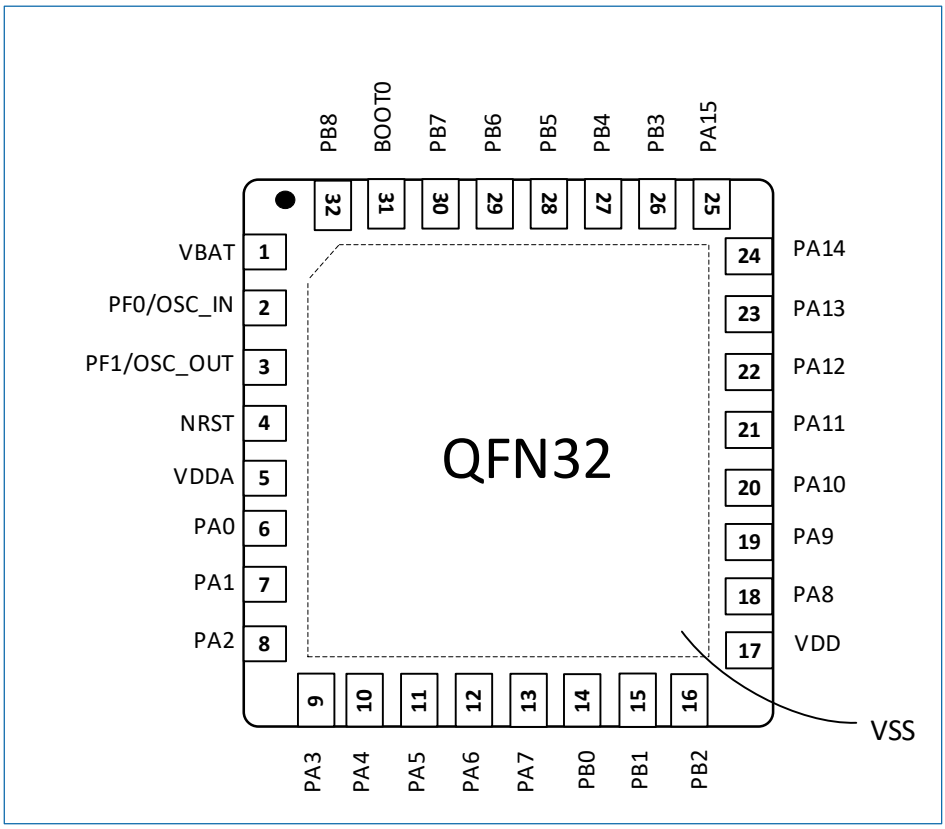

Figure 6-3 QFN32 (HK32A040KBU3) pinout

6.4 QFN28

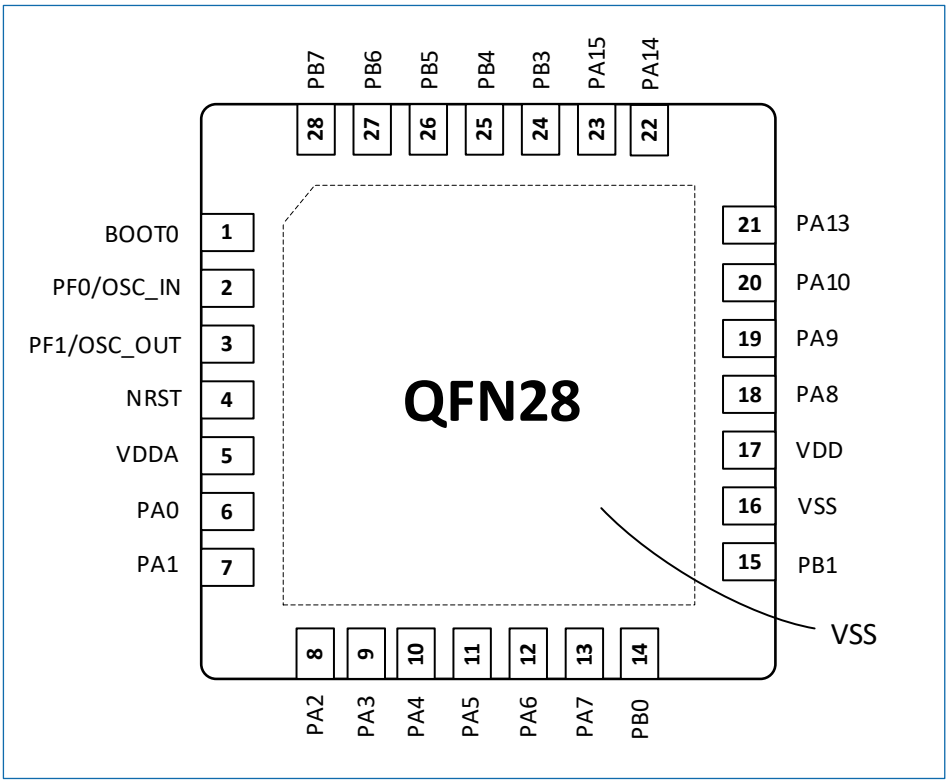

Figure 6-4 QFN28 (HK32A040GBU3) pinout

6.5 Pin descriptions

Table 6-1 Pin description of each package

LQFP64	LQFP48	QFN32	QFN28	Pin Name	Type(1)	5 V-tolerant	Alternate Function	Additional Function
1	1	1	-	VBAT	S		Battery power supply input	
2	2	-	-	PC13	I/O	FT(4)	-	RTC_TAMP1 RTC_TS RTC_OUT WKUP2 EXTI13
3	3	-	-	PC14	I/O	FT	-	OSC32_IN EXTI14
4	4	-	-	PC15	I/O	FT	-	OSC32_OUT EXTI15
5	5	2	2	PF0	I/O	FT	I2C1_SDA	OSC_IN
6	6	3	3	PF1	I/O	FT	I2C1_SCL	OSC_OUT
7	7	4	4	NRST	I/O	-	Reset input/internal reset output, active low	
8	-	-	-	PC0	I/O	-	-	ADC_IN10 EXTI0
9	-	-	-	PC1	I/O	-	-	ADC_IN11 EXTI1
10	-	-	-	PC2	I/O	-	SPI2_MISO I2S2_MCK	ADC_IN12 EXTI2
11	-	-	-	PC3	I/O	-	SPI2_MOSI I2S2_SD	ADC_IN13 EXTI3
12	8	-	-	VSSA	S	-	Analog ground	
13	9	5	5	VDDA	S	-	Analog power supply	
14	10	6	6	PA0	I/O	-	USART1_CTS USART2_CTS TIM2_CH1 TIM2_ETR CMP1_ININ1/CMP1_OUT LPUART_RX CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN0 WKUP1 RTC_TAMP2 EXTCLK4 EXTI0
15	11	7	7	PA1	I/O	-	USART1_RTS/USART1_DE USART2_RTS/USART2_DE TIM15_CH1N TIM2_CH2 CMP1_INP1 CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN1 EXTI1
16	12	8	8	PA2	I/O	-	USART1_TX USART2_TX TIM15_CH1 TIM2_CH3 CMP2_INN1 CMP2_OUT CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN2 EXTI2
17	13	9	9	PA3	I/O	-	USART1_RX USART2_RX TIM15_CH2 TIM2_CH4 CMP2_INP1 CLU0_O	ADC_IN3 EXTI3

LQFP64	LQFP48	QFN32	QFN28	Pin Name	Type(1)	5 V-tolerant	Alternate Function	Additional Function
							CLU1_O CLU2_O CLU3_O	
18	-	-	-	PF4	I/O	-	-	ADC_AIN17 EXTI4
19	-	-	-	PF5	I/O	FT	-	EXTI5
20	14	10	10	PA4	I/O	-	SPI1_NSS I2S1_WS USART1_CK USART2_CK TIM14_CH1 CMP1_INN2 CMP2_INN2 CMP3_INN2 CLU0_O CLU1_O CLU2_O CLU3_O DAC1_AOUT0	ADC_IN4 EXTCLK1 EXTI4
21	15	11	11	PA5	I/O	-	SPI1_SCK I2S1_CK TIM2_CH1 TIM2_ETR CMP1_INN3 CMP2_INN3 CMP3_INN1 CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN5 EXTI5
22	16	12	12	PA6	I/O	-	SPI1_MISO I2S1_MCK TIM3_CH1 TIM1_BKIN TIM16_CH1 CMP1_OUT LPUART_CTS CAN_RX CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN6 EXTI6
23	17	13	13	PA7	I/O	-	SPI1_MOSI I2S1_SD TIM3_CH2 TIM14_CH1 TIM1_CH1N TIM17_CH1 RCC_MCO CMP2_OUT CAN_TX CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN7 EXTI7
24	-	-	-	PC4	I/O	-	LPUART_TX	ADC_IN14 EXTI4
25	-	-	-	PC5	I/O	-	LPUART_RX	ADC_IN15 EXTI5
26	18	14	14	PB0	I/O	-	TIM3_CH3 TIM1_CH2N CMP3_INN3	ADC_IN8 EXTI0

LQFP64	LQFP48	QFN32	QFN28	Pin Name	Type(1)	5 V-tolerant	Alternate Function	Additional Function
27	19	15	15	PB1	I/O		TIM3_CH4 TIM14_CH1 TIM1_CH3N CMP3_INN1/CMP3_OUT LPUART_RTS/LPUART_DE CLU0_O CLU1_O CLU2_O CLU3_O	ADC_IN9 EXTI1
28	20	16	-	PB2	I/O	FT	I2C1_SMBA I2C2_SMBA	EXTI2
29	21	-	-	PB10	I/O	FT	I2C1_SCL I2C2_SCL SPI2_SCK I2S2_CK TIM2_CH3 LPUART_TX	EXTI10
30	22	-	-	PB11	I/O	FT	I2C1_SDA I2C2_SDA TIM2_CH4 LPUART_RX	EXTI11
31	23	-	16	VSS	S	-	Ground	
32	24	17	17	VDD	S	-	Digital power supply	
33	25	-	-	PB12	I/O	FT	SPI1_NSS I2S1_WS SPI2_NSS I2S2_WS TIM1_BKIN TIM15_BKIN I2C2_SMBA LPUART_RTS/LPUART_DE	EXTI12
34	26	-	-	PB13	I/O	FT	SPI1_SCK I2S1_CK SPI2_SCK I2S2_CK TIM1_CH1N I2C2_SCL LPUART_CTS	EXTI13
35	27	-	-	PB14	I/O	FT	SPI1_MISO I2S1_MCK SPI2_MISO I2S2_MCK TIM1_CH2N TIM15_CH1 I2C2_SDA LPUART_RTS/LPUART_DE	EXTI14
36	28	-	-	PB15	I/O	FT	SPI1_MOSI I2S1_SD SPI2_MOSI I2S2_SD TIM1_CH3N TIM15_CH1N TIM15_CH2	EXTI15 RTC_REFIN
37	-	-	-	PC6	I/O	FT	TIM3_CH1	EXTI6
38	-	-	-	PC7	I/O	FT	TIM3_CH2	EXTI7
39	-	-	-	PC8	I/O	FT	TIM3_CH3	EXTI8
40	-	-	-	PC9	I/O	FT	TIM3_CH4	EXTI9
41	29	18	18	PA8	I/O	FT	USART1_CK TIM1_CH1 RCC_MCO LPUART_RX	WKUP3 EXTI8
42	30	19	19	PA9	I/O	FT	USART1_TX	EXTI9

LQFP64	LQFP48	QFN32	QFN28	Pin Name	Type(1)	5 V-tolerant	Alternate Function	Additional Function
							TIM1_CH2 TIM15_BKIN I2C1_SCL RCC_MCO LPUART_TX CAN_RX	
43	31	20	20	PA10	I/O	FT	USART1_RX TIM1_CH3 TIM17_BKIN I2C1_SDA LPUART_RX CAN_TX	EXTI10
44	32	21	-	PA11	I/O	-	USART1_CTS TIM1_CH4 I2C2_SCL CAN_RX CMP1_OUT CLU0_O CLU1_O CLU2_O CLU3_O	EXTI11
45	33	22	-	PA12	I/O	-	USART1_RTS/USART1_DE TIM1_ETR I2C2_SDA CAN_TX CMP2_OUT CLU0_O CLU1_O CLU2_O CLU3_O	EXTI12
46	34	23	21	PA13	I/O	FT	IRTIM_IROUT SWDIO CAN_RX LPUART_RX CMP3_OUT CLU0_O CLU1_O CLU2_O CLU3_O	EXTCLK2 EXTI13
47	35	-	-	PF6	I/O	FT	I2C1_SCL I2C2_SCL	EXTI6
48	36	-	-	PF7	I/O	FT	I2C1_SDA I2C2_SDA	EXTI7
49	37	24	22	PA14	I/O	FT	USART1_TX USART2_TX SWCLK CAN_TX LPUART_TX CLU0_O CLU1_O CLU2_O CLU3_O	EXTCLK3 EXTI14
50	38	25	23	PA15	I/O	FT	SPI1_NSS I2S1_WS USART1_RX USART2_RX TIM2_CH1 TIM2_ETR	EXTI15
51	-	-	-	PC10	I/O	FT	LPUAR_TX CLU0_O CLU1_O CLU2_O	EXTI10

LQFP64	LQFP48	QFN32	QFN28	Pin Name	Type(1)	5 V-tolerant	Alternate Function	Additional Function
							CLU3_O	
52	-	-	-	PC11	I/O	FT	CAN_RX LPUART_RX CLU0_O CLU1_O CLU2_O CLU3_O	EXTI11
53	-	-	-	PC12	I/O	FT	CAN_TX CLU0_O CLU1_O CLU2_O CLU3_O	EXTI12
54	-	-	-	PD2	I/O	FT	TIM3_ETR LPUART_DE/LPUART_RTS	EXTI2
55	39	26	24	PB3	I/O	FT	SPI1_SCK I2S1_CK TIM2_CH2 CMP3_OUT	EXTI3
56	40	27	25	PB4	I/O	FT	SPI1_MISO I2S1_MCK TIM3_CH1 TIM17_BKIN	EXTI4
57	41	28	26	PB5	I/O	FT	SPI1_MOSI I2S1_SD I2C1_SMBA TIM16_BKIN TIM3_CH2	EXTI5
58	42	29	27	PB6	I/O	FT	I2C1_SCL USART1_TX TIM16_CH1N LPUART_TX	EXTI6
59	43	30	28	PB7	I/O	FT	I2C1_SDA USART1_RX TIM17_CH1N LPUART_RX	EXTI7
60	44	31	1	BOOT0(2)	I		Boot mode configuration	
61	45	32	-	PB8	I/O	FT	I2C1_SCL TIM16_CH1 CAN_RX	EXTI8
62	46	-	-	PB9	I/O	FT	I2C1_SDA IRTIM_IROUT TIM17_CH1 SPI2_NSS I2S2_WS CAN_TX	EXTI9
63	47	0(3)	0(3)	VSS	S		Ground	
64	48	-	-	VDD	S		Digital power supply	

(1). I = input, O = output, I/O = input/output, S = power supply.

(2). By default, the Boot0 pin has a 50 kΩ pull-down resistor.

(3). In the QFN package, the pin 0 is the thermal pad on the package bottom.

(4). FT: 5 V tolerant.

Note:

- Unless otherwise specified, all I/Os are configured in input floating mode during and after resets.
- For details about alternate functions, see section "6.8 Alternate function table".

6.6 Alternate function table

Table 6-2 Alternate function table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0/AIN0	-	USART1_CTS	TIM2_CH1/TIM2_ETRIN	USART2_CTS	-	LPUART_RX/LPUART_TX	-	COMP1_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PA1/AIN1	-	USART1_RTS/USART1_DE	TIM2_CH2	USART2_RTS/USART2_DE	-	TIM15_CH1N	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PA2/AIN2	TIM15_CH1	USART1_TX/USART1_RX	TIM2_CH3	USART2_TX/USART2_RX	-	-	-	COMP2_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PA3/AIN3	TIM15_CH2	USART1_RX/USART1_TX	TIM2_CH4	USART2_RX/USART2_TX	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PA4/AIN4	SPI1_NSS/I2S1_WS	USART1_CK	-	USART2_CK	TIM14_CH1	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PA5/AIN5	SPI1_SCK/I2S1_CK	-	TIM2_CH1/TIM2_ETRIN	-	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PA6/AIN6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	LPUART_CTS	-	TIM16_CH1	-	COMP1_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_RX	-
PA7/AIN7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	-	COMP2_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_TX	RCC_MCO
PA8	RCC_MCO	USART1_CK	TIM1_CH1		-	LPUART_RX/LPUART_TX	-	-	-	-	-	-	-	-	-	-
PA9	TIM15_BKIN	USART1_TX/USART1_RX	TIM1_CH2	LPUART_TX/LPUART_RX	I2C1_SCL	RCC_MCO	-	-	-	-	-	-	-	-	CAN_RX	-
PA10	TIM17_BKIN	USART1_RX/USART1_TX	TIM1_CH3	LPUART_RX/LPUART_TX	I2C1_SDA	-	-	-	-	-	-	-	-	-	CAN_TX	-
PA11	-	USART1_CTS	TIM1_CH4	-	-	I2C2_SCL	-	COMP1_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_RX	-
PA12	-	USART1_RTS/USART1_DE	TIM1_ETR	-	-	I2C2_SDA	-	COMP2_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_TX	-
PA13	CM0_SWD	IRTIM_IROUT	-	LPUART_RX/LPUART_TX	-	-	-	COMP3_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_RX	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA14	CM0_SWCLK	USART1_TX/USART1_RX	-	LPUART_TX//LPUART_RX	-	USART2_TX/USART2_RX	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_TX	-
PA15	SPI1_NSS/I2S1_WS	USART1_RX/USART1_TX	TIM2_CH1/TIM2_ETRIN		-	USART2_RX/USART2_TX	-	-	-	-	-	-	-	-	-	-
PB0/AIN8		TIM3_CH3	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	-	-	-
PB1/AIN9	TIM14_CH1	TIM3_CH4	TIM1_CH3N	LPUART_RTS/LPUART_DE	-	-	-	COMP3_OUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PB2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	-	-	-	I2C1_SMBA
PB3	SPI1_SCK/I2S1_CK	-	TIM2_CH2	-	-	-	-	COMP3_OUT	-	-	-	-	-	-	-	-
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	-	-	-	TIM17_BKIN	-	-	-	-	-	-	-	-	-	-
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-	-	-	-	-	-	-	-	-	-	-
PB6	USART1_TX/USART1_RX	I2C1_SCL	TIM16_CH1N	LPUART_TX/LPUART_RX	-	-	-	-	-	-	-	-	-	-	-	-
PB7	USART1_RX/USART1_TX	I2C1_SDA	TIM17_CH1N	LPUART_RX/LPUART_TX	-	-	-	-	-	-	-	-	-	-	-	-
PB8	-	I2C1_SCL	TIM16_CH1	-	-	-	-	-	-	-	-	-	-	-	CAN_RX	-
PB9	IRTIM_IROUT	I2C1_SDA	TIM17_CH1		-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	-	-	CAN_TX	-
PB10	-	I2C1_SCL	TIM2_CH3	LPUART_TX/LPUART_RX	-	SPI2_SCK/I2S2_CK	I2C2_SCL	-	-	-	-	-	-	-	-	-
PB11	-	I2C1_SDA	TIM2_CH4	LPUART_RX/LPUART_TX	-	-	I2C2_SDA	-	-	-	-	-	-	-	-	-
PB12	SPI1_NSS/I2S1_WS		TIM1_BKIN	LPUART_RTS/LPUART_DE	-	TIM15_BKIN	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	I2C2_SMBA
PB13	SPI1_SCK/I2S1_CK	-	TIM1_CH1N	LPUART_CTS	-	I2C2_SCL	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB14	SPI1_MISO/I2C1_MCK	TIM15_CH1	TIM1_CH2N	LPUART_RTS/LPUART_DE	-	I2C2_SDA	-	-	SPI2_MISO/I2S2_MCK	-	-	-	-	-	-	-
PB15	SPI1_MOSI/I2S1_SD	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-
PC0/AIN10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC1/AIN11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC2/AIN12	-	SPI2_MISO/I2S_MCK	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC3/AIN13	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC4/AIN14		-	-	LPUART_T/LPUART_RX	-	-	-	-	-	-	-	-	-	-	-	-
PC5/AIN15	-	-	-	LPUART_RX/LPUART_TX	-	-	-	-	-	-	-	-	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC10	-	-	-	LPUART_TX/LPUART_RX	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	-	-
PC11	-	-	-	LPUART_RX/LPUART_TX	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_RX	-
PC12	-	-	-	-	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	-	CAN_TX	-
PD2	TIM3_ETR	-	-	LPUART_RTS/LPUART_DE	-	-	-	-	-	-	-	-	-	-	-	-
PF0	-	I2C1_SDA	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF1	-	I2C1_SCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF4		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF5		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PF6	-	I2C1_SCL	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	-	-
PF7	-	I2C1_SDA	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	-	-

7 Packages

7.1 Package outlines

7.1.1 LQFP64

LQFP64 is a 10 mm × 10 mm, 0.5 mm pitch package.

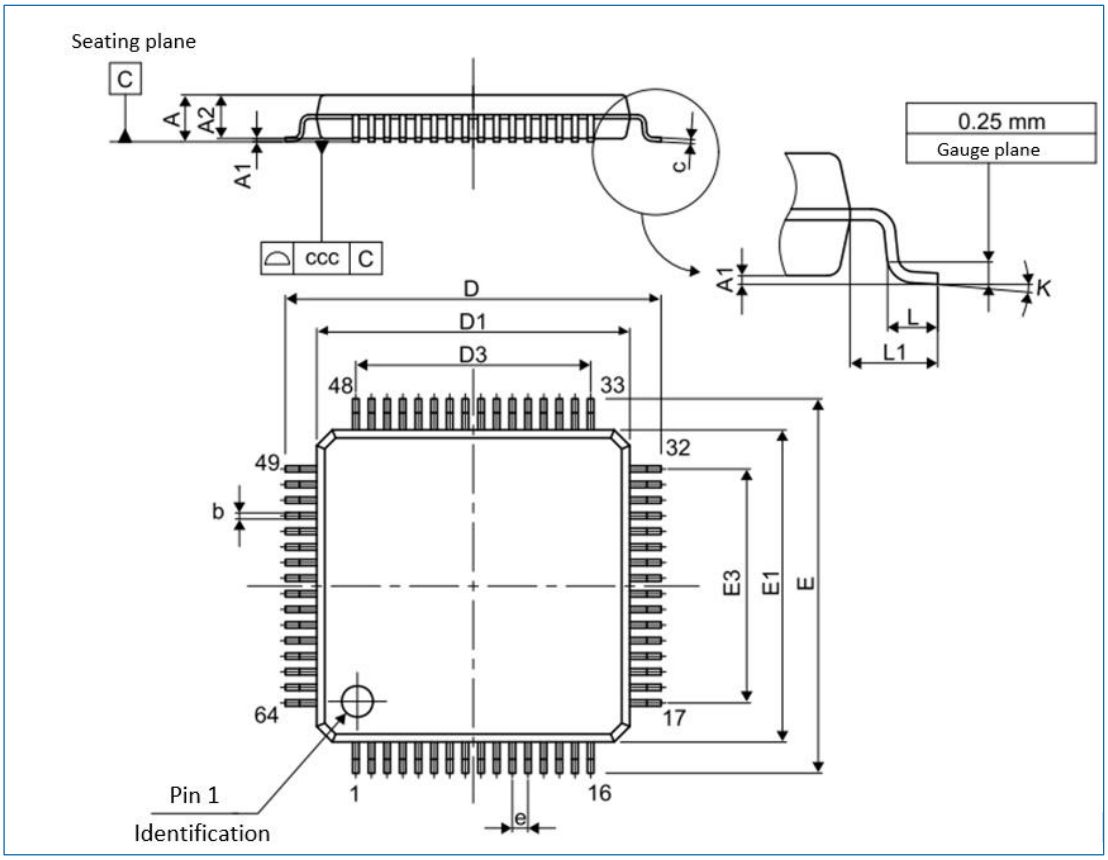

Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.2 LQFP48

LQFP48 is a 7 mm × 7 mm, 0.5 mm pitch package.

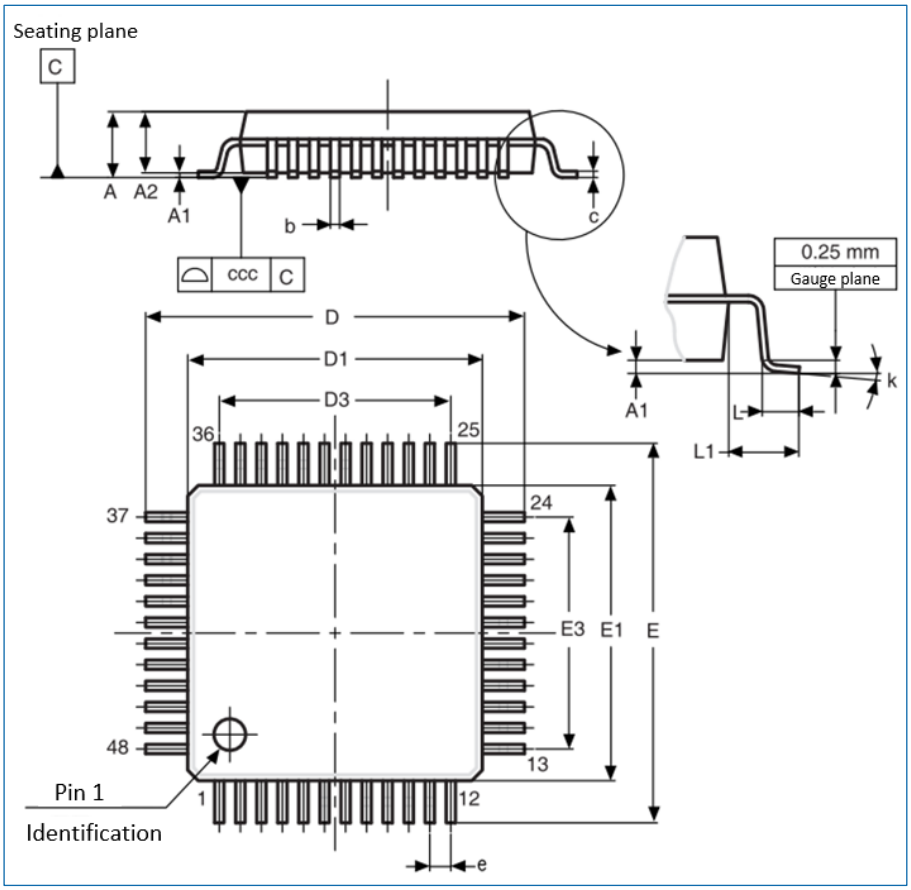

Figure 7-2 LQFP48 package outline

Table 7-2 LQFP48 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	0.080			0.0031		

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.3 QFN32

QFN32 is a 5 mm × 5 mm, 0.5 mm pitch package.

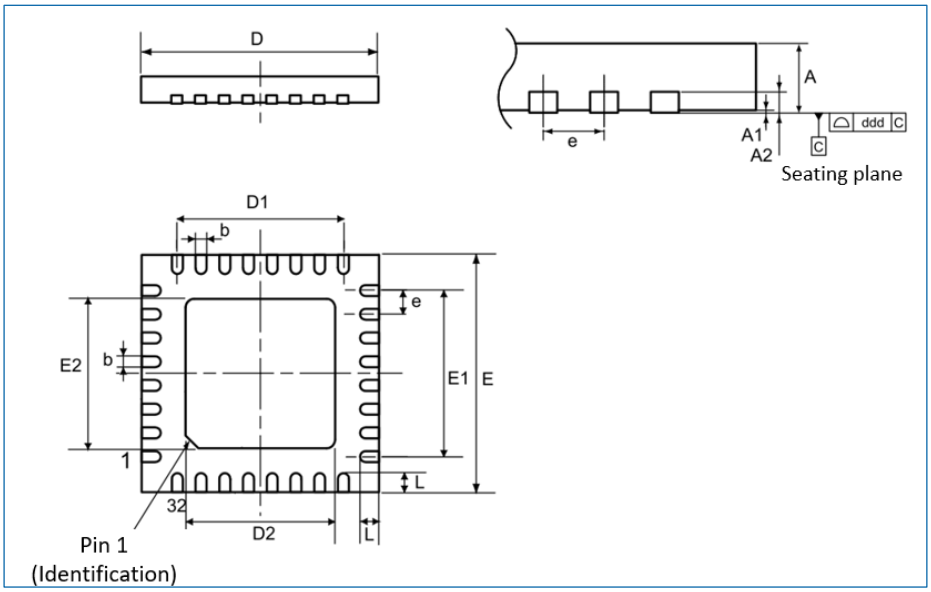

Figure 7-3 QFN32 package outline

Table 7-3 QFN32 package parameters

Symbol	Unit: mm			Unit: inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.500	0.550	0.600	0.0197	0.0217	0.0236
A2	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

(1). The values in inches are converted from the values in millimeters and rounded to four decimal places.

7.1.4 QNF28

QFN28 is a 4 mm × 4 mm, 0.4 mm pitch package.

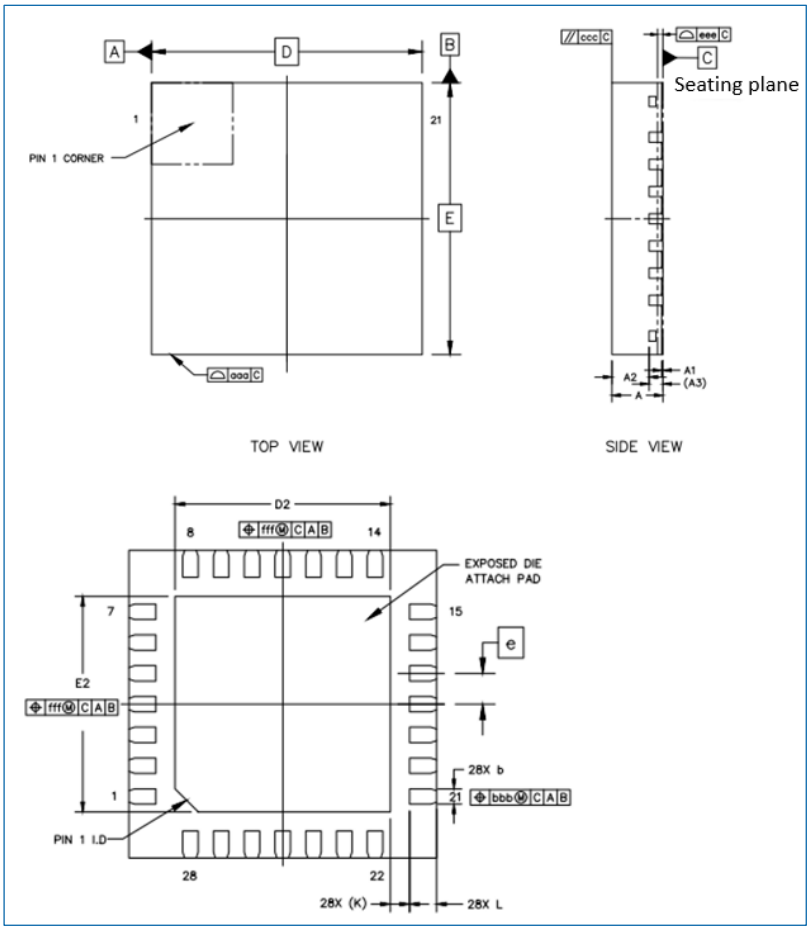

Figure 7-4 QNF28 package outline

Table 7-4 QFN28 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203 REF(1)		
b	0.15	0.20	0.25
D	4 BSC(2)		
E	4 BSC		
e	0.4 BSC		
D2	2.7	2.9	2.9
E2	2.7	2.9	2.9
L	0.3	0.35	0.4
K	0.25 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

(1). REF indicates a reference value.

(2). BSC: basic spacing between centers.

7.2 Device marking

The device marking consists of the Hangshun logo, ARM logo, part number, and lot number. The following table describes the lot number:

Table 7-5 Lot number description

Lot Number	Description
First character	The year when the MCU was manufactured. For example, 1 indicates the year 2021.
Second and third characters	The assembly factory.
Fourth and fifth characters	The week in which the order was placed. For example, 18 indicates that the order was placed in the 18th week of the year.
Sixth, seventh, and eighth characters	The last three characters of the wafer lot number.

7.2.1 LQFP64 marking

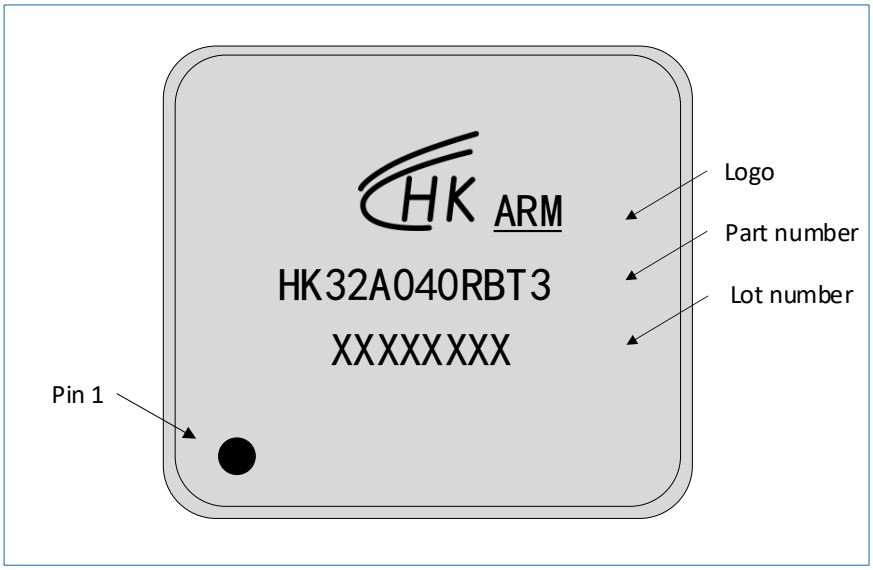

Figure 7-5 LQFP64 HK32A040RBT3 marking example

7.2.2 LQFP48 marking

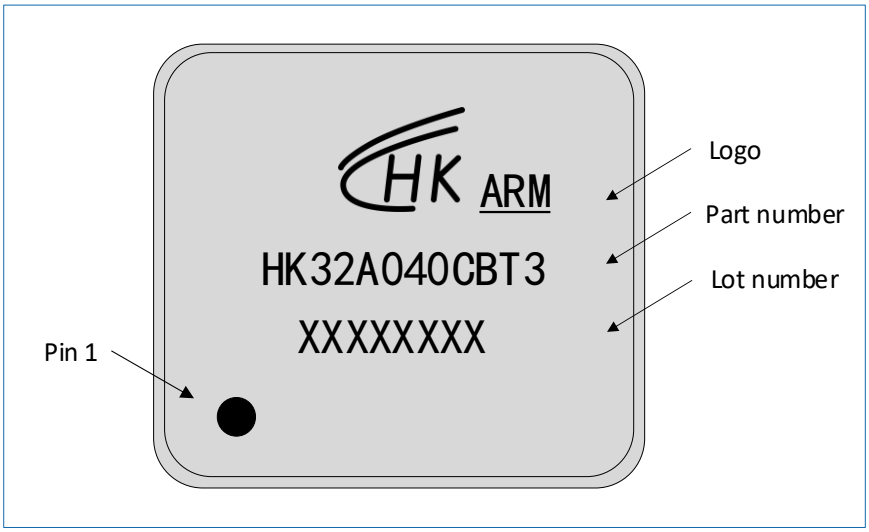

Figure 7-6 LQFP48 HK32A040CBT3 marking example

7.2.3 QFN32 marking

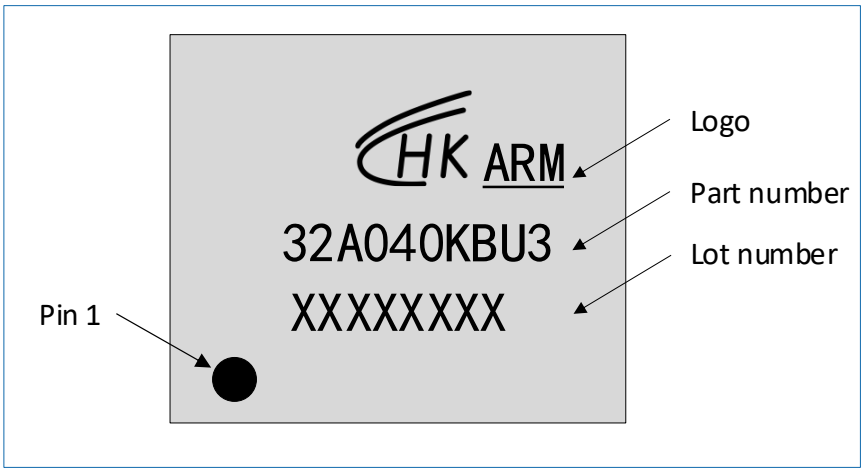

Figure 7-7 QFN32 HK32A040KBU3 marking example

7.2.4 QFN28 marking

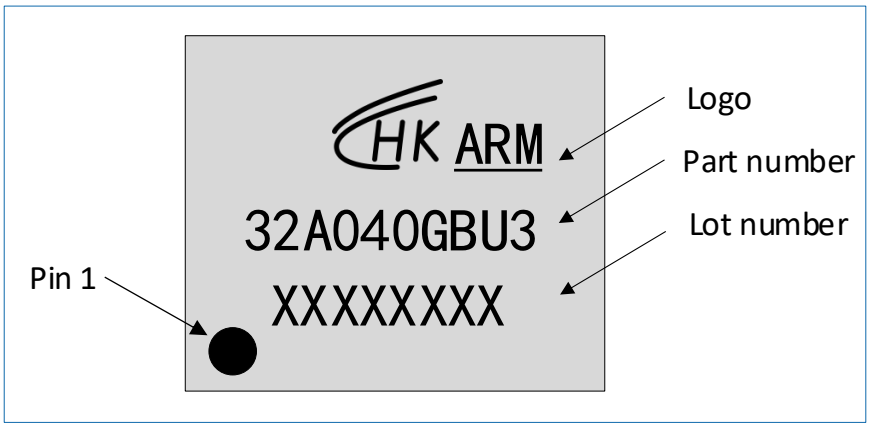

Figure 7-8 QFN28 H32A040GBU3 marking example

8 Ordering information

8.1 Device numbering conventions

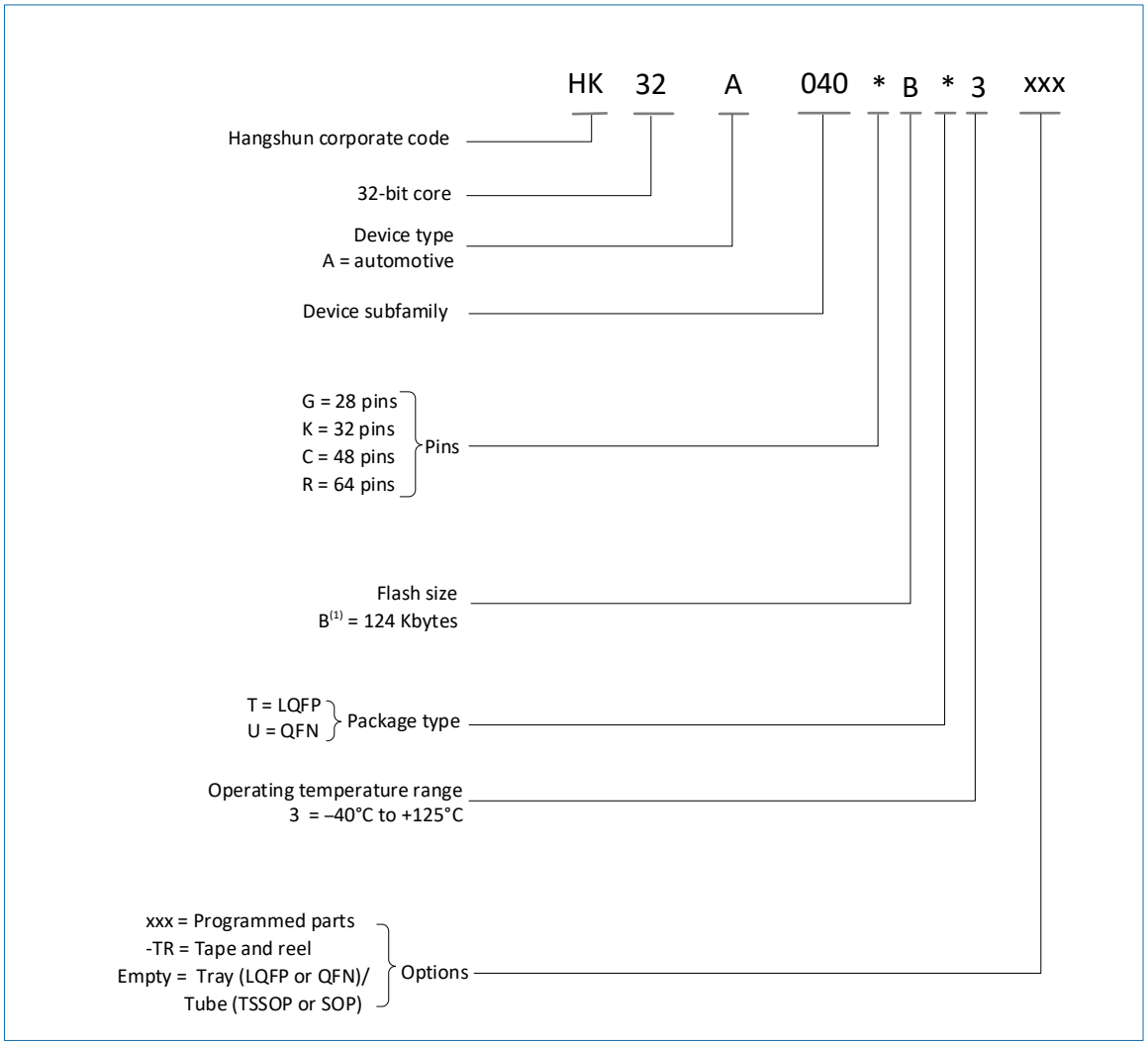

Figure 8-1 Device numbering conventions

Note:

(1). The device numbering of HK32A040 is based on *Hangshun Product Naming Conventions V0.9*, which is slightly different from the latest naming conventions.

8.2 Packaging information

Table 8-1 HK32A040 ordering information

Package	Part Number	Shipping Option	Remarks
LQFP64	HK32A040RBT3	Tray	-
LQFP64	HK32A040RBT3-TR	Tape and reel	-
LQFP48	HK32A040CBT3	Tray	-
LQFP48	HK32A040CBT3-TR	Tape and reel	-
QFN32	HK32A040KBU3	Tray	-
QFN32	HK32A040KBU3-TR	Tape and reel	-
QFN28	HK32A040GBU3	Tray	-
QFN28	HK32A040GBU3-TR	Tape and reel	-

9 Acronyms

Term	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-wakeup Unit
CLU	Configurable Logic Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EMACC	Electric Motor Acceleration
EXTI	Extended Interrupt/Event Controller
FT	5 V-tolerant
GPIO	General-purpose Input/Output
HSE	High Speed External (Clock Signal)
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low Speed Internal (clock signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-down Reset
PLL	Phase-locked Loop
POR	Power-on Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computer
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
WWDG	Window Watchdog

10 Legal and contact information

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