HK25Q80C

DATASHEET

Contents

FEATURES

- **Single power supply operation**
  - Full voltage range: 2.7-3.6 volt
- **8 Mbit Serial Flash**
  - 8 M-bit/1024 K-byte/4096 pages
  - 256 bytes per programmable page
  - Uniform 4K-byte Sectors/64K-byte Blocks
- **Standard and Dual**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DIO, DO, WP#
  - Fast Read Dual Output instruction
  - Auto-increment Read capability
- **Temperature Ranges**
  - Industrial (-40°C to +85°C)
  - Automotive (-40°C to +105°C)
- **Low power consumption**
  - 9 mA typical active current
  - 2 uA typical power down current
- **Flexible Architecture with 4KB sectors**
  - Sector Erase (4K-bytes)
  - Block Erase (64K-bytes)
  - Page Program up to 256 bytes
  - More than 100K erase/write cycles
  - More than 20-year data retention
- **Software and Hardware Write Protection**
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- **High performance program/erase speed**
  - Page program time: 0.5ms typical
  - Sector erase time: 40ms typical
  - Block erase time: 250ms typical
  - Chip erase time: 6 Seconds typical
- **Package Options**
  - 8-pin SOIC 150/208-mil
  - 8-pad WSON 6x5-mm
  - 8-pin PDIP 300-mil
  - All Pb-free packages are RoHS compliant

GENERAL DESCRIPTION

The HK25Q80C of non-volatile flash memory devices supports the standard Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO). This multiple width interface is called SPI Multi-I/O or MIO.

The SPI protocols use only 4 signals:

◆ Chip Select (CS#)

◆ Serial Clock (CLK)

◆ Serial Data

- IO0 (DIO)
- IO1 (DO)

The DIO protocol uses Serial Input (DI) and Serial Output (DO) for data transfer. The DIO protocols use IO0 and IO1 to input or output two bits of data in each clock cycle.

The Write Protect (WP#) input signal option allows hardware control over data protection. Software controlled commands can also manage data protection.

The SPI clock frequencies of up to 100MHz are supported allowing equivalent clock rates of 100MHz for Dual Output. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

◆ The HK25Q80C also offers a sophisticated method for protecting individual blocks against erroneous or malicious program and erase operations. By providing the ability to individually protect and unprotect blocks, a system can unprotect a specific block to modify its contents while keeping the remaining blocks of the memory array securely protected. This is useful in applications where program code is patched or updated on a subroutine or module basis, or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments.

◆ The HK25Q80C is designed to allow either single Sector/Block at a time or full chip erase operation. The HK25Q80C can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

◆ The HK25Q80C provides an ideal storage solution for systems with limited space, signal connections, and power. These memories' flexibility and performance is better than ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

1. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:

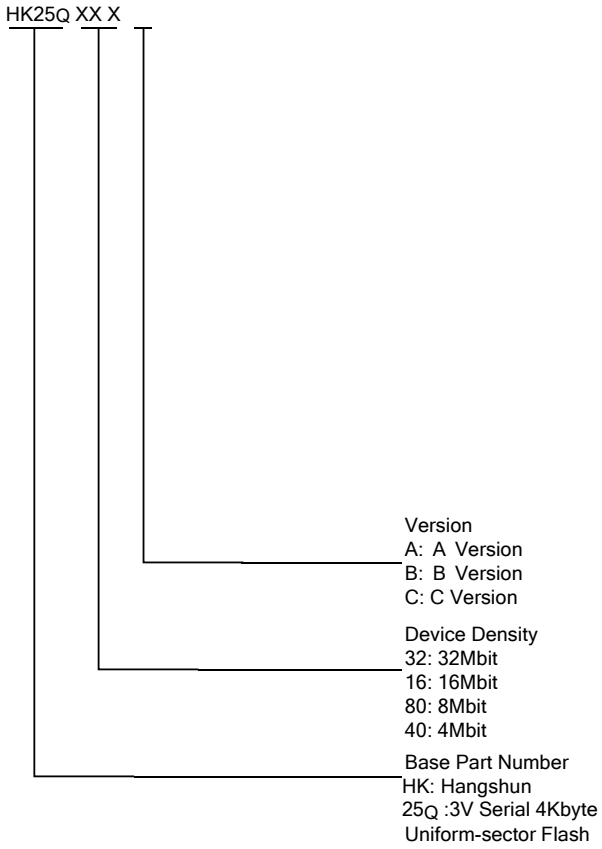


Figure 1 Ordering Information

2. BLOCK DIAGRAM

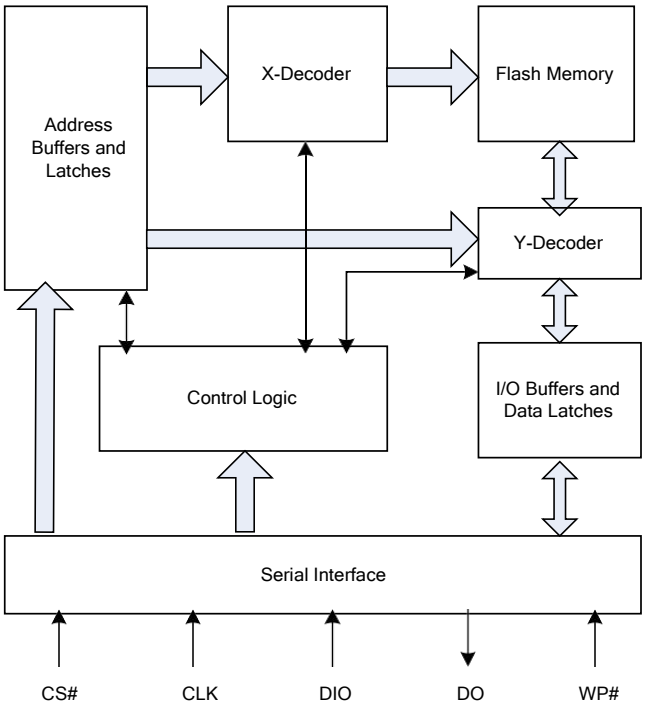


Figure 2.1 Block Diagram

3. CONNECTION DIAGRAMS

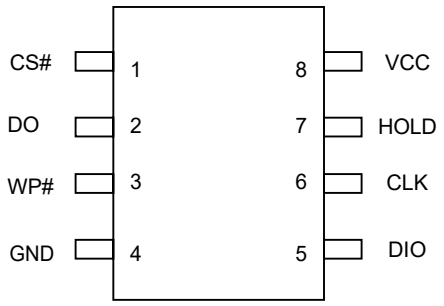


Figure 3.1 8-pin SOP (150/208mil)/ PDIP (300mil)

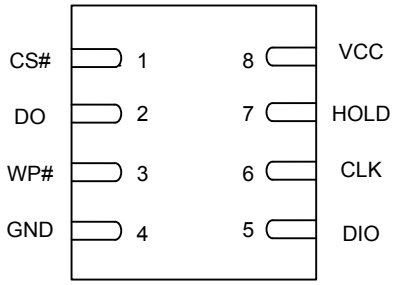


Figure 3.2 8-Contact 6 x 5 mm WSON

4. SIGNAL DESCRIPTIONS

4.1. Serial Data Input/Output (DIO)

The SPI Serial Data Input/Output (DIO) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DIO pin is also used as an output pin when the Fast Read Dual Output instruction is executed.

4.2. Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

4.3. Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

4.4. Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output pins are at high impedance.

When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

4.5. Write Protect (WP#)

Write Protect in single bit or Dual data commands. The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1and BP2, BP3) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

Table 4.1 Pin Descriptions

Symbol	Pin Name
CLK	Serial Clock Input
DIO	Serial Data Input / Output (1)
DO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
V_{CC}	Supply Voltage (2.7-3.6V)
GND	Ground

Notes:
(1) DIO output is used for Dual instructions.

5. MEMORY ORGANIZATIONS

5.1. The memory is organized as:

- 1,048,576bytes
- Uniform Sector Architecture 16 blocks of 64-Kbyte
- 256 sectors of 4-Kbyte
- 4,096 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 5(1) Memory Organization

Block	Sector	Address range	
15	255	0FF000H	0FFFFFH
	.....	.....	.....
	240	0F0000H	0F0FFFH
14	239		
	.....	.....	.....
	224	0E0000H	0E0FFFH
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
.....	.....	.....	.....
	.....	.....	.....
	.....	.....	.....
2	47	02F000H	02FFFFH
	.....	.....	.....
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	.....	.....	.....
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	.....	.....	.....
	0	000000H	000FFFH

Notes:
(1) These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4-kB sectors have the pattern XXX000h-XXXFFFh.

6. FUNCTION DESCRIPTION

6.1. SPI Modes

The HK25Q80C can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the CLK signal and the output data is always available from the falling edge of the CLK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- CLK will stay at logic low state with CPOL = 0, CPHA = 0
- CLK will stay at logic high state with CPOL = 1, CPHA = 1

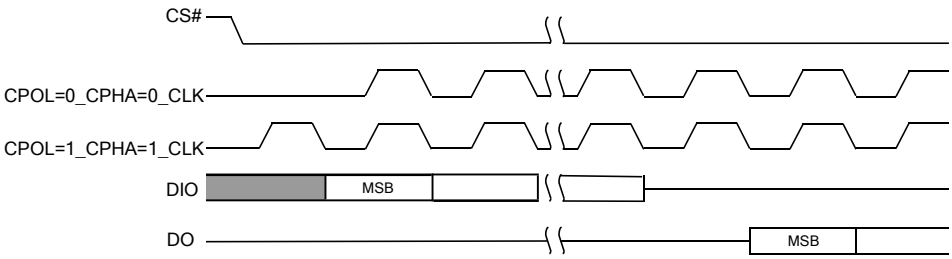


Figure 6.1 SPI Modes

Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing CLK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with CLK low at the fall of CS#. In such a case, mode 3 timing simply means clock is high at the fall of CS# so no CLK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

CLK cycles are measured (counted) from one falling edge of CLK to the next falling edge of CLK. In mode 0 the beginning of the first CLK cycle in a command is measured from the falling edge of CS# to the first falling edge of CLK because CLK is already low at the beginning of a command.

6.2. Dual Output SPI

The HK25Q80C supports Dual Output Operation when using the “Fast Read with Dual Output” (3B hex) instruction. This feature allows data to be transferred from the Serial Flash at twice the rate possible with the standard SPI. This instruction is ideal for quickly downloading code from Flash to RAM upon Power-up (Code-shadowing) or for applications that cache code-segments to RAM for execution. The Dual Output feature simply allows the SPI input pin to also serve as an output during this instruction. All other operations use the standard SPI interface with single signal.

6.3. Status Register

Status Register can be used to provide status on the availability of the flash memory array, if the device is write enabled or disabled, the state of write protection, setting, Security Register lock status, and Erase / Program Suspend status. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

Table 6.1(1) Status Register Bit Locations

R7	R6	R5	R4	R3	R2	R1	R0
SRP	Reserved	BP3	BP2	BP1	BP0	WEL	BUSY

Notes:
(1) Please contact sales for more information.

- **BUSY** is a read only bit in the status register (R0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

- **Write Enable Latch (WEL)** is a read only bit in the status register (R1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

- **Block Protect Bits (BP3, BP2, BP1, BP0)** are non-volatile read/write bits in the status register (R5, R4, R3 and R2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits cannot be written, if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (WP#) pin is low.

- **The Status Register Protect (SRP)** bit is a non-volatile read/write bit in status register (R7) that can be used in conjunction with the Write Protect (WP#) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default) the (WP#) pin has no control over status register. When the SRP pin is set to a 1, the non-volatile bits of the Status Register(SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is not execution while the (WP#) pin is low. When the (WP#) pin is high the Write Status Register instruction is allowed.

6.4. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the HK25Q80C provide the following data protection mechanisms:

- Device resets when V_{CC} is below threshold
- Time delay write disable after Power-Up
- Write enable / disable commands and automatic write disable after erase or program
- Command length protection
  - All commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8 bits have been clocked) otherwise the command will be ignored.

- ◆ Software and Hardware write protection using Status Register control
  - WP# input protection
  - Lock Down write protection until next power-up or Software Reset
  - One-Time Program (OTP) write protection

- ◆ Write Protection using the Deep Power-Down command

Upon power-up or at power-down, the HK25Q80C will maintain a reset condition while VCC is below the threshold value of VWI, (see Figure 8.1). While reset, all operations are disabled and no commands are recognized. During power-up and after the V_{CC} voltage exceeds VWI, all program and erase related commands are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Registers commands. Note that the chip select pin (CS#) must track the V_{CC} supply level at power-up until the V_{CC}-min level and t_{VSL} time delay is reached. If needed a pull-up resistor on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Registers command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled main flash array write protection is facilitated using the Write Status Registers command to write the Status Register Protect (SRP) and Block Protect (BP3, BP2, BP1 and BP0) bits.

The BP method allows a portion as small as 4-kB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See the Table 6.1. for further information.

Additionally, the Deep Power-Down (DPD) command offers an alternative means of data protection as all commands are ignored during the DPD state, except for the Release from Deep-Power-Down (RES ABh) command. Thus, preventing any program or erase during the DPD state.

Table 6.2 Protected Area Sizes Block Organization

Status Bit			HK25Q 80C (8Mb) Block Protection
BP2	BP1	BP0	Protect Level
0	0	0	0(none)
0	0	1	1(1 block, block 15th)
0	1	0	2(2 blocks, block 14th-15th)
0	1	1	3(4 blocks, block 12th-15th)
1	0	0	4(8 blocks, block 8th-15th)
1	0	1	5(16 blocks, all)
1	1	0	6(16 blocks, all)
1	1	1	7(16 blocks, all)

6.5. Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}). To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

6.6. Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE} t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

6.7. Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

6.8. Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to ICC1.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to ICC2. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

7. INSTRUCTIONS

The instruction set of the HK25Q80C consists of fifteen basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DIO input provides the instruction code. Data on the DIO input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in figures 7.1 through 7.5. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

Table 7.1(1) Instruction Set

INSTRUCTION NAME	BYTE1 (CODE)	BYTE2	BYTE3	BYTE4	BYTE5	BYTE6	N-BYTES
Write Enable	06h						
write Disable	04h						
Read Status Register	05h	(S7-S0)(2)					
Write Status Register	01h	(S7-S0)(2)					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next byte) continuous
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	DIO= (D6,D4,D2,D0) DO= (D7,D5,D3,D1)	(One byte per 4 clocks, continuous)
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	Up to 256 bytes
Block Erase(64KB)	D8h	A23-A16	A15-A8	A7-A0			
Half Block Erase(32KB)	52h	A23-A16	A15-A8	A7-A0			
Sector Erase(4KB)	20h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Power-down	B9h						
Release Power-down /Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)(4)		
Manufacturer /Device ID(3)	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	
JEDEC ID	9Fh	(M7-M0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity			

Notes:
(1) Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the DO pin.
(2) The Status Register contents will repeat continuously until CS# terminates the instruction.
(3) See Manufacturer and Device Identification table for Device ID information.
(4) The Device ID will repeat continuously until CS# terminates the instruction.

Table 7.2(1) Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh	-	-	13h
90h	5E	-	13h
9Fh	5E	40h	14h

Notes:
(1) Please contact sales for more information

7.1. Write Enable (06h)

The Write Enable instruction (Figure 7.1) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

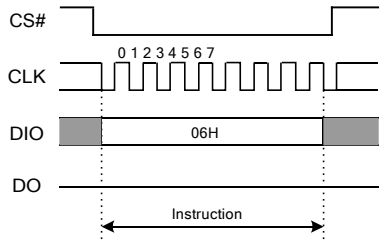


Figure 7.1 Write Enable Instruction Sequence Diagram

7.2. Write Disable (04h)

The Write Disable instruction (Figure 7.2) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code “04h” into the DIO pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

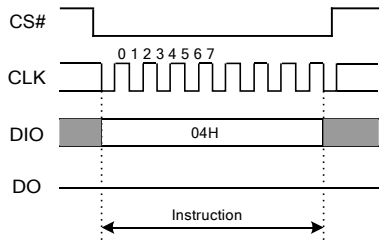


Figure 7.2 Write Disable Instruction Sequence Diagram

7.3. Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h” into the DIO pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 7.3. The Status Register bits are shown in table 6.1.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. Status Registers can be read continuously as each repeated data output delivers the updated current value of each status register.. The instruction is completed by driving CS# high.

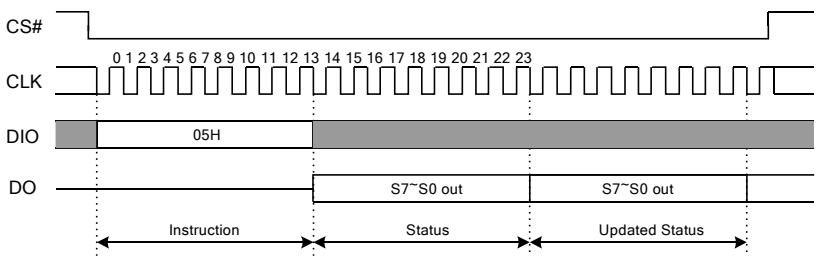


Figure 7.3 Read Status Register Instruction Sequence Diagram

7.4. Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7.4. The Status Register bits are shown in table 6.1 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP, BP3, BP2, BP1 and BP0 (bits 7, 5, 4, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

During non-volatile Status Register write operation (06h combined with 01h), the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After CS# is driven high, the self- timed Write Status Register cycle will commence for a time duration of t_W (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high at the end of the Write Status Registers command, the Status Register bits will be updated to the new values within the time period of t_{SHSL} (see the AC Electrical Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction allows the Block Protect bits (BP3, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect WP# pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the WP# pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the WP# pin is low. When the WP# pin is high the Write Status Register instruction is allowed.

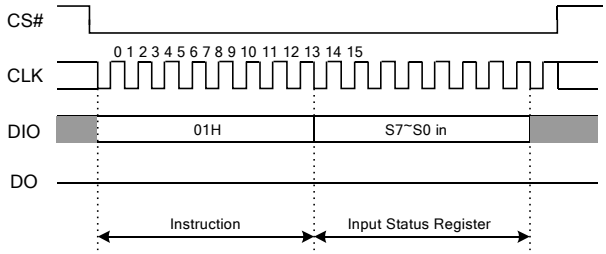


Figure 7.4 Write Status Register Instruction Sequence Diagram

7.5. Read Data (Read) (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DIO pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in figure 7.5. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

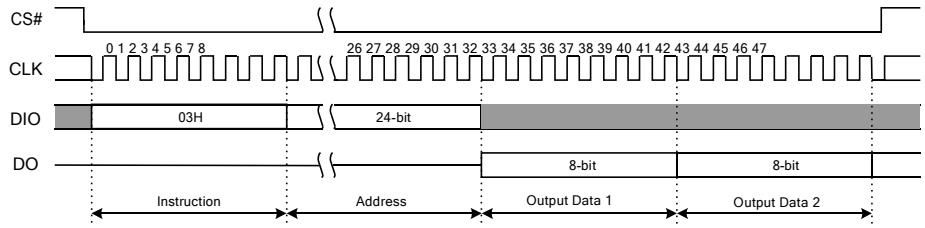


Figure 7.5 Read Data Instruction Sequence Diagram

7.6. Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 7.6. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DIO pin is a “don’t care”.

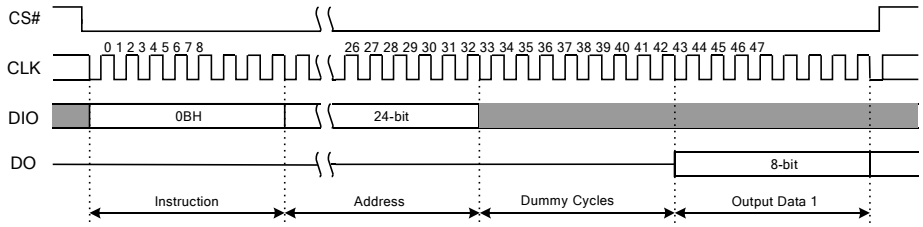


Figure 7.6 Fast Read Instruction Sequence Diagram

7.7. Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the HK25Q80C at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_R (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 7.7. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DIO pin should be high-impedance prior to the falling edge of the first data out clock.

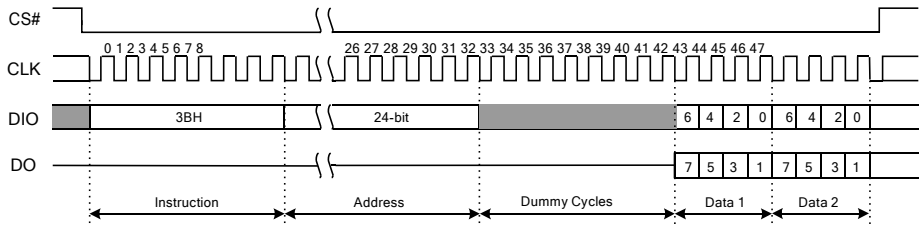


Figure 7.7 Fast Read Dual Output Instruction Sequence Diagram

7.7. Page Program (PP) (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DIO pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 7.7.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of t_{pp} (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

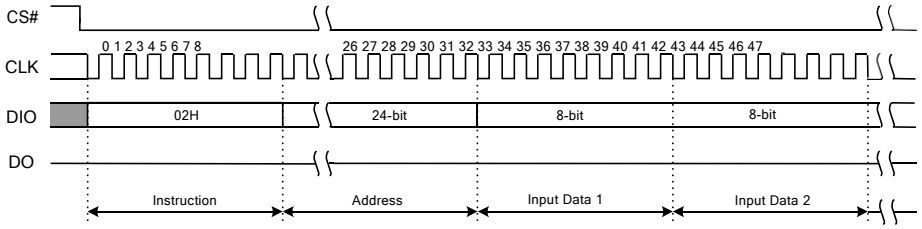


Figure 7.7 Page Program Instruction Sequence Diagram

7.8. Sector Erase (SE) (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in figure 7.8.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

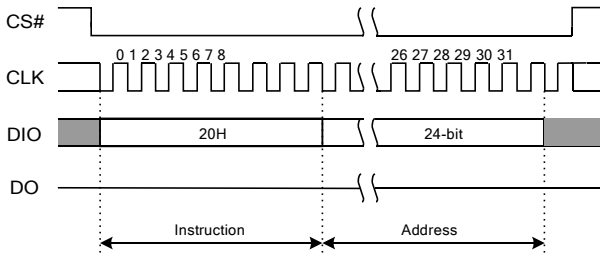


Figure 7.8 Sector Erase Instruction Sequence Diagram

7.9. Block Erase (BE) (D8h) and Half Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) or half block (32K- bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL mustequal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D8h” or “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in figure 7.9.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

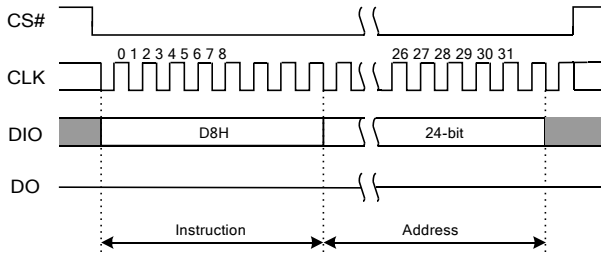


Figure 7.9 Block Erase Instruction Sequence Diagram

7.10. Chip Erase (CE) (C7h or 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 7.10.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP3,BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

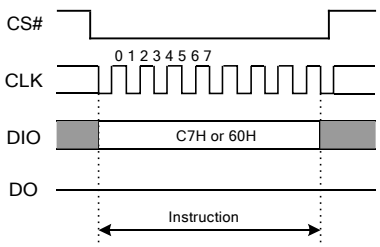


Figure 7.10 Chip Erase Instruction Sequence Diagram

7.11. Deep Power-down (DP) (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power- down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the CS# pin low and shifting the instruction code “B9h” as shown in figure 7.11.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power- down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

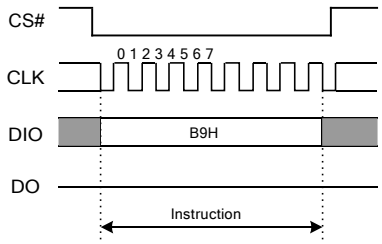


Figure 7.11 Deep Power-down Instruction Sequence Diagram

7.12. Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

To release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in figure 7.12. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 7.13. The Device ID value for the HK25Q80C is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 7.13, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

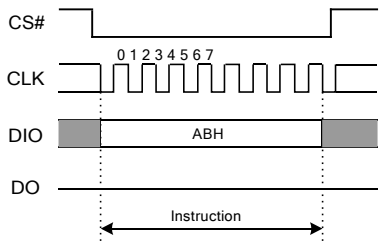


Figure 7.12 Release Power-down Instruction Sequence

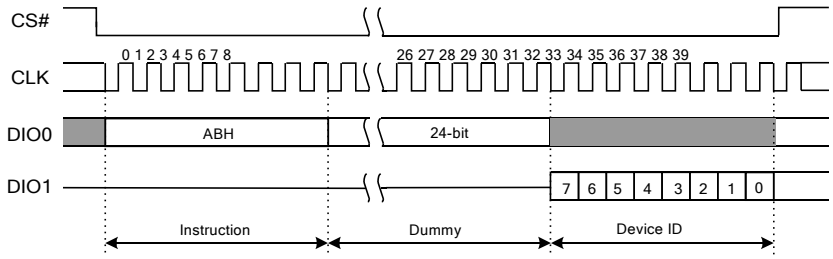


Figure 7.13 Release Power-down / Device ID Instruction Sequence Diagram

7.13. Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7.14. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high..

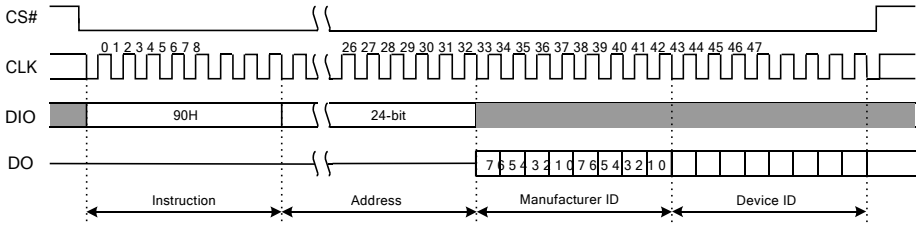


Figure 7.14 Read Manufacturer / Device ID Diagram

7.13. Read Identification (RDID) (9Fh)

For compatibility reasons, the HK25Q80C provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 7.15. For memory type and capacity values refer to Manufacturer and Device Identification table.

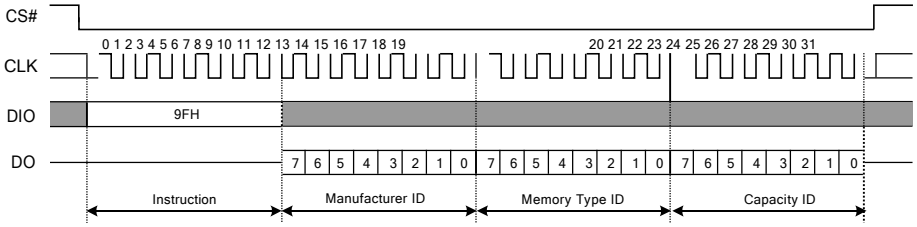


Figure 7.15 Read JEDEC ID instruction Sequence Diagram

8. ELECTRICAL CHARACTERISTIC

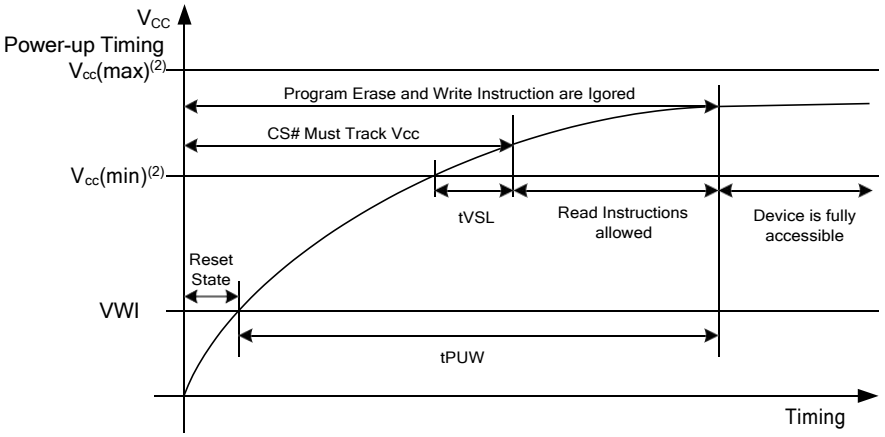


Figure 8.1 Power-up Timing

Table 8.1 Power-up Timing

PARAMETER	SYMBOL	TYPE		UNIT
		MIN	MAX	
Vcc(min) to CS# Low	t_{VSL}(1)	10	-	μs
Time Delay Before Write Instruction	t_{PUW}(1)	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1	2	V

Notes:
(1) The parameters are characterized only.
(2) V_{CC} (max.) is 3.6V and V_{CC} (min.) is 2.7V.

8.1. Absolute Maximum Ratings

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values.

Table 8.2(1) Absolute Maximum Ratings

PARAMETERS(2)	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	V_{CC}		-0.6 to +4.0	V
Voltage applied on any pin	V_{IO}	Relative to Ground	-0.6 to V_{CC}+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20ns Transient Relative to Ground	-2.0 to V_{CC}+2.0	V
Storage Temperature	T_{STG}		-65 to +150	℃
Lead Temperature	T_{LEAD}		See Note(3)	℃
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model(4)	-2000 to +2000	V

Notes:
(1) Specification for HK25Q80C is preliminary. See preliminary designation at the end of this document.
(2) This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
(3) Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
(4) JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

8.2. Recommended Operating Ranges：

Table 8.3 Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	V_{CC}(1)	F_R=100MHz,f_R=55MHz	2.7	3.6	V
Ambient Temperature, Operating	T_A	Industrial	-40	+85	℃

Notes:
(1) Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.

8.3. DC Characteristics

Table 8.4 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
CIN(1)	Input Capacitance	VIN = 0V(2)			6	pF
COUT(1)	Output Capacitance	VOUT = 0V(2)			8	pF
ILI	Input Leakage				±2	μA
ILO	I/O Leakage				±2	μA
ICC1	Standby Current	CS# = V_{CC}, VIN= GND or V_{CC}		12	15	μA
ICC2	Power-down Current	CS# = V_{CC}, VIN= GND or V_{CC}		2	5	μA
ICC3	Current Read Data / Dual Output Read 33MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		6/7	9/10	mA
ICC3	Current Read Data / Dual Output Read 85MHz(2)	C = 0.1 V_{CC} / 0.9 V_{CC} DO = Open		9/10	13/15	mA
ICC4	Current Page Program	CS# = V_{CC}			10	mA
ICC5	Current Write Status Register	CS# = V_{CC}			10	mA
ICC6	Current Sector/Block Erase	CS# = V_{CC}			10	mA
ICC7	Current Chip Erase	CS# = V_{CC}			10	mA
VIL	Input Low Voltage		- 0.5		V_{CC}×0.2	V
VIH	Input High Voltage		V_{CC}×0.7		V_{CC}+0.4	V
VOL	Output Low Voltage	IOL = 1.6 mA	V_{SS}		0.4	V
VOH	Output High Voltage	IOH = - 100 μA	V_{CC} - 0.2		V_{CC}	V

Notes:
(1) Tested on sample basis and specified through design and characterization data. T_A=25° C, V_{CC}=3V.
(2) Checker Board Pattern.

8.4. AC Measurement Conditions

Table 8.5 AC Measurement Conditions

Symbol	PARAMETER	Min.	Max.	Unit
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
VtIN	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
VtON	Output Timing Reference Voltages	0.5 V_{CC} to 0.5 V_{CC}		V

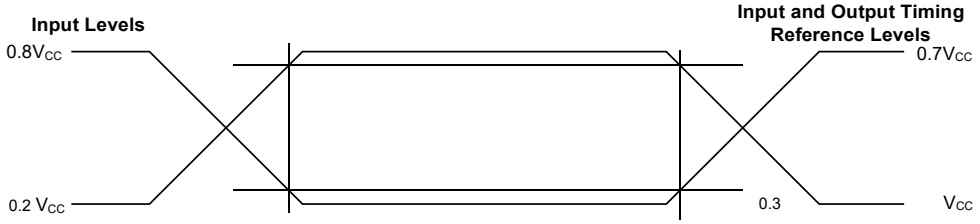


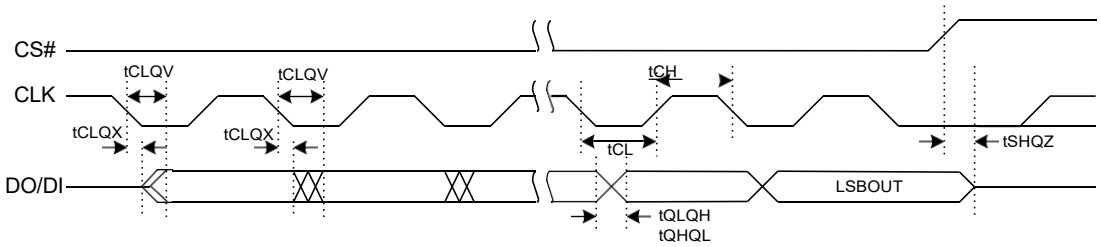
Figure 8.2 AC Measurement I/O Waveform

8.5. AC Electrical Characteristics

Table 8.6 AC Electrical Characteristics

SYMBOL	ALT	Parameter	SPEC			UNIT
			MIN	TYP	MAX	
F_R	f_C	Clock frequency For all instructions, except Read Data (03h) and Dual output(3bh) 2.7V-3.6V V_{CC} & Industrial Temperature	D.C.		100	MHz
f_R		Clock freq. Read Data instruction (03h)	D.C.		55	MHz
t_{CLH}, t_{CLL} (1)		Clock High, Low Time for all instructions except Read Data (03h)	4			ns
t_{CRLH}, t_{CRLL} (1)		Clock High, Low Time for Read Data (03h) instruction	4			ns
t_{CLCH} (2)		Clock Rise Time peak to peak	0.1			V/ns
t_{CHCL} (2)		Clock Fall Time peak to peak	0.1			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time relative to CLK	5			ns
t_{CHSL}		CS# Not Active Hold Time relative to CLK	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		CS# Active Hold Time relative to CLK	5			ns
t_{SHCH}		CS# Not Active Setup Time relative to CLK	5			ns
t_{SHSL}	t_{CSH}	CS# Deselect Time (for Array Read Array Read / Erase or Program Read Status Register)	40/130			ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time			7	ns
t_{CLQV}	t_V	Clock Low to Output Valid 2.7V- 3.6V			7	ns
t_{CLQX}	t_{HO}	Output Hold Time	2			ns
t_{WHSL} (3)		Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL} (3)		Write Protect Hold Time After CS# High	100			ns
t_{DP} (2)		CS# High to Power-down Mode			3	us
t_{RES1} (2)		CS# High to Standby Mode without Electronic Signature Read			8	us
t_{RES2} (2)		CS# High to Standby Mode with Electronic Signature Read			8	us
t_W		Write Status Register Time		4	120	ms
t_{PP}		Page Program Time		0.5	1	ms
t_{SE}		Sector Erase Time (4KB)		40	200	ms
t_{BE}		Block Erase Time (64KB)		0.25	5	s
t_{CE}		Chip Erase Time		3	12	s

Notes:
(1) Clock high + Clock low must be less than or equal to $1/f_C$.
(2) Value guaranteed by design and/or characterization, not 100% tested in production.
(3) Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1. 4, For multiple bytes after first byte within a page, $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical) and $t_{BPN} = t_{BP1} + t_{BP2} * N$ (max), where N = number of bytes programmed.



*DIO IS AN OUTPUT ONLY FOR THE FAST READ DUAL OUTPUT INSTRUCTIONS (3BH)

Figure 8.3 Serial Output Timing

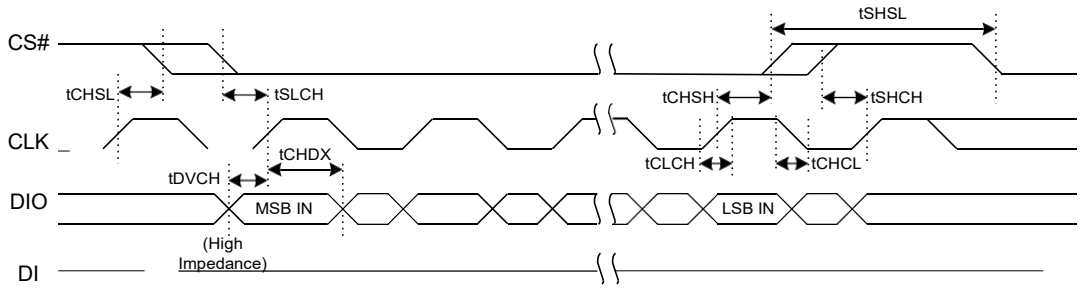
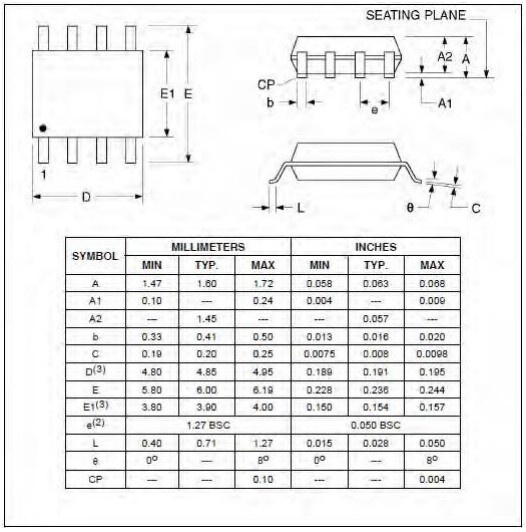


Figure 8.4 Input Timing

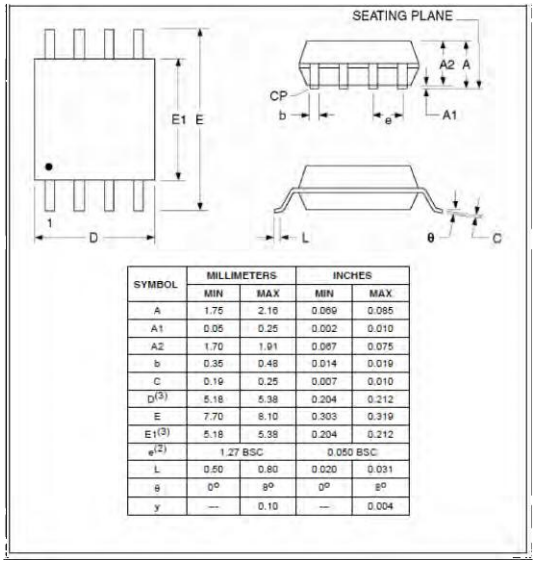
9. PACKAGE MECHANICAL

9.1. 8-Pin SOIC 150-mil



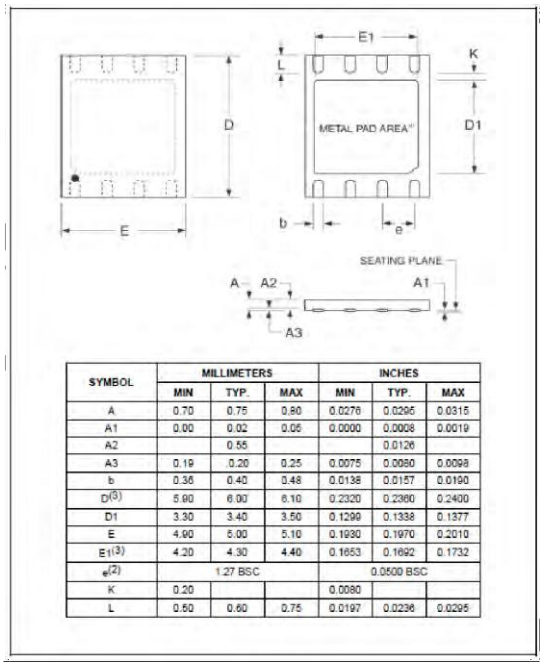
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	1.47	1.60	1.72	0.058	0.063	0.068
A1	0.10	---	0.24	0.004	---	0.009
A2	---	1.45	---	---	0.057	---
b	0.33	0.41	0.50	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D(3)	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.19	0.228	0.236	0.244
E1(3)	3.80	3.90	4.00	0.150	0.154	0.157
e(2)	1.27 BSC			0.050 BSC		
L	0.40	0.71	1.27	0.015	0.028	0.050
θ	0°	---	8°	0°	---	8°
CP	---	---	0.10	---	---	0.004

9.2. 8-Pin SOIC 208-mil



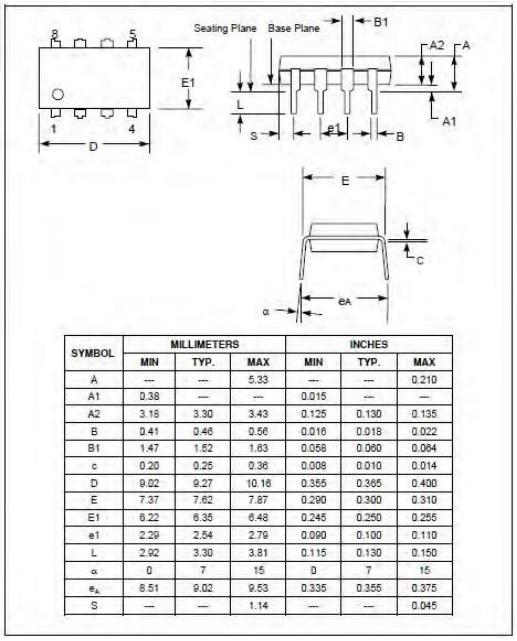
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D(3)	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1(3)	5.18	5.38	0.204	0.212
e(2)	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

9.3. 8-Contact WSON (6x5mm)



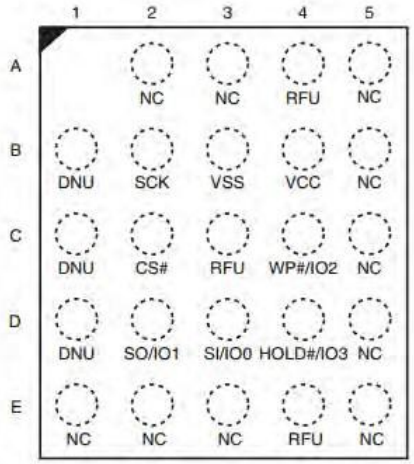
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	0.20	0.25	0.0075	0.0080	0.0098
b	0.35	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.20	4.30	4.40	0.1653	0.1692	0.1732
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

9.4. 8-Pin PDIP 300-mil

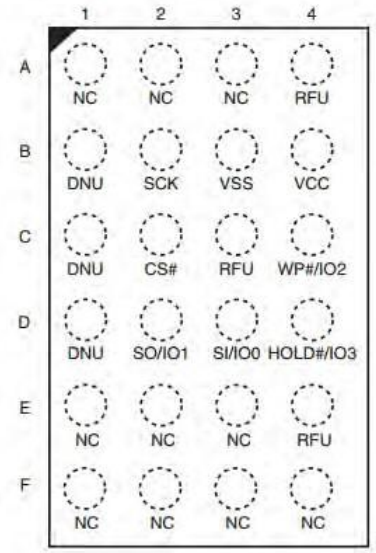


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	---	---	5.33	---	---	0.210
A1	0.38	---	---	0.015	---	---
A2	3.18	3.30	3.43	0.125	0.130	0.135
B	0.41	0.46	0.56	0.016	0.018	0.022
B1	1.47	1.52	1.63	0.058	0.060	0.064
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.37	7.62	7.87	0.290	0.300	0.310
E1	6.22	6.35	6.48	0.245	0.250	0.255
e1	2.29	2.54	2.79	0.090	0.100	0.110
L	2.92	3.30	3.81	0.115	0.130	0.150
α	0	7	15	0	7	15
eA	8.51	9.02	9.53	0.335	0.355	0.375
S	---	---	1.14	---	---	0.045

9.5. FAB024 24-Ball BGA



9.6. FAC024 24-Ball BGA Package



REVISION LIST

Version No.	Description	Date
A	Initial Release	2016/04/07